Ketra Inc.

Ketra VER006 2.4GHz ZigBee Module

Operational Description

Part #: 830-000057-xx

	Title Ketra VER006 2.4GHz ZigBee Module – Operational Description		
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Description

Version: 006
Zigbee IC: Silicon Laboratories EM3585
FEM IC: RFMD 6525
Antenna: 2.4GHz meander antenna
Aux RF: RFOUT pin on edge connector

Features

Transmit Power:	+20 dBm	Board Size:	0.690” x 0.940”
Sensitivity:	-102 dBm	PCB:	0.031”, 4-layer FR4
RF Link Budget:	+108 dB	VCC:	2.1V – 3.6V
Network Speed:	250 kbps	RX Current:	37 mA
RF Channels:	16	TX Current:	200 mA
Software:	EmberZNet PRO Stack	Sleep Current:	1 uA
Network:	Mesh		

Cortex-M3 processor
192 kB Flash; 12 kB SRAM
SPI Master / Slave, TWI and UART
Timers, Serial Wire / JTAG Interface
5-channel, 14-bit ADC
Up to 23 GPIO Pins
Integrated PCB Antenna

Electrical Requirements

ABSOLUTE MAXIMUM RATINGS

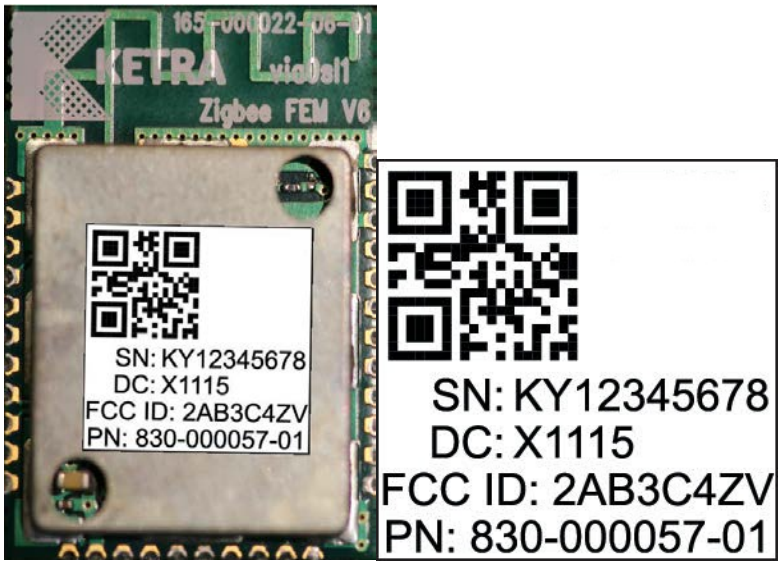
Description	Ketra ZigBee Module		Unit
	Min	Max	
Power Supply Voltage (V_{DD})	-0.3	3.6	VDC
Voltage on any I/O Line	-0.3	V_{DD} + 0.3	VDC
Storage Temperature Range	-40	125	°C
Reflow Soldering Temperature	–	260	°C

Note: *Exceeding the maximum ratings may cause permanent damage to the module or devices.*

RECOMMENDED OPERATING CONDITIONS

Description	Ketra ZigBee Module			Unit
	Min	Typ	Max	
Power Supply Voltage (V_{DD})	2.1	3.3	3.6	VDC
Input Frequency	2405	–	2480	MHz
Ambient Temperature Range	-40	25	85	°C

Device Label



FCC ID

FCC ID: 2AB3C4ZV

Operational Description

The EM358x radio receiver is a low-IF, super-heterodyne receiver. The architecture has been chosen to optimize co-existence with other devices in the 2.4 GHz band (namely Wi-Fi and Bluetooth), and to minimize power consumption. The receiver uses differential signal paths to reduce sensitivity to noise interference. Following RF amplification, the signal is downconverted by an image-rejecting mixer, filtered, and then digitized by an ADC.

The digital section of the receiver uses a coherent demodulator to generate symbols for the hardware-based MAC. The digital receiver also contains the analog radio calibration routines, and controls the gain within the receiver path.

The radio transmitter uses an efficient architecture in which the data stream directly modulates the VCO frequency. An integrated PA provides the output power. Digital logic controls Tx path and output power calibration. If the EM358x is to be used with an external PA, use the TX_ACTIVE or nTX_ACTIVE signal to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24 MHz crystal with its loading capacitors is required to establish the PLL local oscillator signal.

The MAC interfaces the on-chip RAM to the Rx and Tx baseband modules. The MAC provides hardware-based IEEE 802.15.4-2003 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchronization effort of the Ember software and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4-2003 CSMA-CA algorithm.

The EM358x integrates hardware support for a packet trace module, which allows robust packet-based debug. This element is a critical component of Ember Desktop, the Ember development environment, and provides advanced network debug capability when used with the Ember Debug Adapter (ISA3).

The EM358x integrates an ARM® CortexTM-M3 microprocessor, revision r1p1. This industry-leading core provides 32-bit performance and is very power-efficient. It has excellent code density using the ARM® Thumb-2 instruction set. The processor can be operated at 12 or 24 MHz when using the high-frequency crystal oscillator, or at 6 MHz or 12 MHz when using the high-frequency internal RC oscillator.

EM358x parts have either 256 or 512 kB of flash memory and either 32 or 64 kB of RAM on-chip, and the ARM configurable memory protection unit (MPU).

The EM358x implements both the ARM Serial Wire and JTAG debug interfaces. These interfaces provide real time, non-intrusive programming and debugging capabilities. Serial Wire and JTAG provide the same functionality, but are mutually exclusive. The Serial Wire interface uses two pins; the JTAG interface uses five. Serial Wire is preferred, since it uses fewer pins.

The EM358x contains the ARM® Embedded Trace Macrocell (ETM) to provide advanced real time software debugging features for complex systems.

The EM358x contains 24 GPIO pins shared with other peripheral or alternate functions. Because of flexible routing within the EM358x, external devices can use the alternate functions on a variety of different GPIOs. The integrated serial controller SC1 can be configured for SPI (master or slave), TWI (master-only), or UART operation, and the serial controller SC2 can be configured for SPI (master or slave) or TWI (master-only) operation.

The EM358x has a general purpose ADC which can sample analog signals from six GPIO pins in single-ended or differential modes. It can also sample the 1.8 V regulated supply VDD_PADSA, the voltage reference VREF, and GND. The ADC has one voltage range: 0 V to 1.2 V (normal). The ADC has a DMA mode to capture samples and automatically transfer them into RAM. The integrated voltage reference for the ADC, VREF, can be made available to external circuitry. An external voltage reference can also be driven into the ADC. The regulator input voltage, VDD_PADS, cannot be measured using the general purpose ADC, but it can be measured through Ember software.

The EM358x contains four oscillators: a high-frequency 24 MHz external crystal oscillator, a high-frequency 12 MHz internal RC oscillator, an optional low-frequency 32.768 kHz external crystal oscillator, and a low-frequency 10 kHz internal RC oscillator.

The EM358x has an ultra low power, deep sleep state with a choice of clocking modes. The sleep timer can be clocked with either the external 32.768 kHz crystal oscillator or with a 1 kHz clock derived from the internal 10 kHz RC oscillator. Alternatively, all clocks can be disabled for the lowest power mode. In the lowest power mode, only external events on GPIO pins will wake up the chip. The EM358x has a fast startup time (typically 110 µs) from deep sleep to the execution of the first ARM® Cortex™-M3 instruction.

The EM358x contains three power domains. The always-on high voltage supply powers the GPIO pads and critical chip functions. Regulated low voltage supplies power the rest of the chip. The low voltage supplies are disabled during deep sleep to reduce power consumption. Integrated voltage regulators generate regulated 1.25 V and 1.8 V voltages from an unregulated supply voltage. The 1.8 V regulator output is decoupled and routed externally to supply analog blocks, RAM, and flash memories. The 1.25 V regulator output is decoupled externally and supplies the core logic.

The RF6525 integrates a complete solution in a single Front End Module (FEM) for ZigBee® applications in the 2.4GHz to 2.5GHz band. This FEM integrates the PA plus harmonic filter in the transmit path and the LNA with bypass mode in the receive side. It also integrates a diversity switch and provides balanced input and output signals for both the TX and RX paths respectively.

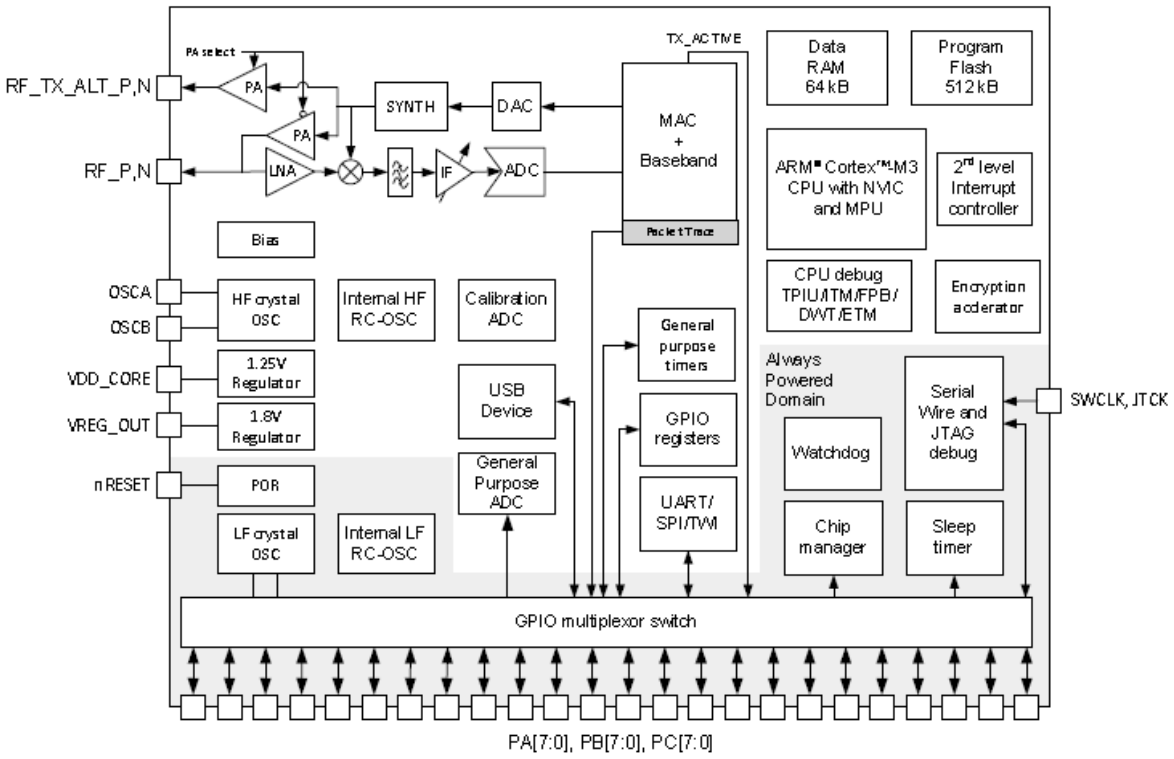


Figure 1 EM358x Block Diagram

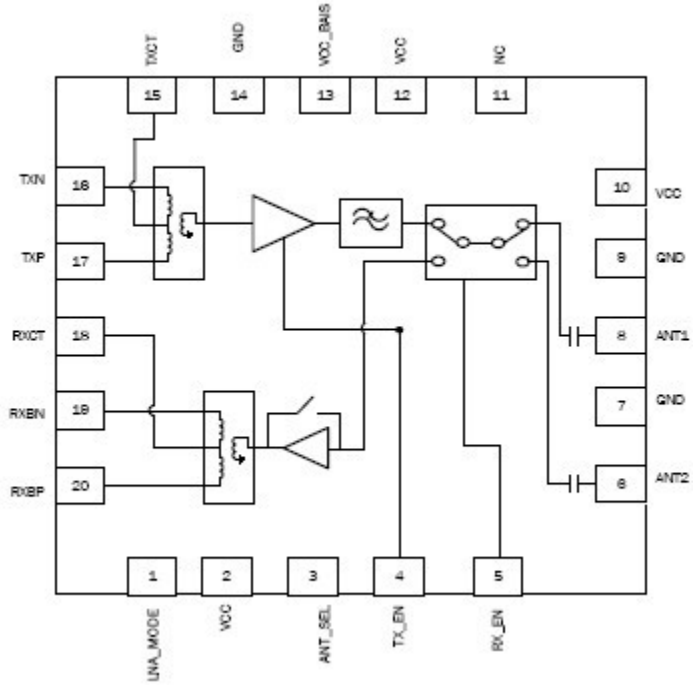


Figure 2 RF6525 Block Diagram

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