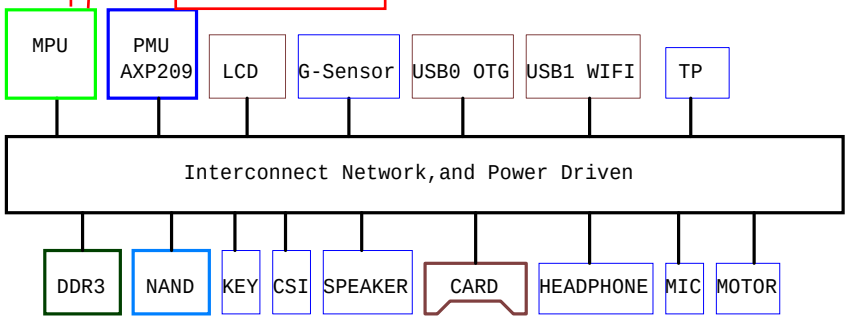
COVER

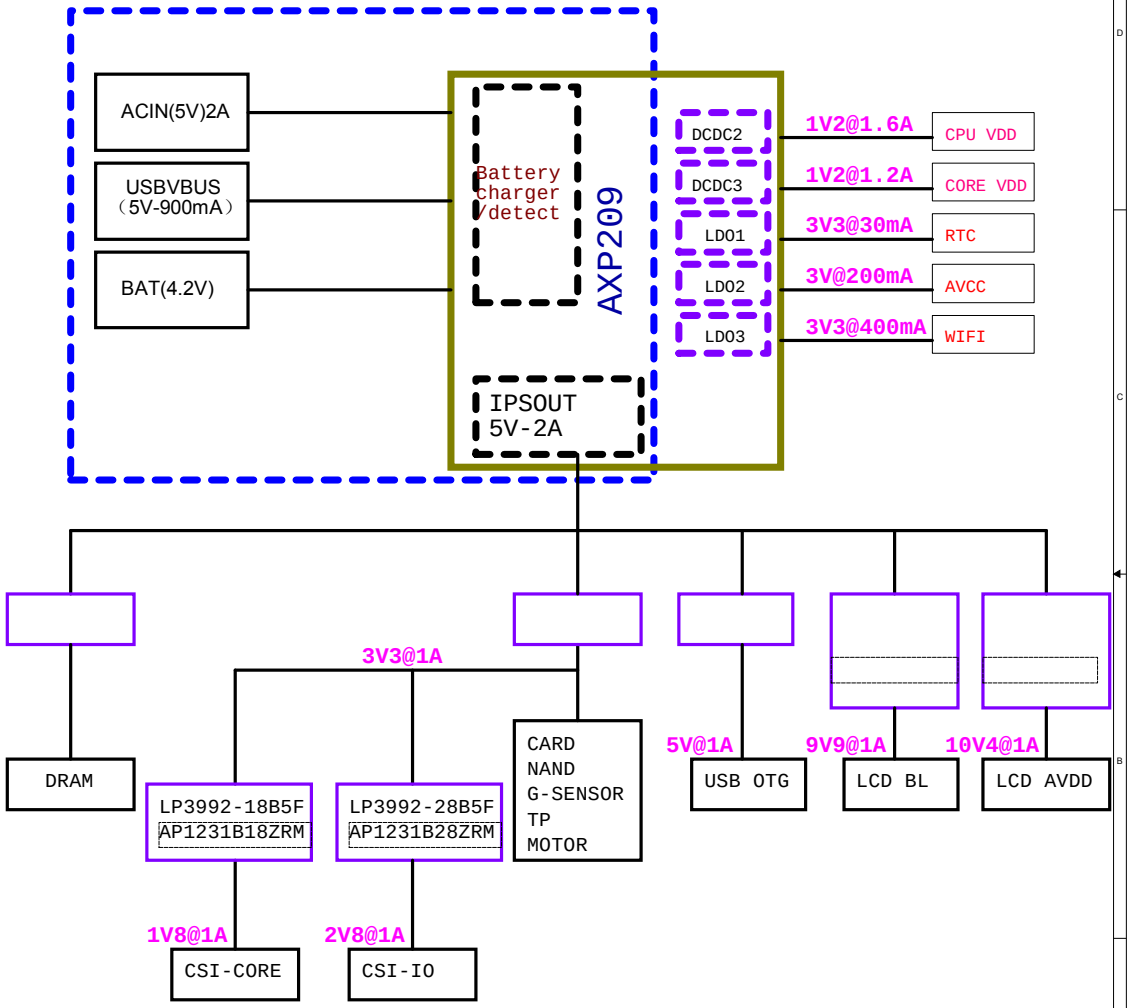
X1=24MHz

X2=32.768KHz

BLOCK



POWER TREE



GPIO ASSIGNMENT

CPU	Define	Function
PB0	TWI0_SCK	TWI0
PB1	TWI0_SDA	
PB2	PWM0	LCD
PB3	GPIO-OUT	TP-WAKE-RST
PB4	NC	
PB10	GPIO-OUT	CSI-STY
PB15	TWI1_SCK	TWI1
PB16	TWI1_SDA	
PB17	TWI2_SCK	TWI2
PB18	TWI2_SDA	
PG0	INPUT	SD0-DET-N
PG1	GPIO-IN	USB0-VBUSDET
PG2	GPIO-IN	USB0-IDDET
PG3	UART-TX	UART-TX
PG4	UART-RX	UART-RX
PG9	GPIO-OUT	MT-EN
PG10	GPIO-OUT	PA-SHDN
PG11	EINT	TP-INT
PG12	GPIO-OUT	USB0-DRV
PMU	**Define**	**Function**
GPIO0	GPIO-OUT	LCD-PWR
GPIO1	GPIO-OUT	LCD-BL-EN
GPIO2	GPIO-OUT	CSI-PWR-EN
GPIO3	GPIO-OUT	CSI-RST

REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
APP3_PAD_DDR3_V1_20	version 1.20		CPL		

Title	APP3_PAD_DDR3	
Size A3	Document Name COVER	Rev
Date:	Sheet 1 of 6	

2412-2462MHz, ANT. Gain:0dBi