SecureJet Intelligent Appliance V8 Design

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Revision	Date of Document	Pages Affected / Remarks
	18/03/13	draft release

Acronyms used

EOL	End of Line Testing or Board level testing
EMI/EMC	Electromagnetic Interference / Compatibility
ESD	Electro-Static Discharge
UUT	Unit under Test
LCD	Liquid Crystal Display
RGB	Red Green Blue (refers to LCD video signals)
CPU	Center Processing Units
LVDS	Low-voltage differential signaling

Table of Contents

1 Introduction

This document describes the hardware design for the SecureJet Intelligent Appliance v8.0, hereby refer to as SIA.

SIA consist of 2 components, the CPU unit (refer to as CPU) and the Screen Display unit (refer to as Display). As shown below.

Figure 1

SIA CPU unit is compact low power embedded box with 32bit ARM11 micro-processor running Linux operating system, below is the specs of CPU unit.

- CPU: 32bit SSD1938 Solomon Systech, 800MHz ARM11 processor
- Flash Memory: 2GB Nand Flash
- RAM: DDR2 256MB
- USB Host 2.0 x2
- USB Client 2.0 x1
- LAN Port RJ45 x2 (built-in Ethernet switch)
- Proprietary I/O port
- Built in Hardware RTC
- Built in micro SD slot
- Weight : TBD
- Casing : Aluminum extrusion
- Power consumption : < 3 W

Below is the specification of the Display unit

- LCD panel : 7” TFT 800 x 480 pixel, 24bit RGB LCD display
- Touch panel : 4 wires resistive touch panel 7”
- Speaker: 8ohm 250mW
- USB Host 2.0 x2
- Video signaling : LVDS R,G,B, clock
- Weight:
- Casing: Plastics
- Power consumption : < 3W

2 CPU unit design

2.1 PCB assembly

This is the top PCBA view of the main CPU Board, top and bottom view.

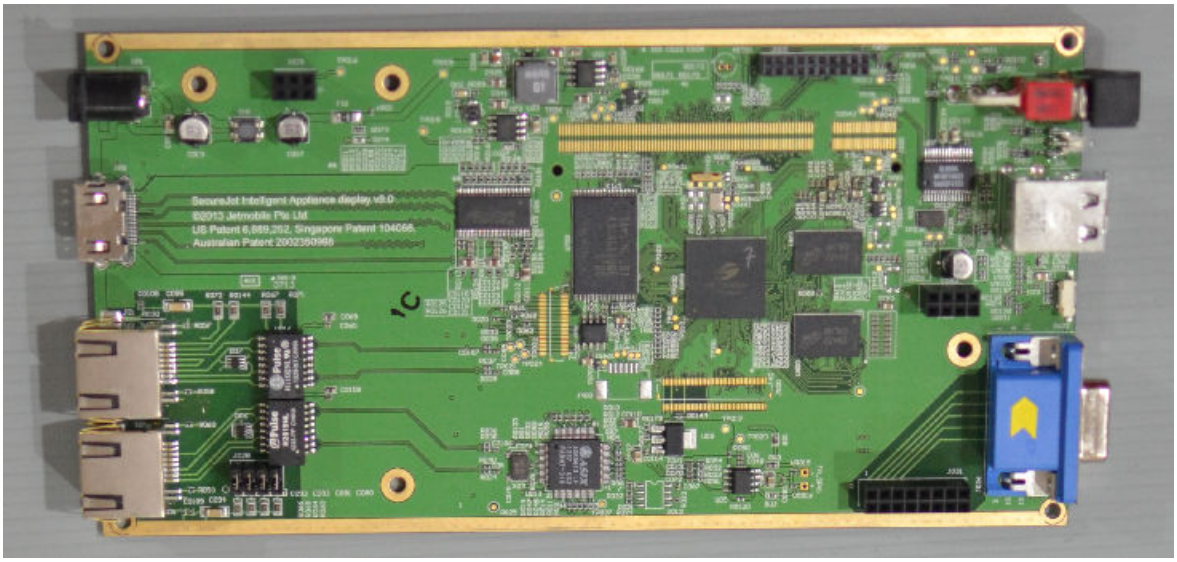


Figure 2 – PCBA Top view of CPU unit

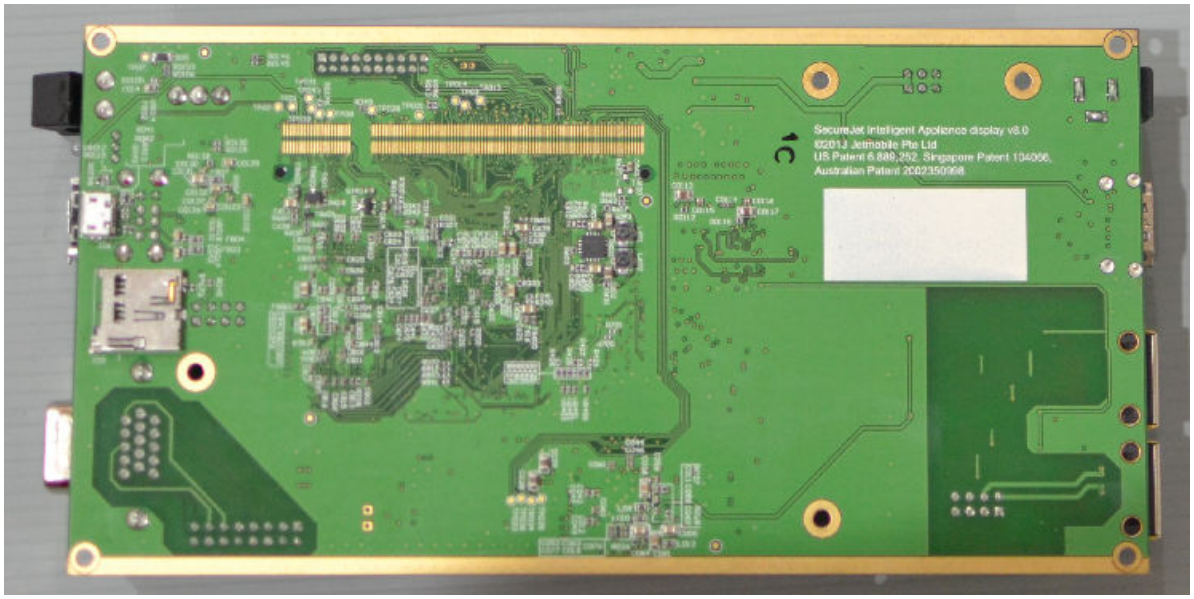


Figure 3- PCBA Bottom view of CPU unit

2.2 PCB connectors

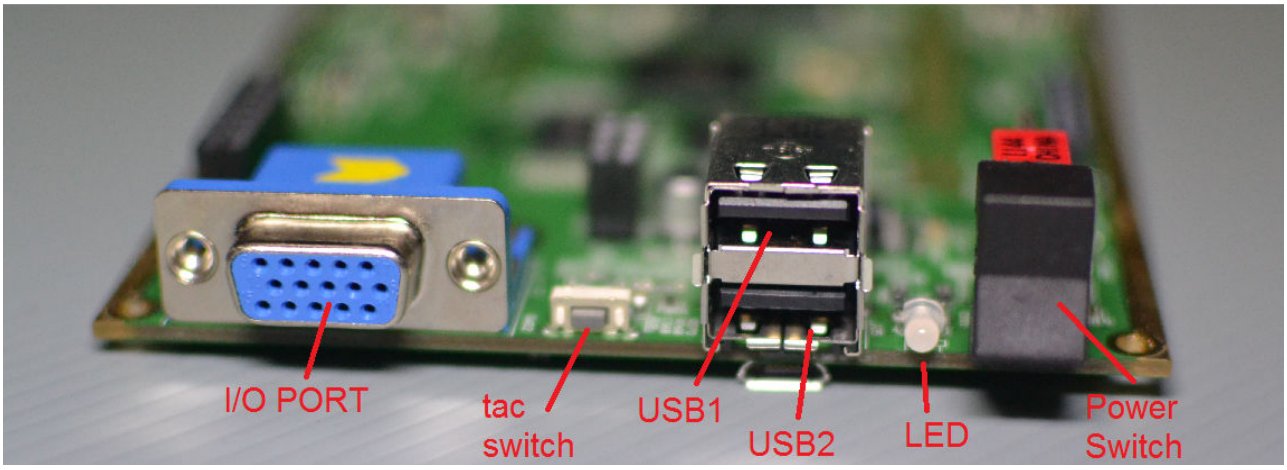


Figure 4 – PCBA side connectors Side 1

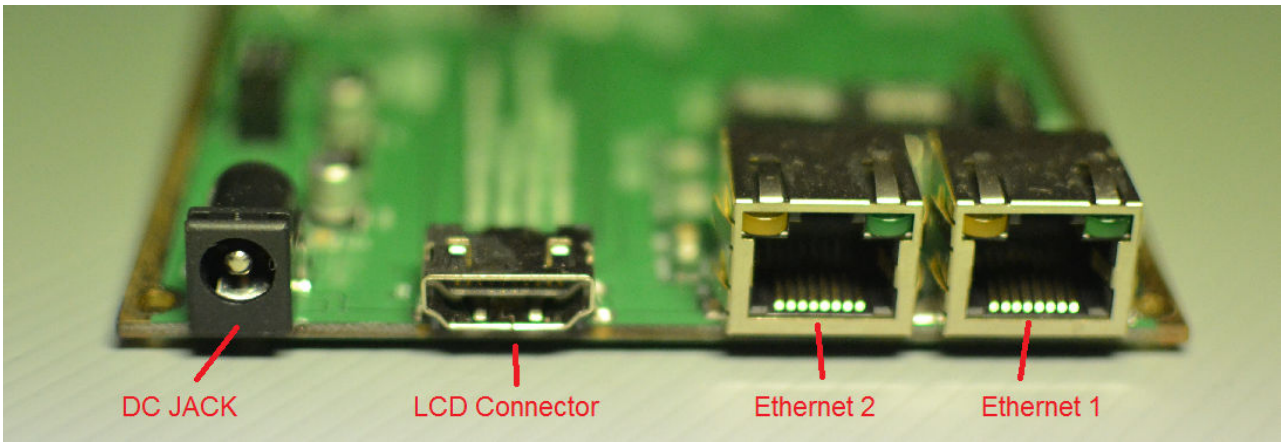


Figure 5 – PCBA side connectors Side 2

2.3 With casings

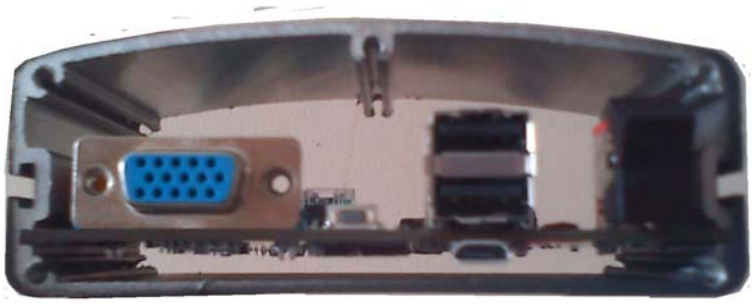


Figure 6 – PCBA CPU unit in enclosure

Figure 7 – CPU unit in enclosure

2.4 Functional blocks on PCBA

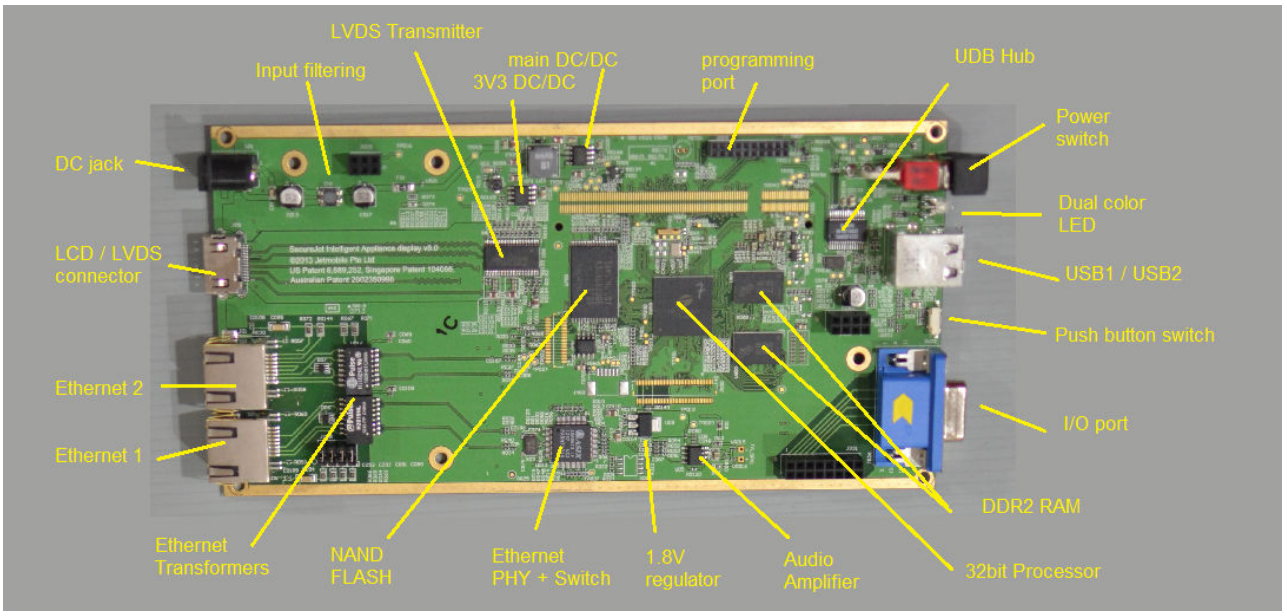


Figure 8 – Functional blocks on top view PCBA of CPU Unit

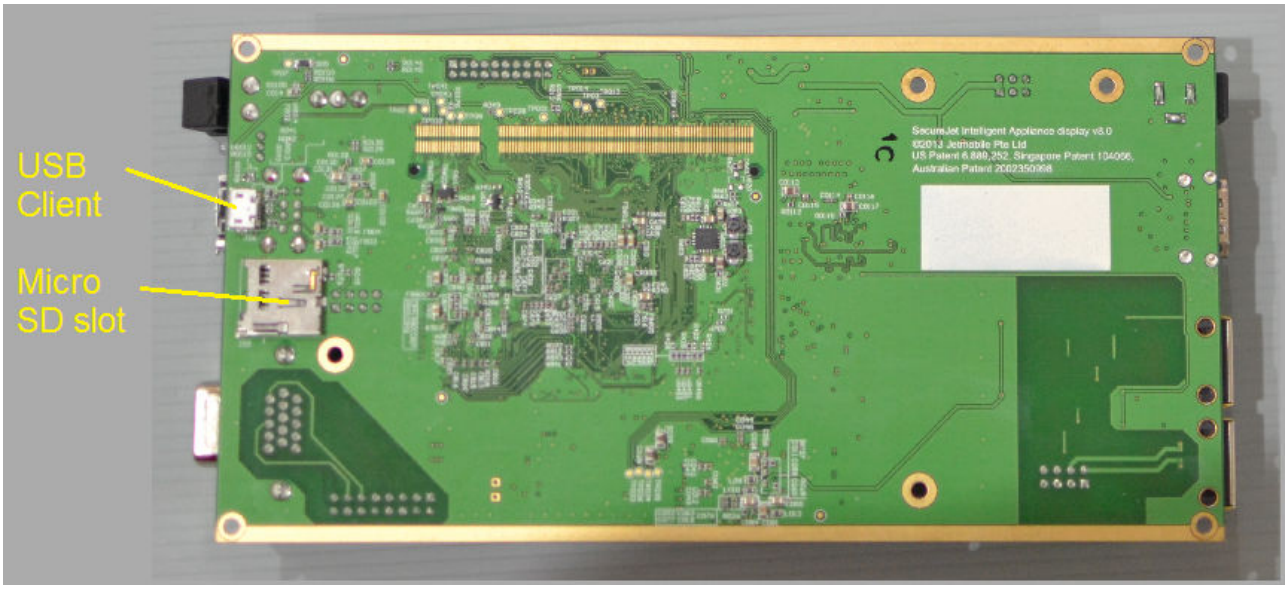


Figure 9 – Functional blocks of bottom view PCBA of CPU unit

2.5 Block Diagram

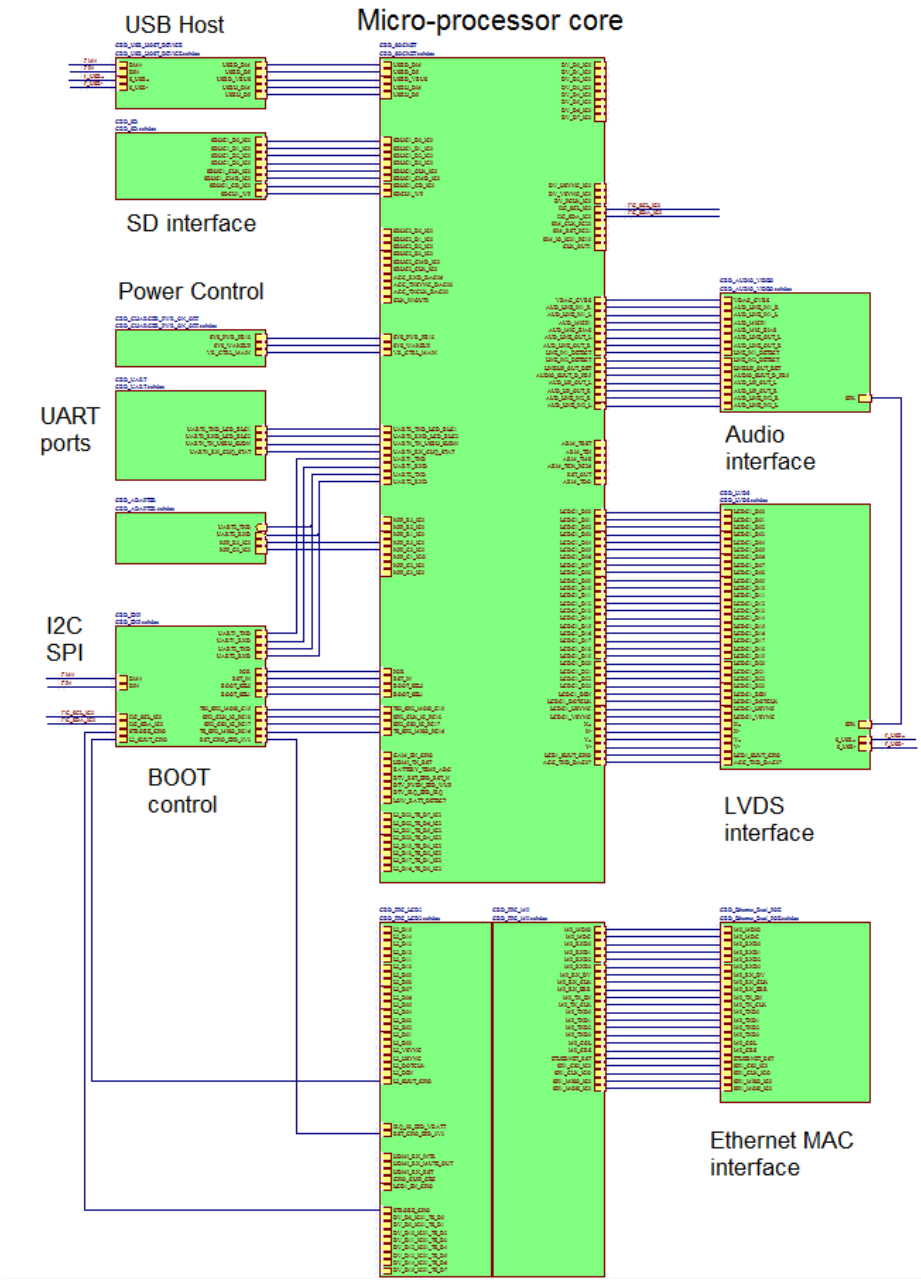


Figure 10

2.6 Schematics

Schematics with descriptions

2.6.1 Grounding isolation

To minimized EMC/EMI, Global chassis grounding concept is used in the design for the isolation between the chassis ground and the internal ground. A ground ring is used as shown below for continuous contract with aluminum casing. This design will also minimized the potential ESD damaged to sensitive component in the center of the board such as microprocessor and memory chips.

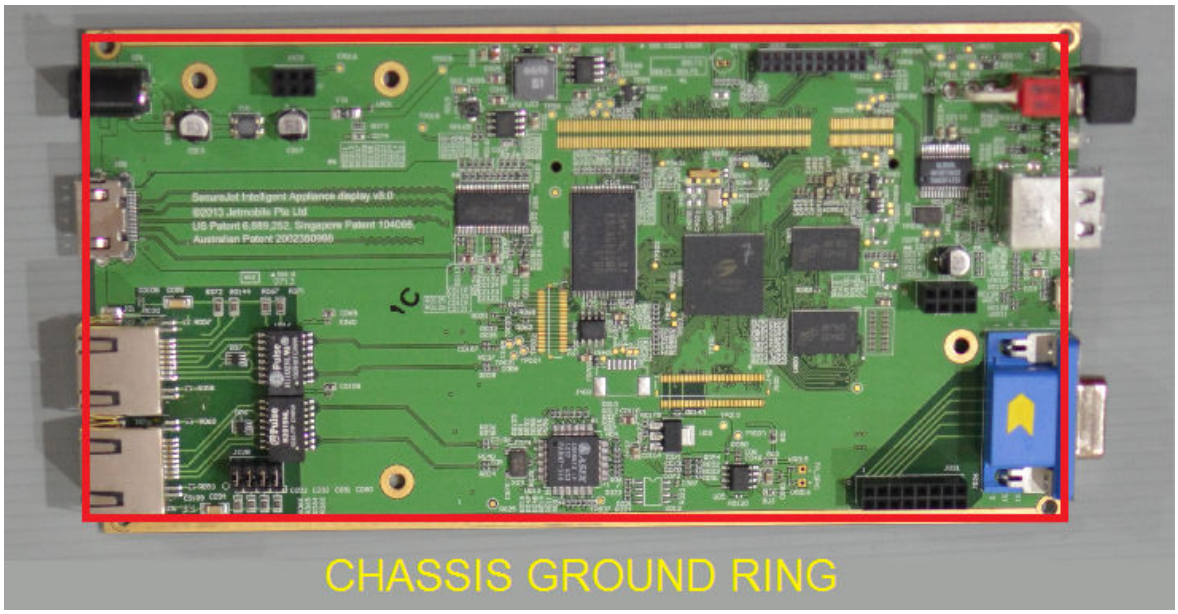


Figure 11 – Chassis grounding isolation

2.6.2 Power regulator input filtering circuit

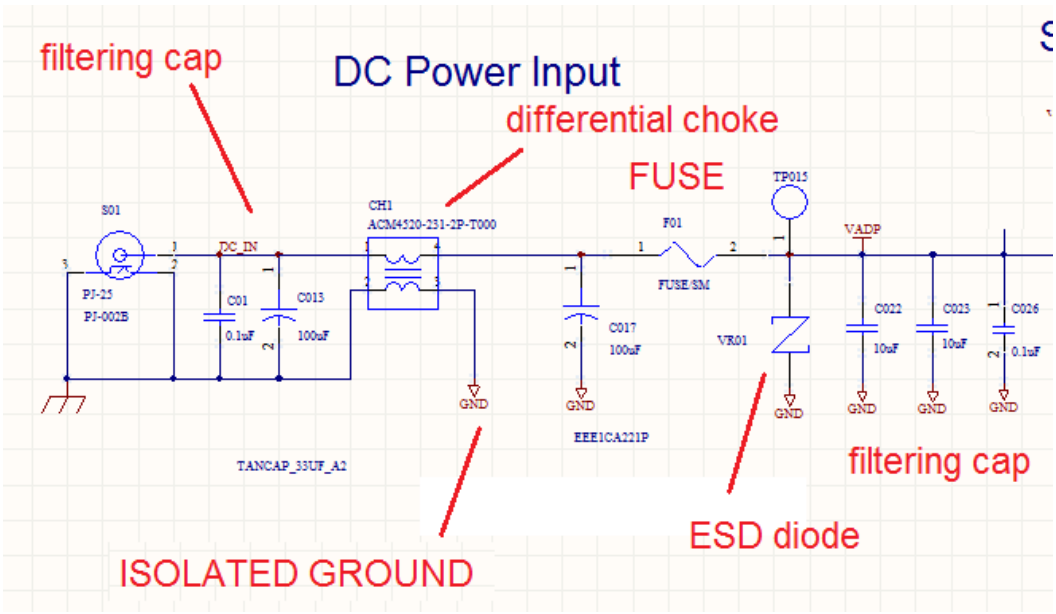


Figure 12 – Electronic circuitry diagram of Input filtering circuit

Input circuit consist of differential inductor / choke (CH1) and capacitor for EMC/EMI blocking, design to minimize the noise from the input DC/DC converters.

Fuse and ESD diodes also present for short circuit and ESD protection.

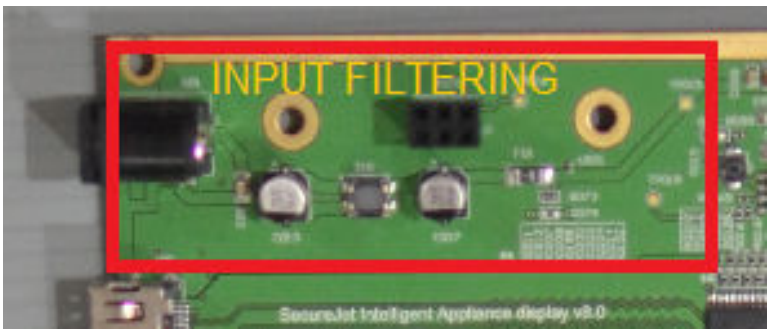


Figure 13 – PCBA showing Input filtering design

2.6.3 Main regulators and power circuits

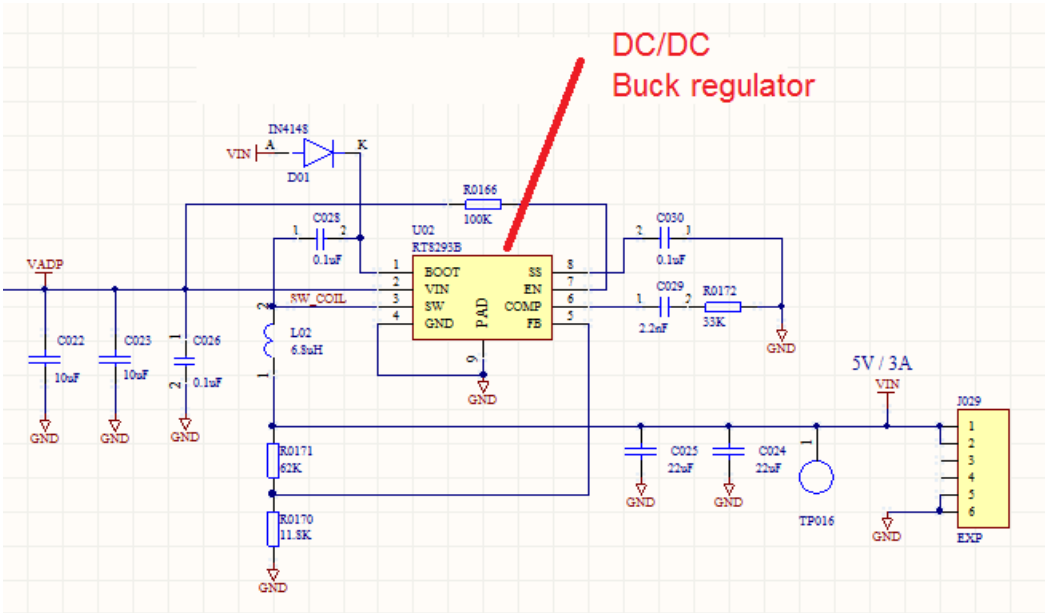


Figure 14 - Electronic circuitry diagram of main regulators and power circuits

The main component (U02) used is the 3A, 23V, 1.2MHz Synchronous Step-Down Converter, RT8293B from Richtek. Its function is to convert input voltage 9V – 12V to regulated 5V. It has fix operating frequency of 1.2MHz for easy filtering, it is operating > 95% efficiency, due to the over design, the regulator is operating well within the operating limits of voltage current and power. It is therefore running cool most of the time. The chip has a thermal pad below for heat-sink purpose.

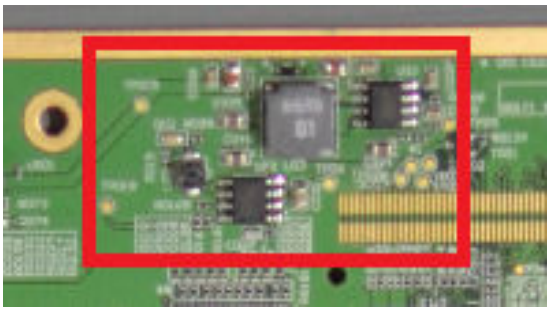


FIGURE 15 - PCBA showing main regulators and power circuits

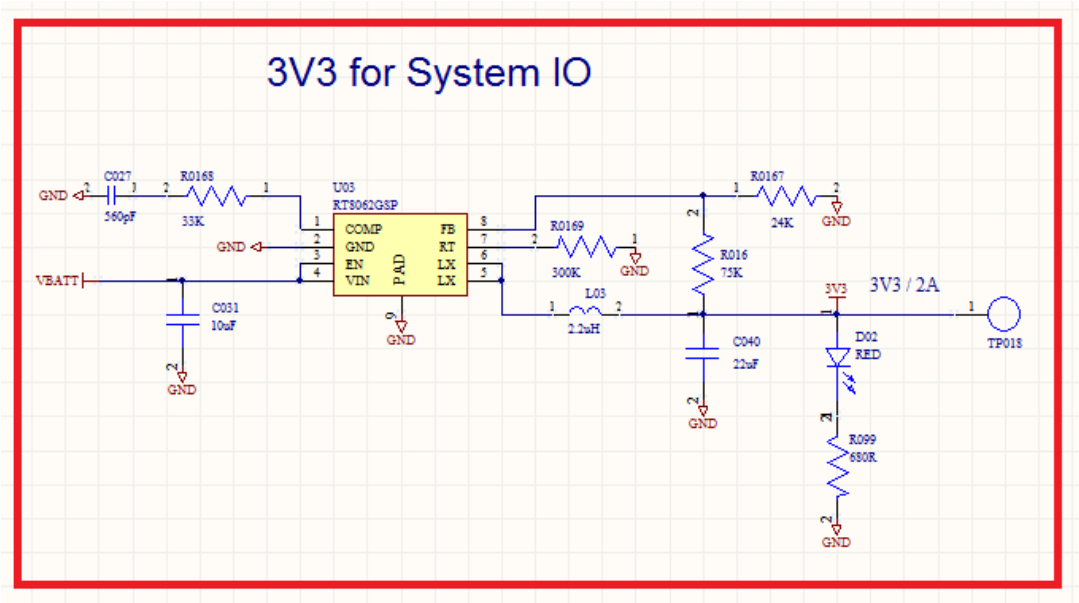


Figure 16 - Electronic circuitry diagram of internal system voltage

Internal system voltage is running at 3.3V, this voltage is provided by U03, RT8062. Its function is to convert 5V to 3.3V with efficiency of > 95%, frequency about 1 MHz

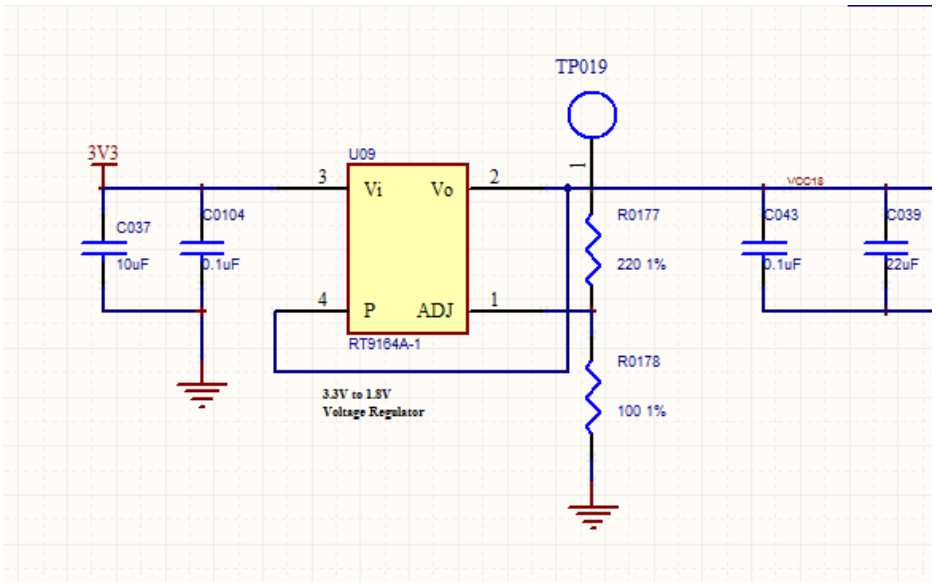


Figure 17 - Electronic circuitry diagram of Ethernet PHY

The Ethernet PHY chip is powered by 1.8V, LDO RT9164A is used for low noise performance.

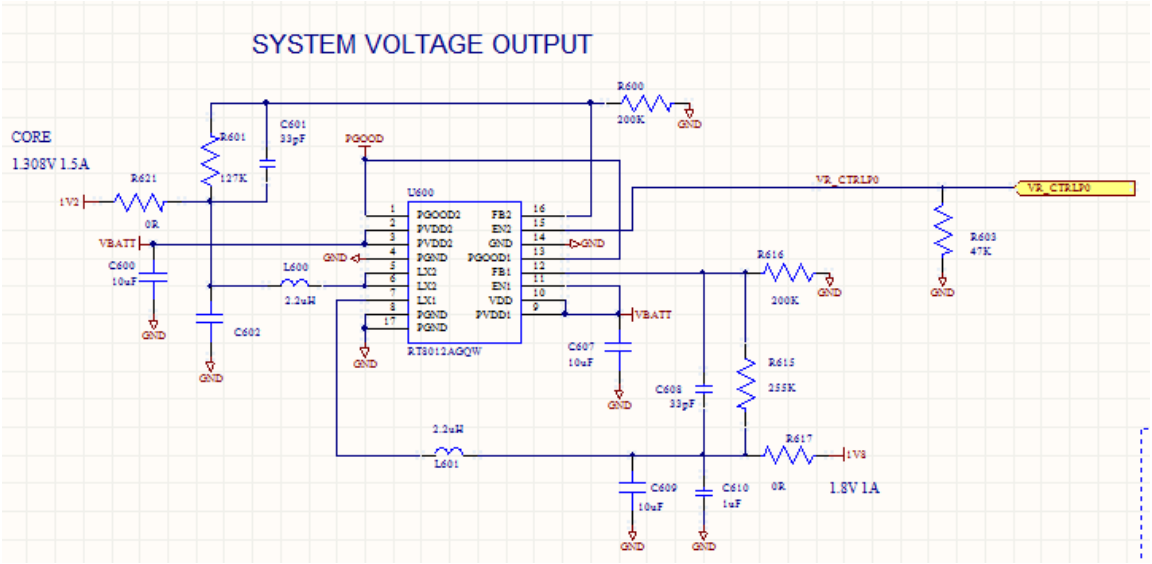


Figure 18 – Electronic circuitry diagram of system voltage output

The micro-processor core voltage is 1.2V and I/O is 1.8V, this is accomplished by U600, RT8012, a dual 1A/1.5A-1.2MHz Synchronous Step-Down Converters. It is a fix frequency (1.2 MHz) buck converter with > 95% efficiency and it is controlled by the CPU core to provide proper power sequencing needed= for proper operations of the CPU.

The rest of the regulators are LDO for analog (U612) and RTC (U610), which requires low noise and separate power lines

2.6.4 CPU Core schematics

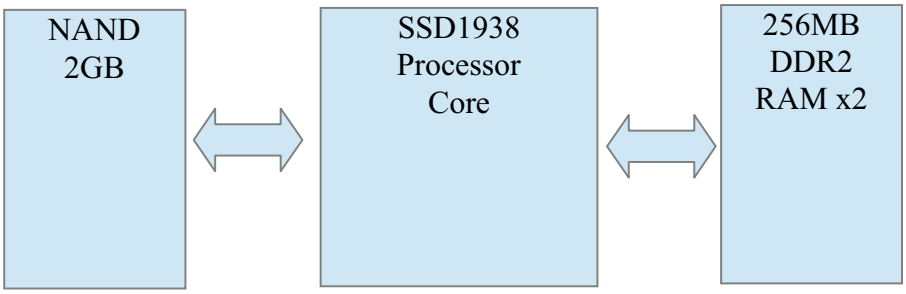


Figure 19 – Block diagram of CPU Core

Full 32 bit memory (2 DDR chips) are used for processing speed performance. For the NAND flash, it is an 8 bit interface MLC NAND flash for efficient program storage.

The CPU core takes its clock from n a 24 MHz crystal, which is internally scaled up to 800 MHz for running the processor. It also has a 32.768 kHz crystal for RTC time keeping.

Highest operating frequency is 800 MHz

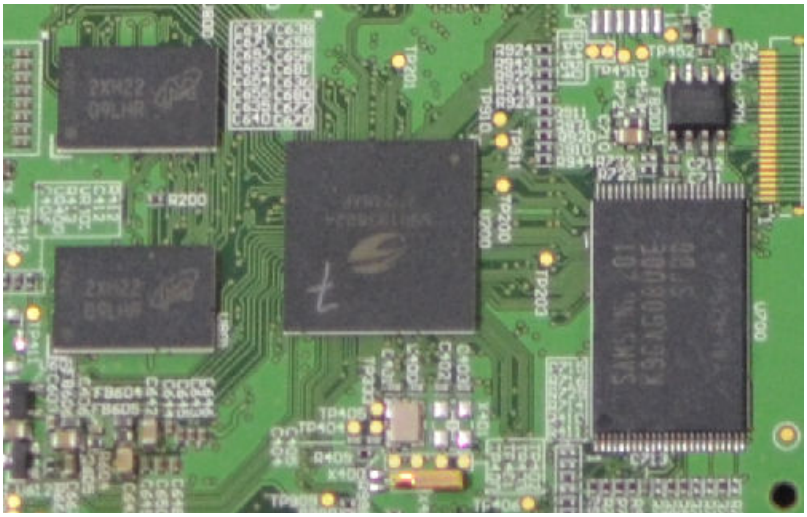


Figure 20 – PCBA showing CPU Core

2.6.5 USB hub

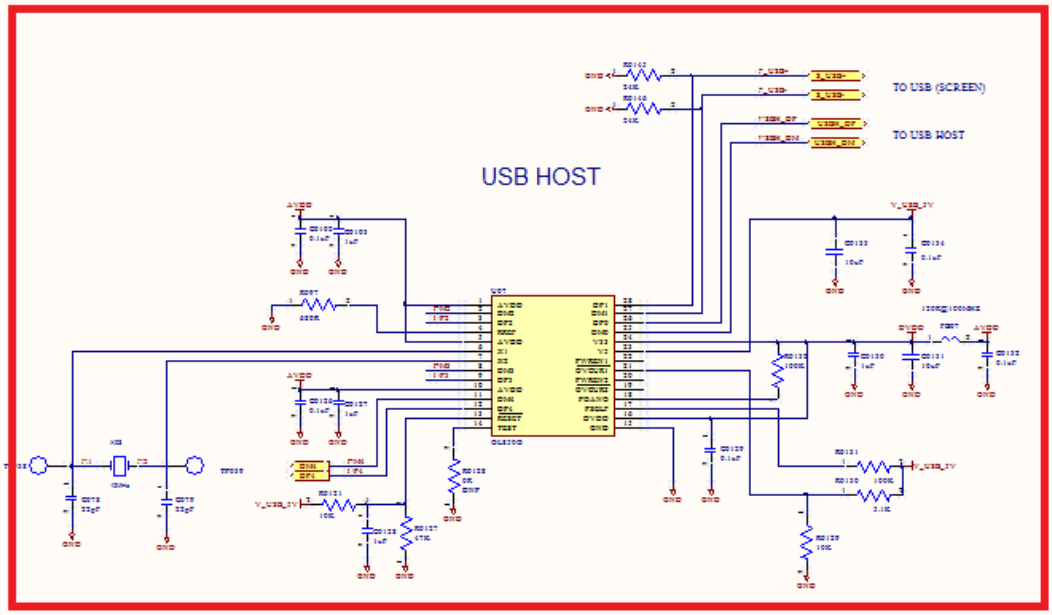


Figure 21 – Electronic circuitry diagram of USB Host

The USB hub used GL850 (U07) USB2.0 chip, it has 4 ports. Two are connected to external double deck connector as follows, one is connected to display units, one spare left for future expansion.

Mostly thumb drives, badge reader, and testing functions; not supporting mouse, keyboard, webcam etc.

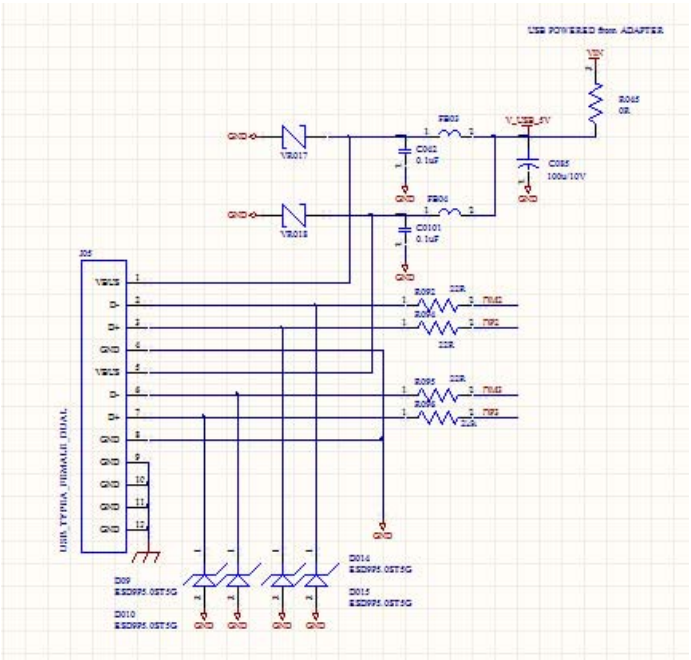


Figure 22 - Electronic circuitry diagram of USB port with ESD diodes for protection.

2.6.6 SD slot

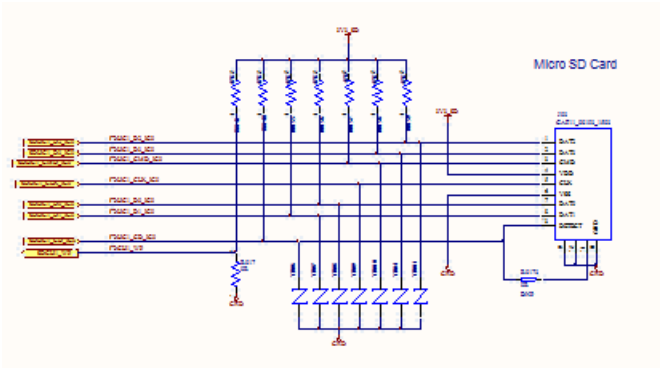


Figure 23 – Electronic circuitry of SD interface

A mini SD card slot is included on the PCB, the SD interface is controlled by built in circuitry in the chip. The SD is optional and concealed internal to the box and not accessible by end users

2.6.7 LVDS schematics for LCD

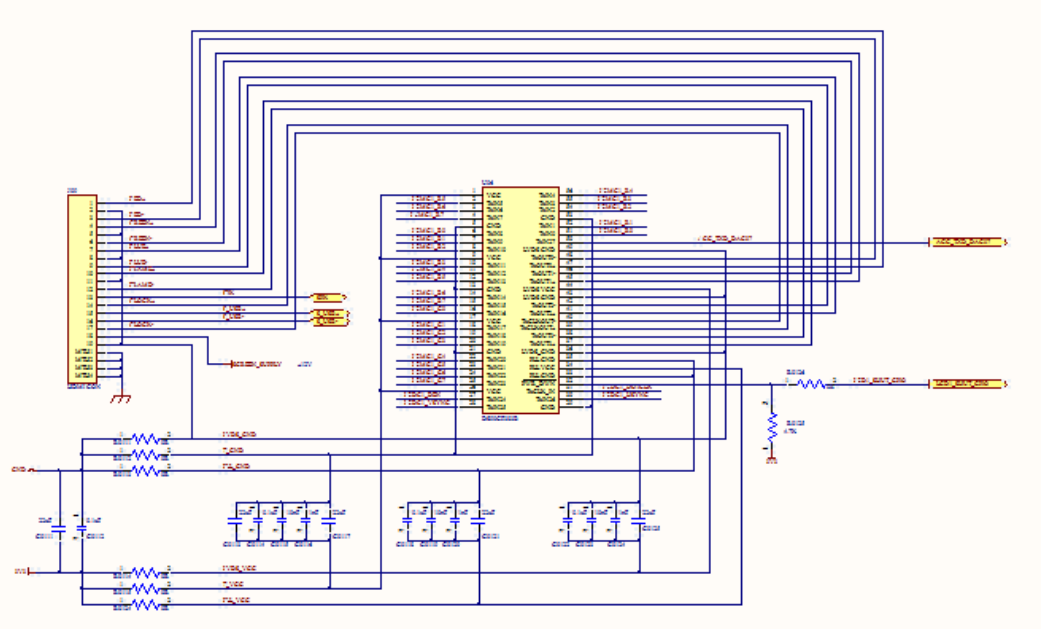
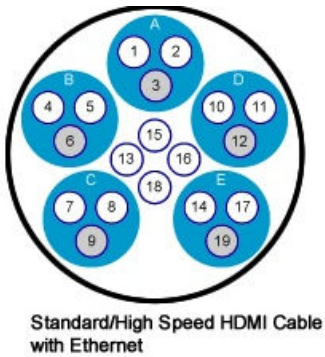


Figure 24

U06 is responsible for converting LCD RGB signal from the CPU to LVDS. LVDS is chosen for low cost and carrying video over a distance of 1-2m.

LVDS although running at high frequency (about 160Mhz), is very small in amplitude, the cable used to carry this signal is using HDMI double shield cables, the EMC emission is keep to minimum.



Standard/High Speed HDMI Cable with Ethernet

Figure 25

2.6.8 Ethernet interface

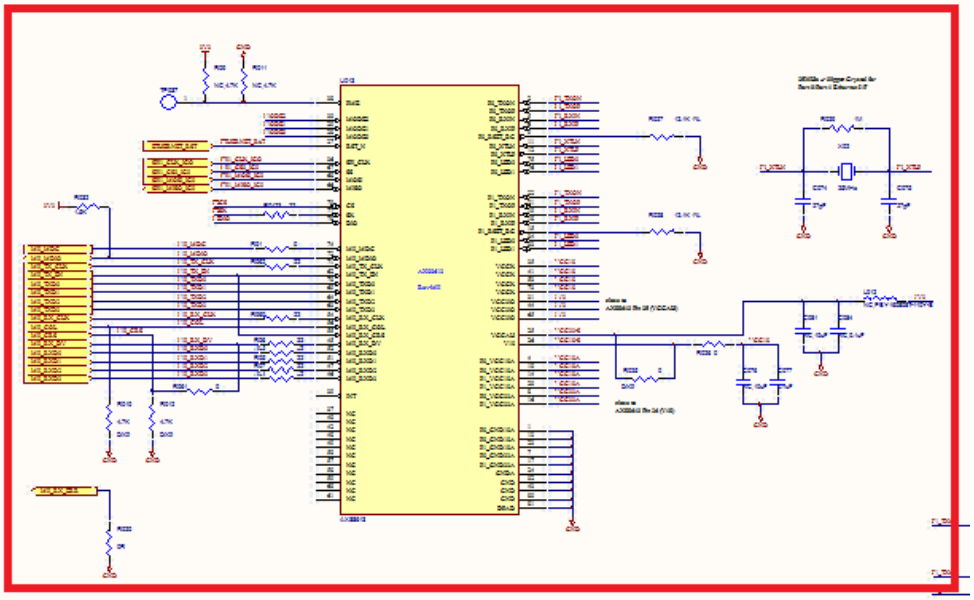


Figure 26

The SSD1938 processor has a built in MAC, therefore, only PHY chip (U013) from ASIX (AX88613) with built-in Ethernet switch is use to implement the Ethernet interfaces.

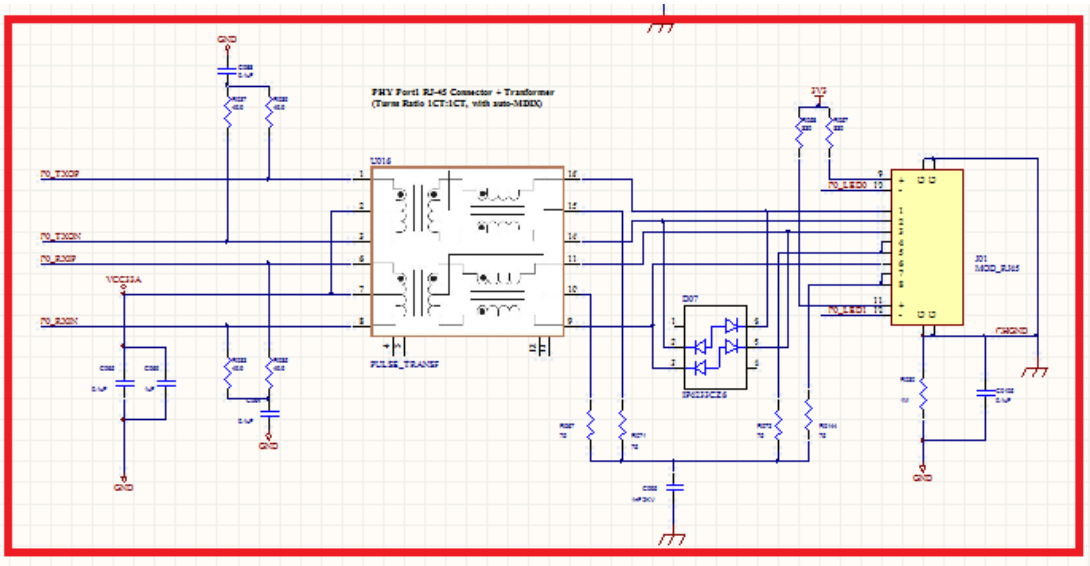


Figure 27

The Ethernet connector is ESD protected, isolated per recommended by the data-sheet to minimize the EMC with proper grounding requirements.

2.6.9 Audio amplifier

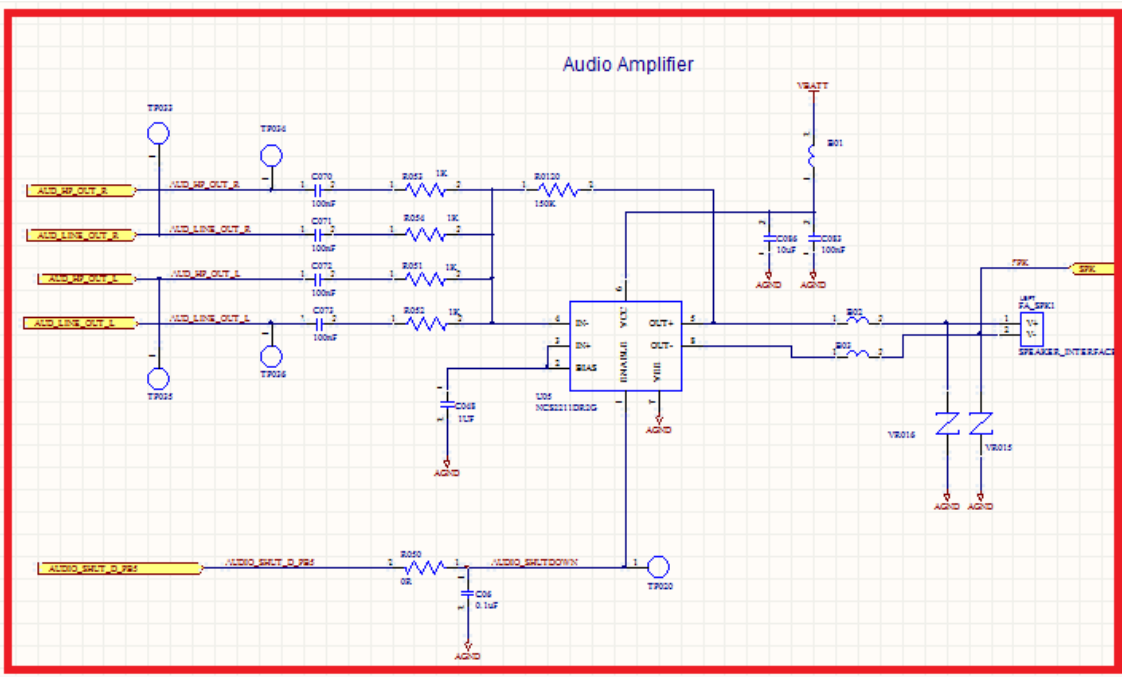


Figure 28 – Electronic circuitry diagram of Audio amplifier

The audio amplifier used is NCS2211DR2G (U05) from On semi. It is a class AB amplifier that drive the speaker directly in the remote display box 1.6m away.

Reason class AB type amplifier is used as opposed to popular PWM type is because of noise generation of PWM type chip, especially over long cables. Another reason is that only one wire is available for speaker lines, therefore only ½ bridge is used, not practical for PWM type amplifier to drive.

3 Screen Display Design

The screen proposes to the user list of documents to print. The user selects some documents which are then printed on the printer attached to the product.

Figure 29 – Screen Display Unit

Figure 30 – PCBA top view of Screen Display Unit

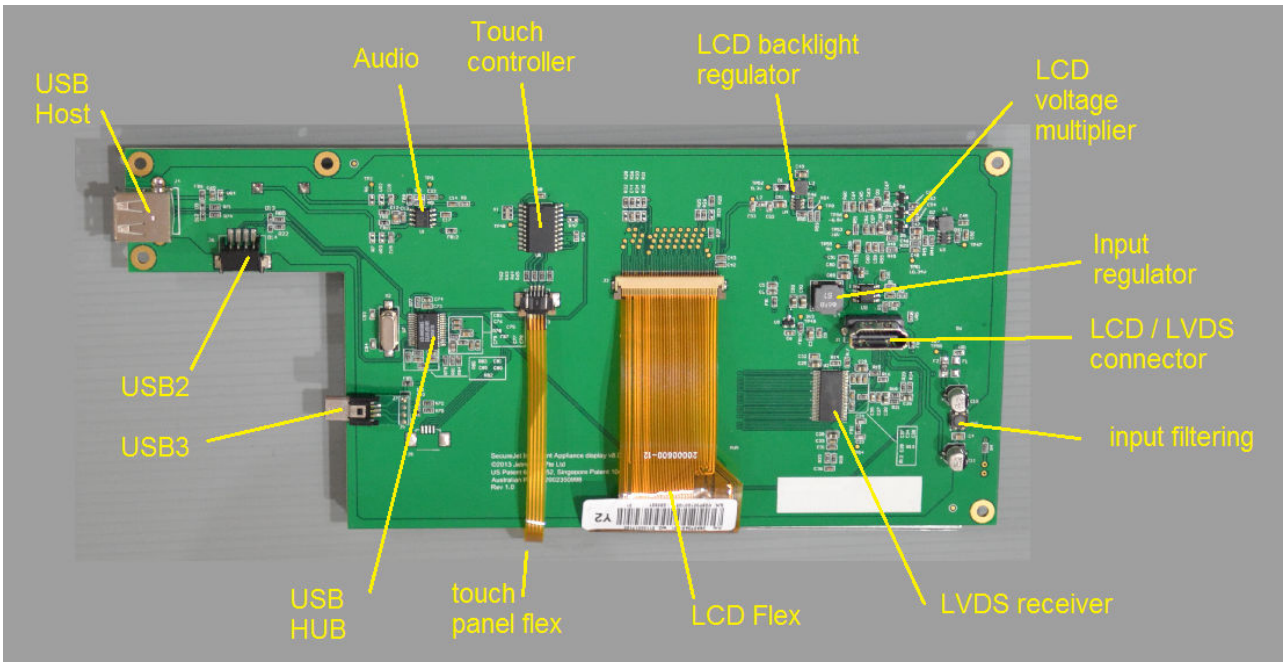


Figure 31 – PCBA Bottom view of Screen Display Unit

3.1 Schematics design – input filters and regulators

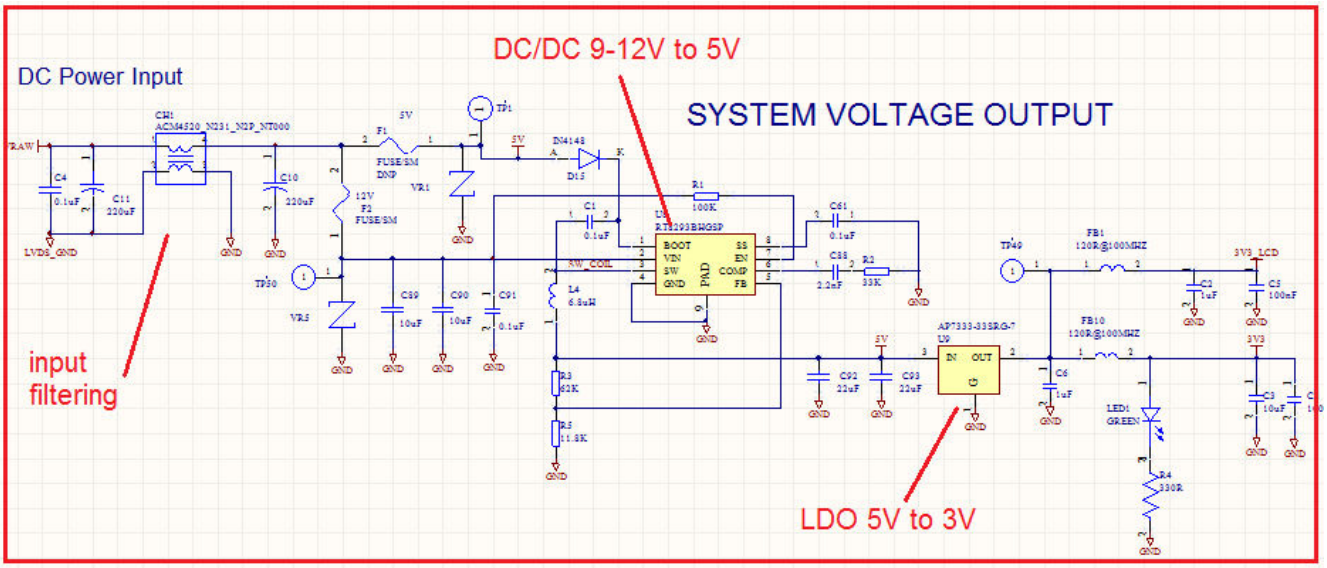


Figure 32

Similar to main CPU unit, the display unit also has the same power input filtering circuits. The same DC/DC chips is used (U8). To minimized EMC, LDO 5V to 3.3V (U9) is used instead of the more efficient DC/DC type. As the 3.3V will power the LVDS chip which is relatively sensitive to noise.

3.2 USB Hub

A 4 port USB 2.0 HUB (U7) similar to the main CPU board is used here for USB connector, USB touch panel, and internal USB connection for RFID boards etc.

The USB on the screen is made to plug a USB thumb drive with documents.

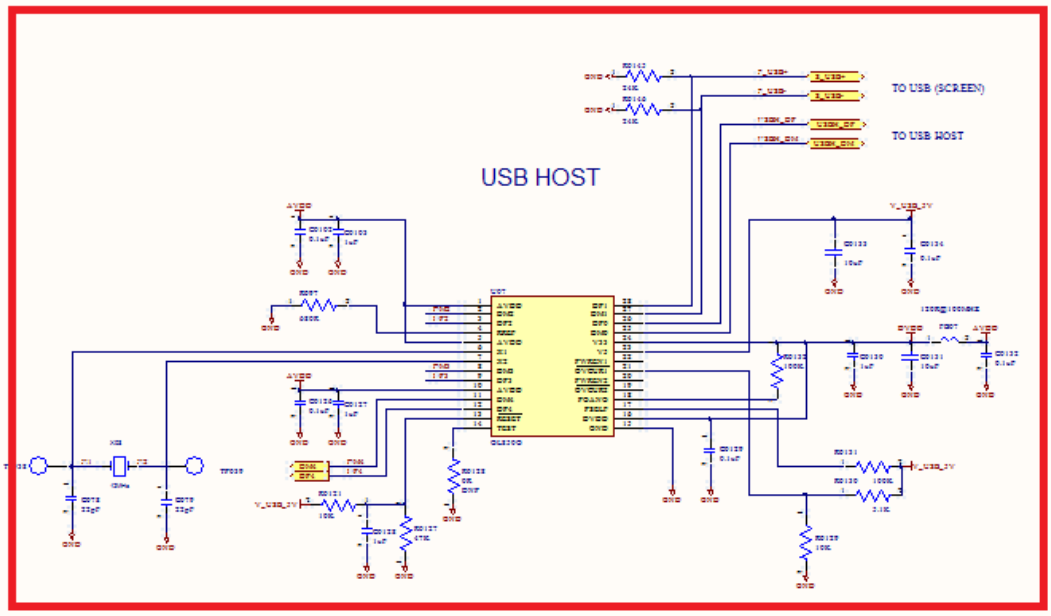


Figure 33

3.3 Voltage multipliers and back-light regulator

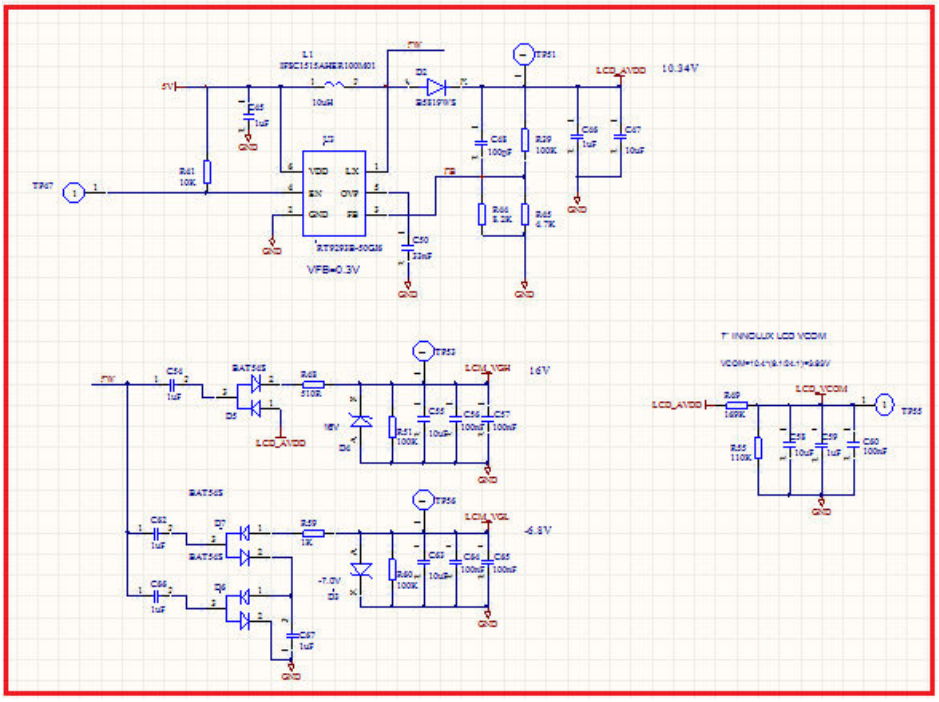


Figure 34

The voltage multiplier circuitry (U3) is responsible for generating voltages for the TFT LCD, includes, 16V, -7V, 10.5V and 4V.

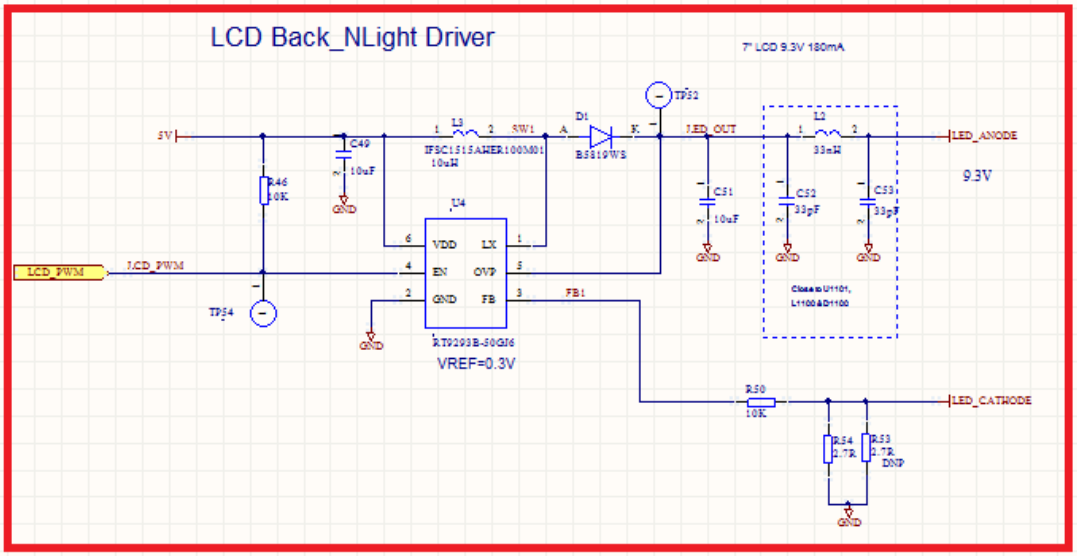


Figure 35

The LCD back-light is powered by U4 to achieved 9.5V 180mA for the LED backlight, it has a PWM input for controlling the screen brightness. The output has a “pi” filter for EMC reduction.

3.4 Touch controller

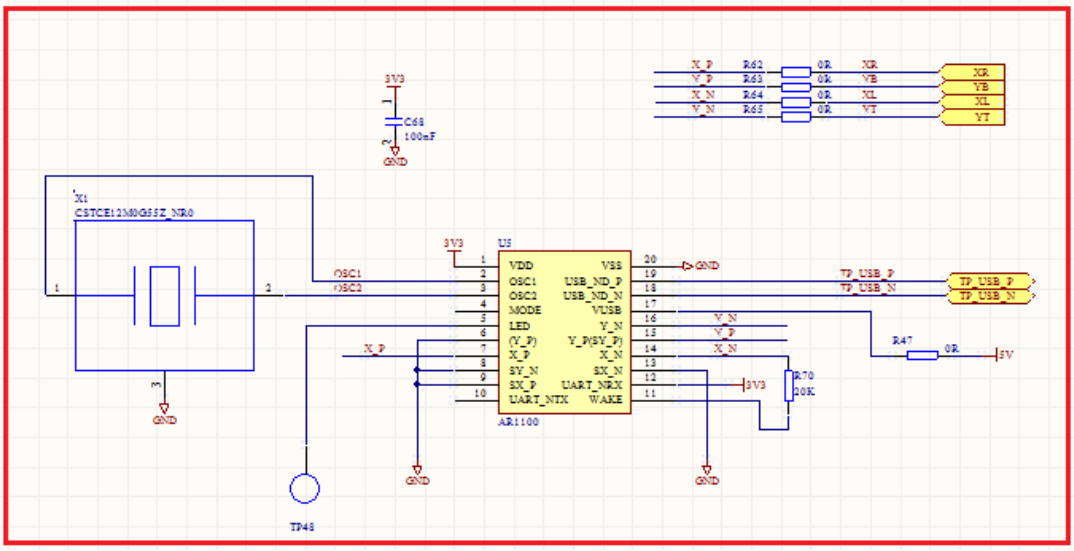


Figure 36

The touch controller is using an AR1100 chip to accomplish. It converts the 4 wires touch signals to USB signal for the main CPU to pick up and decode.

3.5 LVDS receiver

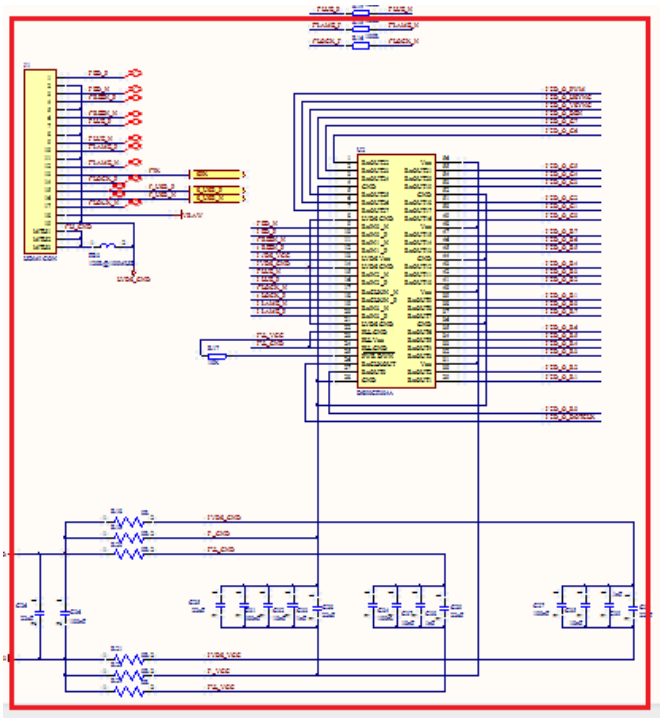


Figure 37

LVDS receiver is U2 (DS90CF384A) is converting the LVDS signals back to RGB signals for the TFT LCD.

3.6 LCD line filtering

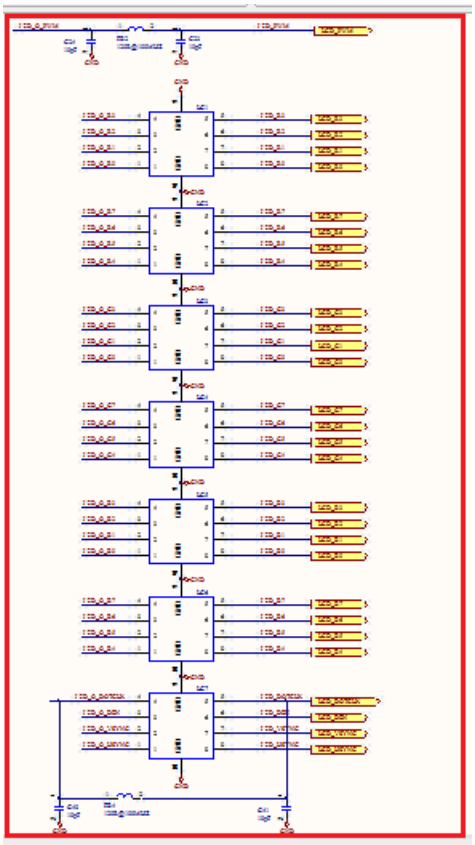
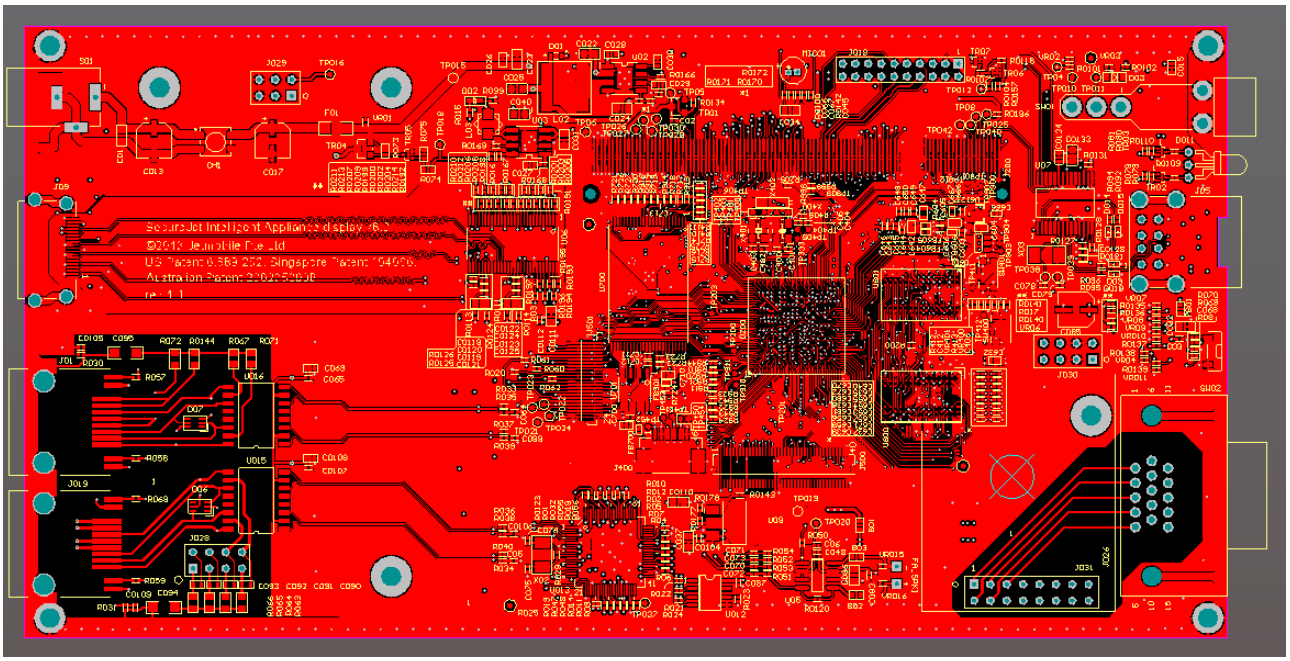


Figure 38

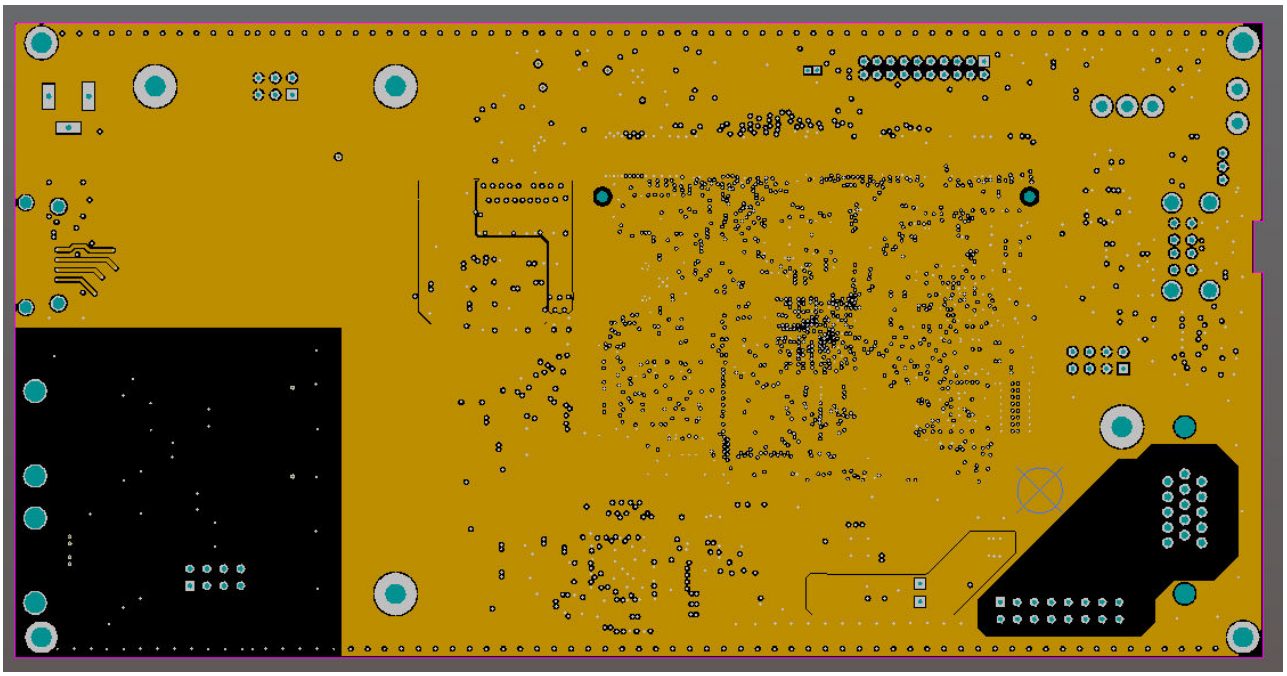
LCD signals are high speed and notorious for EMC emission, for this reason, all LCD signals are passing through a LCR filtering chip to reduce any high harmonic contents to minimized the EMC emission.

3.7 Appendix A – PCB Layouts

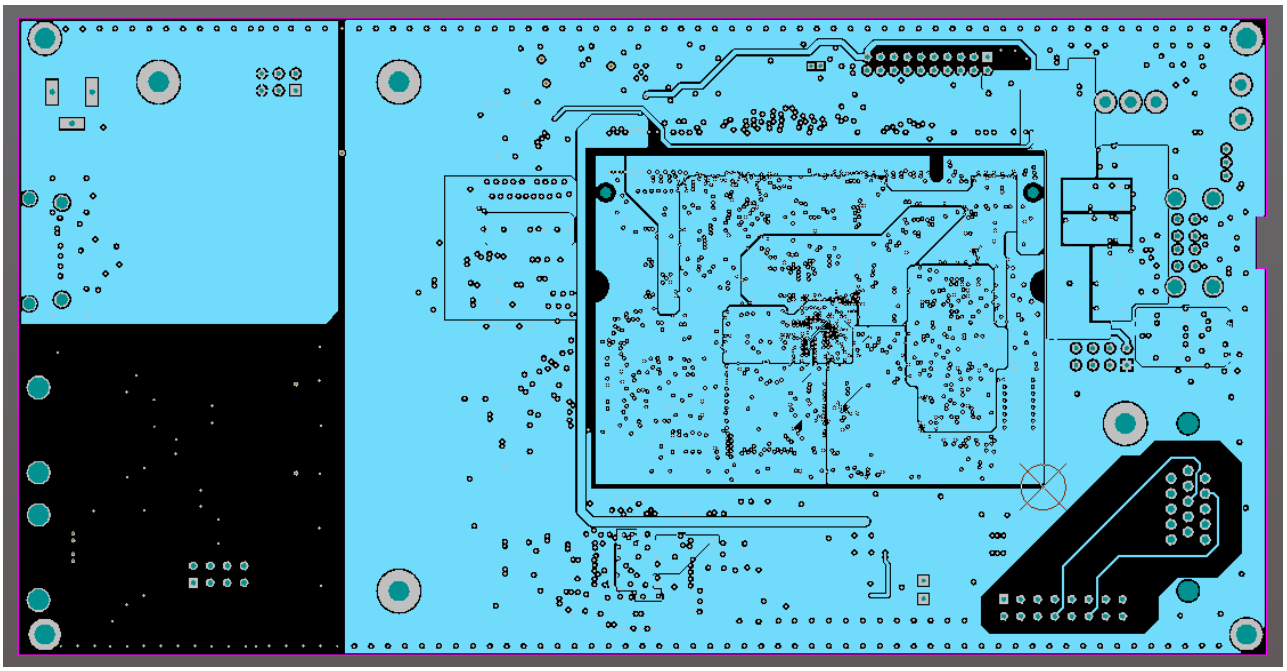
3.7.1 Main PCB top layer (1/6)



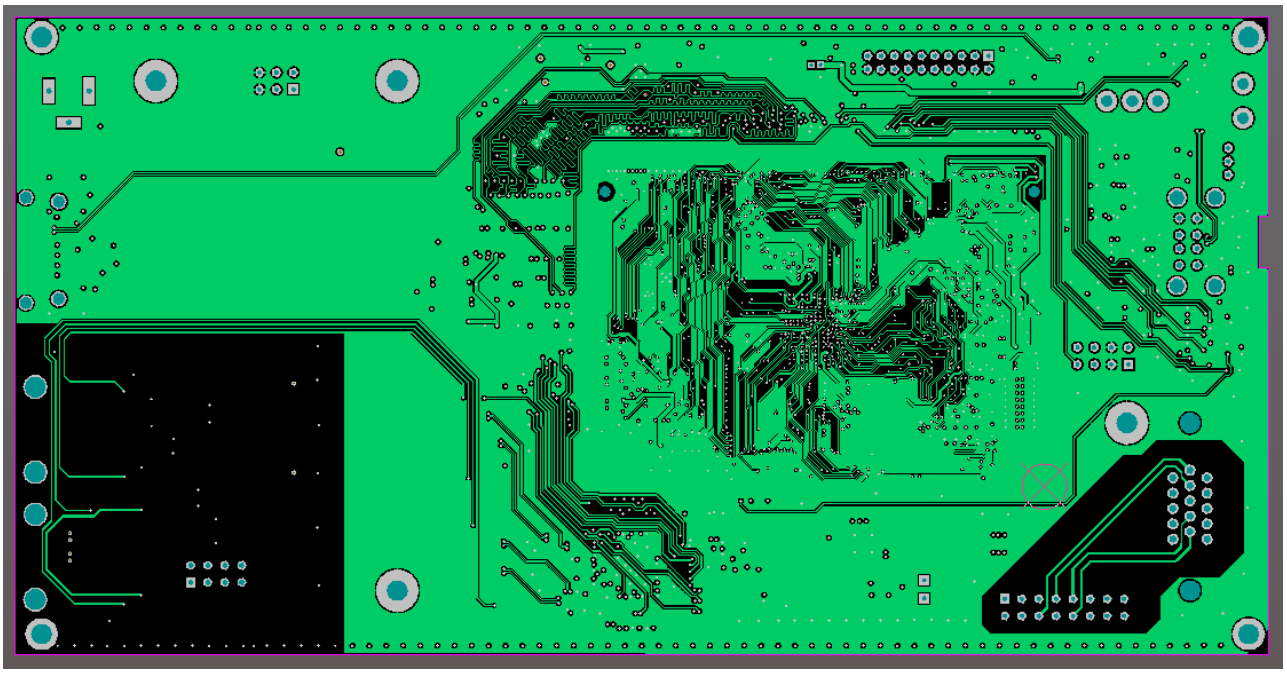
3.7.2 Main PCB 2nd layer (2/6)



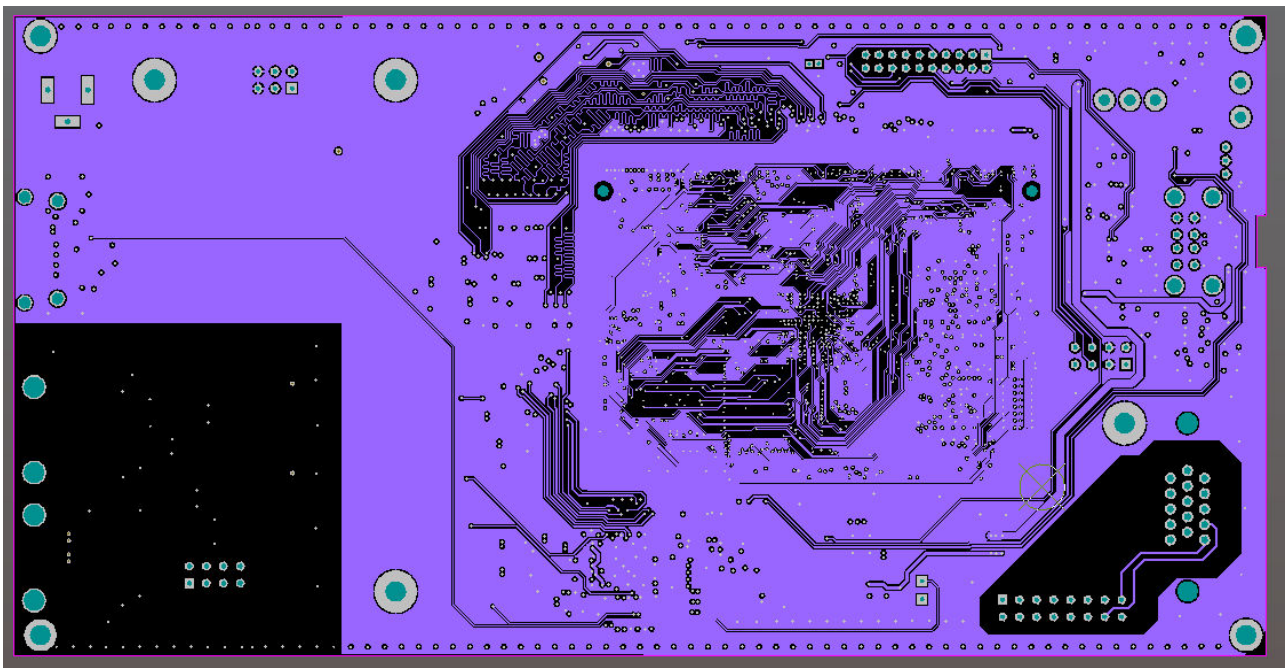
3.7.3 Main PCB 3rd layer (3/6)



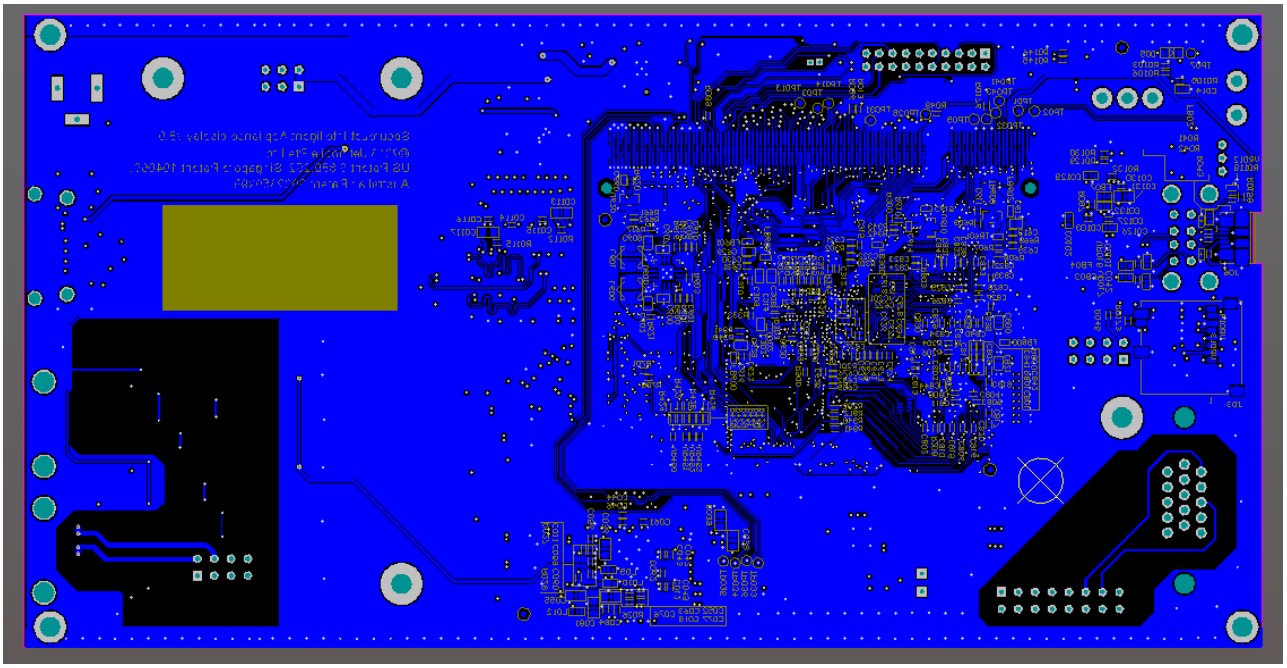
3.7.4 Main PCB 4th layer (4/6)



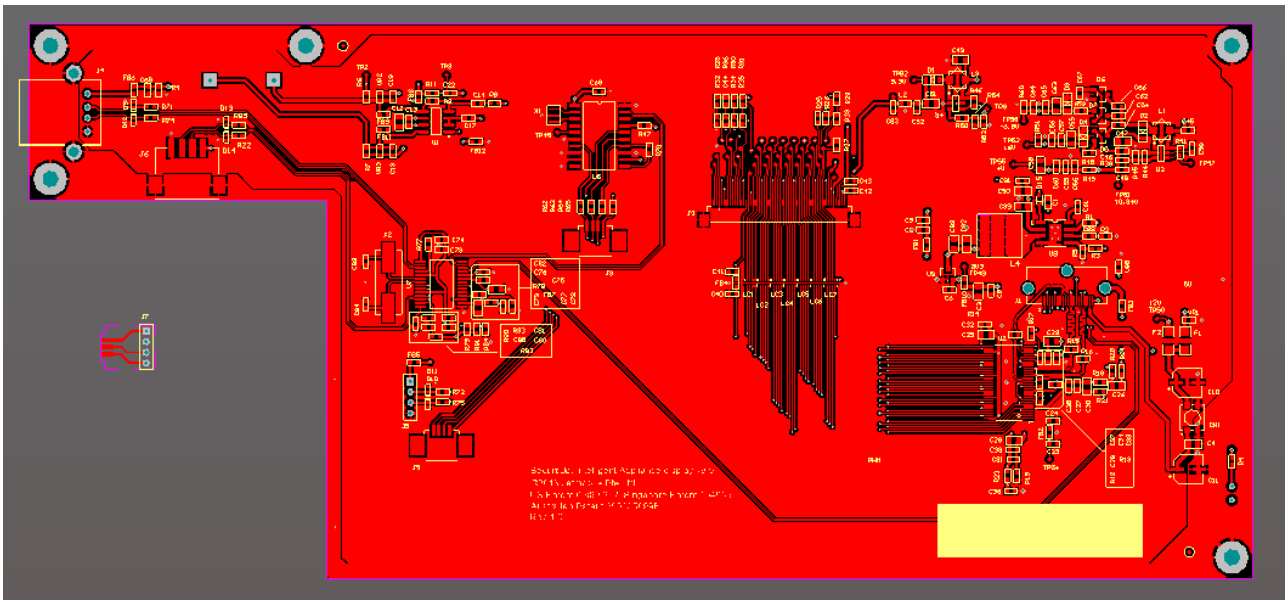
3.7.5 Main PCB 5th layer (5/6)



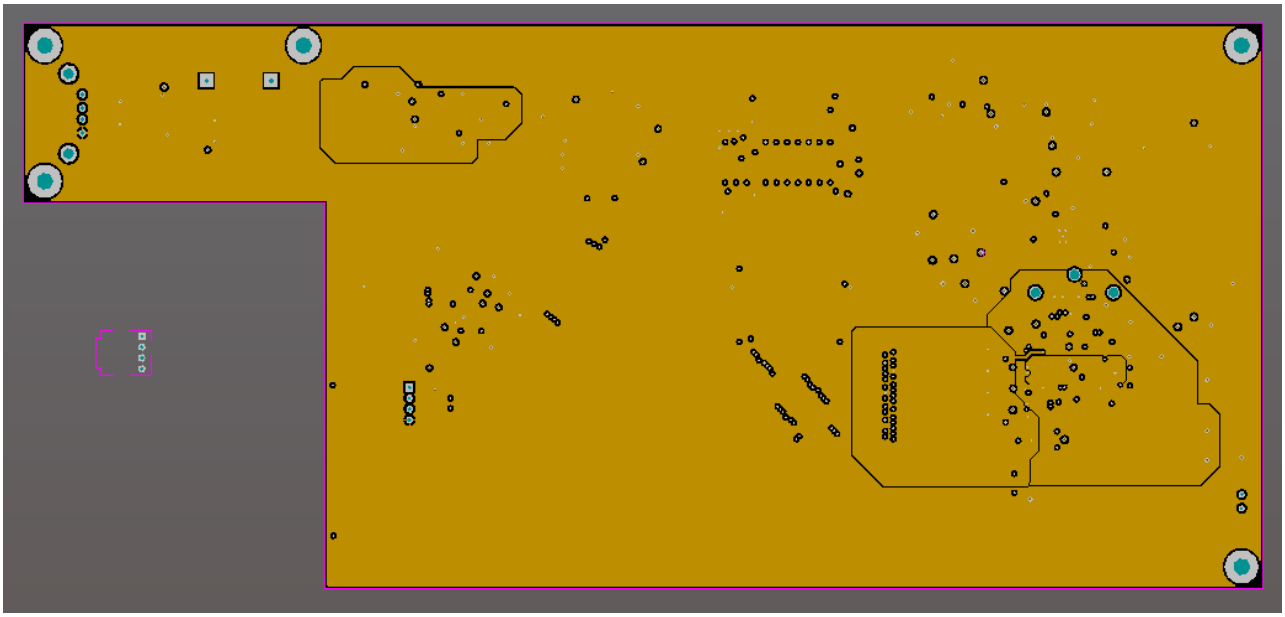
3.7.6 Main PCB 6th layer (bottom layer 6/6)



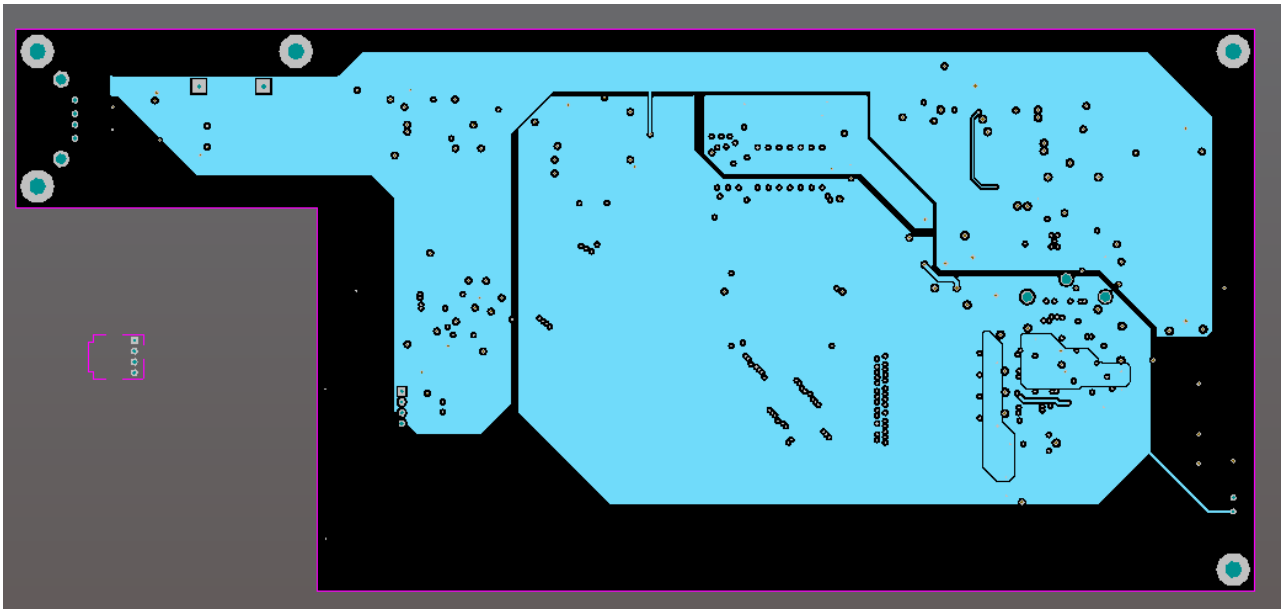
3.7.7 LCD PCB top layer (1/4)



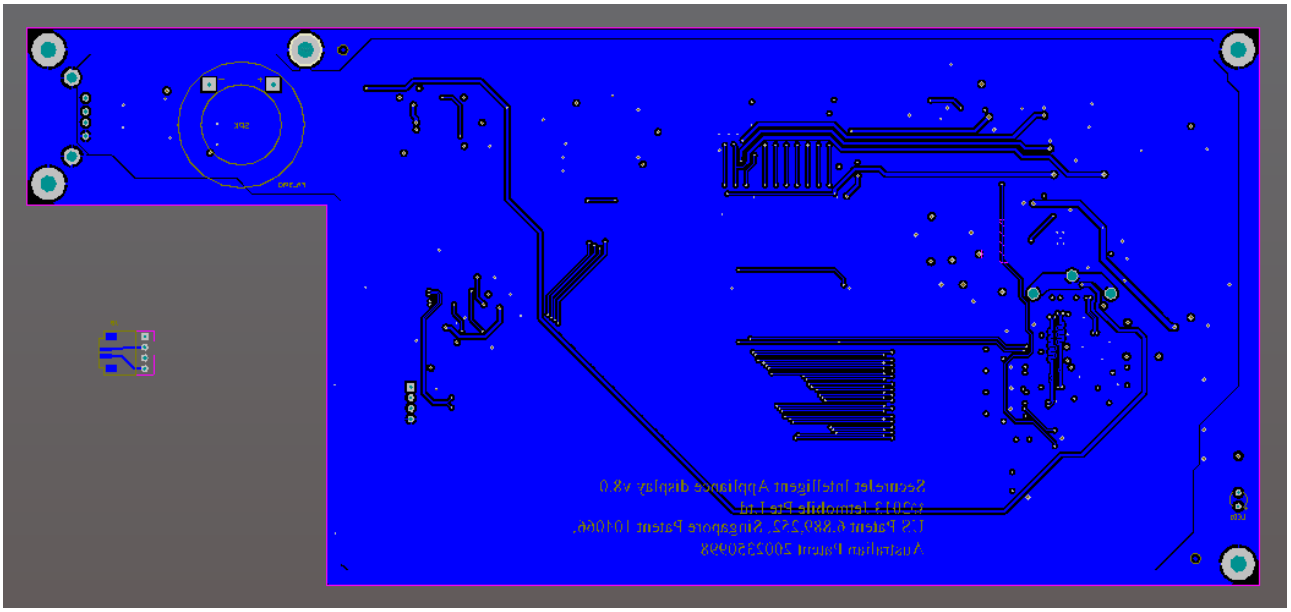
3.7.8 LCD PCB 2nd layer (2/4)



3.7.9 LCD PCB 3rd layer (3/4)



3.7.10 LCD PCB 4th layer (4/4)



3.8 Appendix B - schematics

Refer to attached files indicated

3.8.1 Main CPU device schematics file

CPU unit schematics.pdf

3.8.2 Main CPU device schematics file

Screen Display unit schematics.pdf

--- END OF DOCUMENT ---

REGULATORY COMPLIANCE

SecureJet Intelligent Appliance v8.0 is in conformity with the following standards and/or other normative documents.

RCM-Australia

FCC WARNING :
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE 1: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-- Reorient or relocate the receiving antenna.
-- Increase the separation between the equipment and receiver.
-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.

NOTE 2: Any changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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