Monarch 2 Platform

GM02S Module

Data Sheet

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About this Data Sheet

Purpose and Scope

The GM02S is a complete LTE Cat M1/NB1/NB2 module with baseband, RF and memory, targeted at narrow band low data rate M2M and IoT devices for wide deployment. This document provides technical information about GM02S LGA module. GM02S is based on Sequans's Monarch 2 platform.

Who Should Read this Document?

This document is intended for engineers who develop User Equipment (UE) for LTE systems.

Changes History

This is revision 17 of the GM02S data sheet, superseding version 16.

The signal list delivered as MS-Excel companion file to this data sheet is unchanged.

Version	Date	Changes
17	Jan. 2024	• Remove all hardware v.2 information (EoL as per PCN 12001-23), GM02RBAQRI/Y • New P/N GM02RBAQRL • SIM_VCC output current is increased to 30 mA (instead of 2) • Added a timing diagram in the Power section, as well as a warning related to V_{BAT} levels and power-up slew-rate • New section on MTTF calculation and figure
16	Oct. 2023	• New P/N GM02RBAQRK • Add info on water washing after reflow
15	Sept. 2023	• Added ADC info • Added new part numbers GM02RBAQRH and GM02RBAQRI • Added OTP status for all part numbers • Correction on pad #14 • Removed references to unusable UART3 • Add a mention that power consumption info is available elsewhere • Added further info on pads' physical dimensions • Add new certification information • Add total capacitance and inductance figures • Additional info on power modes • Add a warning about configuring two UART as console
14	Nov. 2022	• Add reliability figures for hardware v.3 (section 4.7) • Removed part numbers in headers in favour of hardware revisions • New GM02RBAQRF P/N in Table 2 (hardware v.3) • Added weight of the GM02S hardware rev. 3
13d	Oct. 2022	• New Part Number GM02RB6QRH in Table 2
13c	Oct. 2022	• New 'change history' presentation • Change THB information to 'PASS' in table 29 for hardware v.2
13b	Aug. 2022	• Updated THB information for hardware v.2. in Table 30
13a	Aug. 2022	• Harmonised Table 27 to gather information about hardware v.2 and v.3

Table 1. Change history

Version	Date	Changes
13	July 2022	• Added information about new hardware v.3 in Section 1.1 Frequency Bands, Section 1.5 Available Part Numbers, Section 1.4 General Features, Section 4.1 Package Description and Section 4.3 Packing • Created Chapter 6 Regulatory Approval for hardware v.3 (GM02RBAQRY)
12e	Dec. 2022	• New Part Number GM02RB6QRG in Table 2
12d	Oct. 2022	• New Part Number GM02RB6QRH in Table 2
12c	Oct. 2022	• New 'change history' presentation • Change THB information to 'PASS' in table 29 for hardware v.2
12b	Aug. 2022	• Updated THB information for hardware v.2. in Table 29
12a	July 2022	• Removed band B.71 operation for hardware v.2 in Section Frequency Bands and Table 22
12	May 2022	• Added information about LTE-M/NB-IoT dual mode operation in Chapter 1 General Description, Section 1.5 Available Part Numbers and Table 22 • Split Section 4.5 Regulatory Approval to accommodate NB-IoT operation
11	March 2022	• Updated Section 4.3 Packaging Information • Erratum to RESETN minimum value (100 ns → 100 µs) in Table 10
10	Feb. 2022	• Updated Section 1.5 Available Part Numbers with new UE and LR versions updated and new marking codes • Pad #71 changed to GND instead of DNC in Table 10 • Changes in Power-up Sequence in Section 3.1.2 Power-Up and Reset Sequences
9	Dec. 2021	• Updated Table 2 in Section 1.5 Available Part Numbers • Updated Section 4.2 Environmental Conditions • Updated Section 4.5 Reliability Specification • Additional RF information and recommendations • Added Section 5.1.3 NCC Regulatory Approval • Added performance at 2.2 V
8	Sept. 2021	• Updated Table 2 in Section 1.5 Available Part Numbers • Updated Section 4.2 Environmental Conditions • Updated Section 4.5 Reliability Specification
7	Aug. 2021	• Updated Table 2 Available Part Numbers • Updated wording related to CTS usage for flow control in Section 2.2 UART • Updated Section 4.3 Packing with full cardbox's weight • Added Section 4.5 Reliability Specification
6	May 2021	• Updated Figure 11 in Section 4.1 Package Description

Table 1. Change history (continued)

Version	Date	Changes
5[1]	April 2021	• Reorganised document • Updated Table 2 Available Part Numbers • Updated Section 3.1 Power • Added Section 3.4 Power Supply Dimensioning • Added Section 3.5 Maximum Electrical Ratings • Updated Chapter 5 Regulatory Approval: added ACMA Regulatory Marking, JATE TELEC Regulatory Marking, RED Regulatory Safety Notice, UKCA Regulatory Marking • Updated MS-Excel companion file with additional information
4	March 2021	• Updated orderable status in Section 1.5 Part Numbers • Updated Section 3.1.3 Power States • Added Sections Detailed Behaviour of I/O Pads of BIDIR Type and Detailed Behaviour of I/O Pads of BIDIR_WAKE Type in Section 3.1 Power • Updated Section 2.2 UART • Updated Section 2.3 SIM0 Interface • Updated Section 3.2 Digital I/O Characteristics • Updated Section 4.1 Package Description • Updated Section 4.2 Environmental Conditions • Updated Section 4.4 Storage and Mounting • Updated Section 5.1.1 FCC Regulatory Approval
3	Dec. 2020	• Updated part numbers details in Table 1 • Added timing diagrams in Section 3.1 Power • Added Section 3.1.3 Power States • Added default Enable status for GPIOs in Section 2.7 GPIO • Added RING0 polarity information in Table 2-13 • Restrict usage for pad #53 to Reserved • Updated wake signals default enable state • Updated V_{BAT} characteristics in Table 2-15 • Updated Section 4.3 Packing • Added Sections FCC Regulatory Approval and Industry Canada Statement in Chapter 5 Regulatory Approval • Changed assignment (from GND to DNC) for pads 71, 74, 75, 76, 77
2	Oct.2020	• Updated list of interfaces, added throughput figures in Chapter 2 • Updated Table 1 • Update power group descriptions in Chapter 2 Interfaces • Updated Figure in Section 4.1 Package Description • Added reflow profile information in Section 4.4 Storage and Mounting • Removed humidity figures in document
1	May 2020	First preliminary version

Table 1. Change history (continued)

1. Removed 'Preliminary' mention

Contents

1. General Description

The Monarch 2 GM02S an LTE Cat M1/NB1/NB2 module based on Sequans' second generation *Monarch 2* chip platform. The GM02S is a total module solution, including a complete, Single-SKU™ RF front end capable of operating on every GSM band worldwide, and an integrated EAL5+ Secure Element (SE) capable of hosting the SIM inside the module with zero compromise on security while lowering cost and reducing complexity. The GM02S is part of Sequans next generation "S" family of modules, featuring a very small and cost-effective form factor that requires no external components.

The GM02S leverages Sequans's 15-plus years of experience in 4G+ technologies and incorporates Sequans's carrier-approved LTE protocol stack and a software suite amongst the most mature in the industry. The GM02S is part of Sequans's next generation "S" family of modules, featuring a very small and cost-effective form factor which requires no external components. The GM02S inherits *Monarch's* already certified LTE-M and NB-IoT stack and delivers a significantly improved performance and lower power consumption thanks to Sequans's second generation *Monarch 2* chip and the new module architecture.

Sequans's technology, both hardware and software, is completely owned by Sequans, ensuring a fast time to market and the lowest total cost of ownership for device makers.

1.1. Frequency Bands

The GM02S supports the following bands:

- B1 (2100);
- B2 (1900 PCS);
- B3 (1800+);
- B4 (AWS-1);
- B5 (850);
- B8 (900 GSM);
- B12 (700 a);
- B13 (700 c);
- B14 (700 PS);
- B17 (700 b);
- B18 (800 Lower);
- B19 (800 Upper);
- B20 (800 DD);
- B25 (1900+);
- B26 (850+);
- B28 (700 APT);
- B66 (AWS-3);
- B71 (600)
- B85 (700 a+).
- B106 (LMR) -> 897.5 - 900.5 MHz in the US according to the FCC rules

1.2. Applications

GM02S is ideal for adding LTE-M and/or NB-IoT LTE connectivity to narrow band, low data rate M2M and IoT devices such as utility meters, industrial sensors, health and fitness appliances, asset trackers, and many additional devices in smart home, smart city, and wearable applications.

GM02S can also be used as a slim modem controlled by an external MCU via its UART. Alternatively, the GM02S can execute applets on its embedded MCU.

1.3. Block Diagram

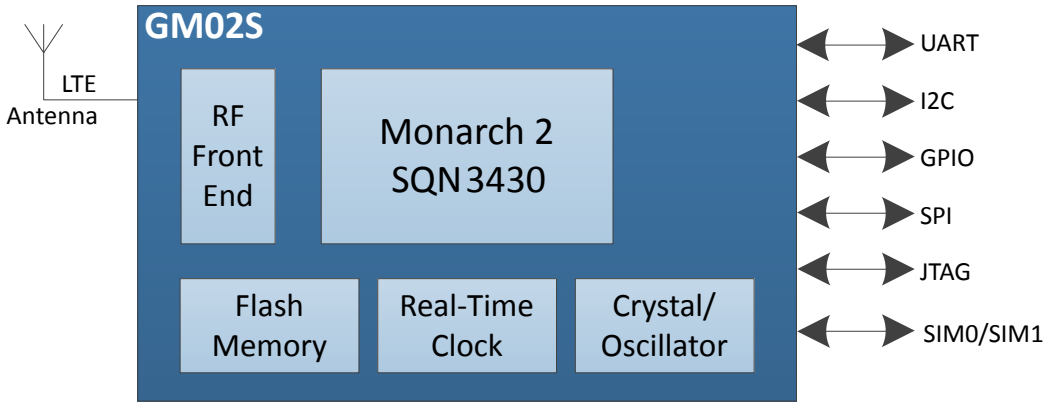

Figure 1. GM02S Block Diagram

1.4. General Features

Physical Characteristics	LGA module, 120 pads. Size: 16.3 × 17 × 2.3 mm
Temperature Range	Operation temperature range: -40 to +85 °C Storage: MSL3
Power Supply	Voltage range for RF compliance: 2.5 to 5.5 V Functional voltage range: 2.2 to 5.5 V
Tx Power	+23 dBm in each band
Interfaces	• Dual (U)SIM Card Interface: support for external, removable or fixed UICC. Support for integrated UICC (iUICC) with a dedicated p/n; • 4x High-Speed UART Interfaces with flow control, up to 921600 bauds; • GPIOs, I²C, SPI, PWM, Pulse Counter, I²S/PCM, ADC;
SMS	Text and PDU modes
Firmware Upgrade	UART interface, FOTA, support of full and differential firmware upgrade
RoHS	All hardware components fully comply with EU RoHS directive, bromine-free
LTE Features	• 3GPP LTE Release 13/14 Cat M1/NB1/NB2 compliant; • LTE Cat M1: 1.1 Mbps / 0.3 Mbps UL/DL throughput; • LTE Cat NB1: 62.5 kbps / 27.2 kbps UL/DL throughput; • LTE Cat NB2: 160 kbps / 120.7 kbps UL/DL throughput.

1.5. Available Part Numbers

GM02S's ECCN is 5A991.

Part Number	Hardware Version	Software Build (ATI1)	UE Version (ATI1)	PTCRB Model Name / Model	SVN	Availability Status
GM02RBAQRF	HW Rev. 3 FCC/IC/RED/UKCA ACMA/JATE/TELEC PTCRB/GCF	LR 8.0.5.11	UE 8.0.5.11	GM02S	12	Available with unlocked OTP
GM02RBAQRH		LR 8.0.5.12	UE 8.0.5.12		13	Available with unlocked OTP
GM02RBAQRK		LR 8.2.0.2	UE 8.2.0.2		15	Available with unlocked OTP
GM02RBAQRL		LR 8.0.5.13	UE 8.0.5.13		16	Available with unlocked OTP

Table 2. Available Part Numbers

2. Interfaces

The GM02S provides electric interfaces connecting it to the external parts, such as communication I/O ports, GPIO and antenna RF I/O. This chapter provides information about all these interfaces.

Power supply pins and details thereof are detailed in section Electrical, RF and Thermal Characteristics *(on page 12)*.

Important: Please refer to this data sheet's companion MS-Excel file for details on each pin's:

- Default assigned function;
- State during low power modes;
- Configurability with AT commands;
- Pull status and requirements.

2.1. Pin Assignment

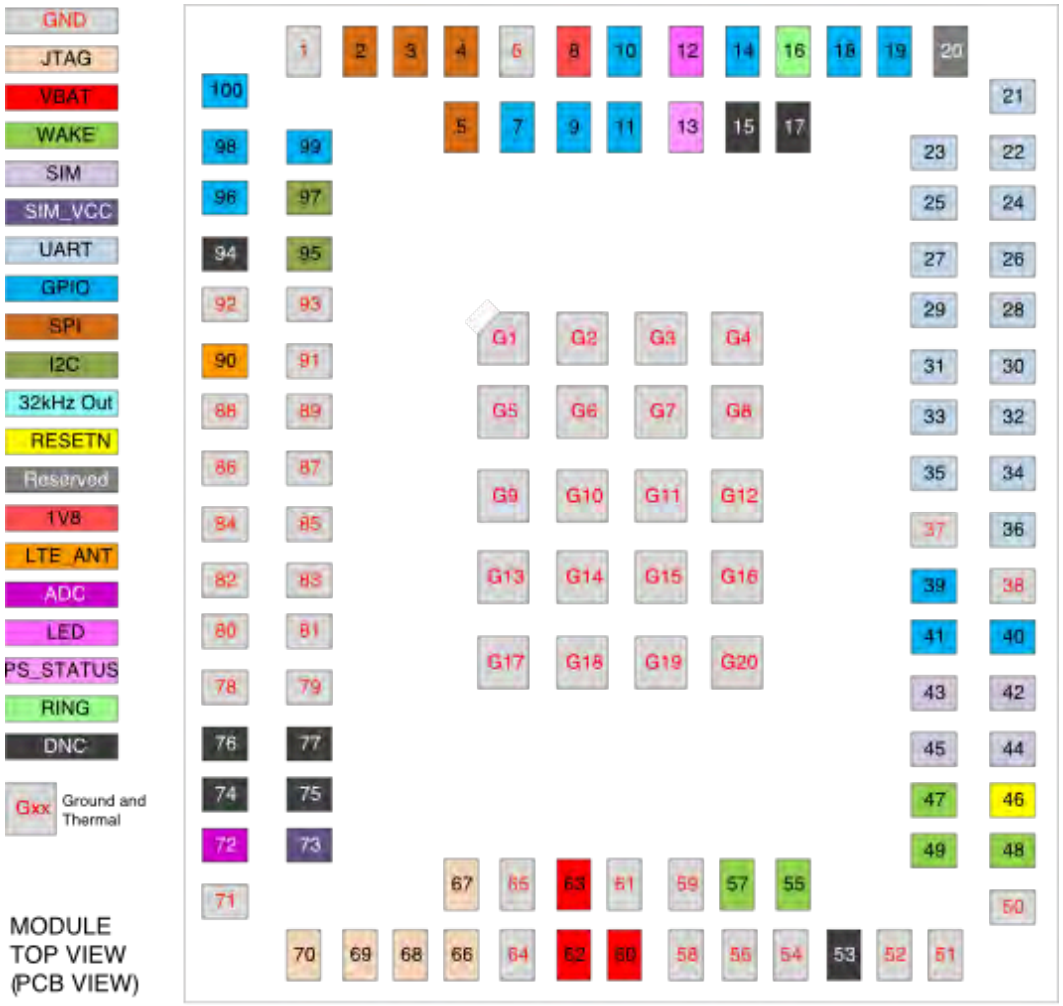

Figure 2. GM02S Module Pads Assignments

2.2. UART

When the GM02S is used as a slim modem, it has three UARTs available. The default function for each UART is as follows:

- UART0: data and control from external MCU via AT commands
- UART1: debug and upgrade
- UART2: modem console

This default configuration can be overridden.

Attention: Although possible, configuring two different UARTs as console will cause the kernel log messages to randomly appear on either one of them.

Note: See section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Alternate Function [2]	Power Group	Direction	Pad type [3]	Reset state
36	GPIO12/TXD0	TXD0	GPIO12	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART0					
34	GPIO13/RXD0	RXD0	GPIO13	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
35	GPIO14/ CTS0	CTS0	GPIO14	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
33	RTS0	RTS0	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
32	TXD1	TXD1	N/A	PVDD_1V8	In	BIDIR	High-Z, 2 mA
		UART1					
30	RXD1	RXD1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
31	CTS1	CTS1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
29	RTS1	RTS1	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
28	GPIO15/TXD2	TXD2	GPIO15	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART2					

Table 3. UART Signals

2. Alternate functions will be available in future versions via SW upgrade.
3. UART pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.

Pad #	Pad Name	Primary Function	Alternate Function [2]	Power Group	Direction	Pad type [3]	Reset state
26	GPIO16/RXD2	RXD2	GPIO16	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART2					
27	GPIO17/ CTS2/ DCD0	GPIO17	CTS2/ DCD0	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART2					
25	GPIO18/ RTS2/DSR0	GPIO18	RTS2/ DSR0	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART2					

Table 3. UART Signals (continued)

High-Speed UARTs Flow Control Signals

- CTS0, CTS1, CTS2 : Clear-To-Send signals of resp. UART0, UART1, UART2, (active low). To be connected to the CTS of the remote UART device. See Figure 3: UART Convention and Flow Control *(on page 6)*.

  Leave CTS unconnected if hardware flow control is not used.

- RTS0, RTS1, RTS2 : Ready-To-Send signals of resp. UART0, UART1, UART2, (active low). To be connected to the RTS of the remote UART device. Tie to a 1 kΩ pull-down when flow control is not used. If connected to an external part (like a RS 232 driver), the user must insure that the part presents a low level to the GM02S See Figure 3: UART Convention and Flow Control *(on page 6)*.

Figure 3: UART Convention and Flow Control *(on page 6)* represents the typical implementation for hardware flow control.

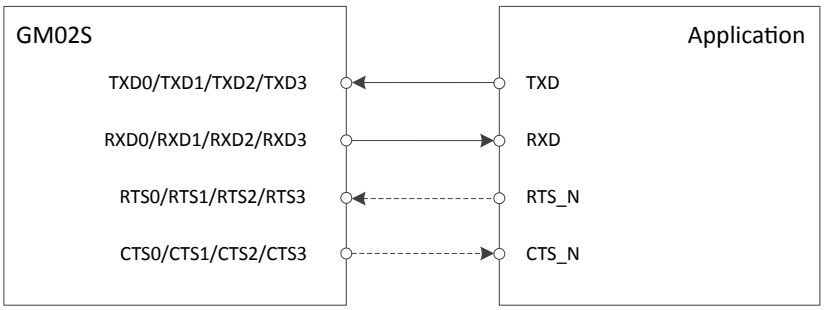

Figure 3. UART Convention and Flow Control

Note: Please refer to *Module Integration Guide* for details on UART connections.

2.3. USIM Interfaces

SIM0 Interface

This is the main external SIM interface. It can be used with removable or non-removable SIM cards or with soldered SIM chips. The modem manages the SIM's power supply to keep consumption as low as possible.

2. Alternate functions will be available in future versions via SW upgrade.
3. UART pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.

Note: See Section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Important: The GM02S only supports 1.8 V SIMs.

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type [4]	Reset State	Comment
42	SIM0_CLK	SIM0_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
45	SIM0_DETECT [5]	SIM0_DETECT	PMU_5V	In	IN	High-Z	Main SIM
44	SIM0_IO	SIM0_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA	Main SIM
43	SIM0_RSTN	SIM0_RSTN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
73	SIM0_VCC [6]	SIM0_VCC	PVDD_1V8	Out	SUPPLY	Out-0, 30 mA	Main SIM

Table 4. SIM0 Signals

SIM1 Interface

This GM02S 's interface to a second SIM is typically meant for soldered SIM chips (since it lacks SIM detect and SIM VCC). If the board makes use of a single SIM, it should be connected to the main SIM interface (see Section SIM0 Interface *(on page 6)* above).

Note: See Section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Alternate Function [7]	Power Group	Direction	Pad Type [8]	Reset state
40	GPIO26/SIM1_CLK	GPIO26	SIM1_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
41	GPIO27/ SIM1_RESETN	GPIO27	SIM1_RESETN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
39	GPIO25/SIM1_IO	GPIO25	SIM1_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA

Table 5. SIM1 Signals

2.4. I²C

Note: See Section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Alternate Function [9]	Power Group	Direction	Pad type [10]	Reset State
95	GPIO23/I2C_SDA	GPIO23	I2C_SDA	PVDD_1V8	In/Out	BIDIR	High-Z

Table 6. I²C Pad Details

4. USIM pad types electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.
5. SIM0_DETECT is active high (high when a card is present, low when no card is present). It can be configured as a WAKE pin via software command.
6. See range of values in Table 15: Power Pads *(on page 12)*.
7. Alternate functions will be available in future versions via SW upgrade.
8. Pad types electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.
9. Alternate functions will be available in future versions via SW upgrade.
10. I²C pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.

Pad #	Pad Name	Primary Function	Alternate Function[9]	Power Group	Direction	Pad type [10]	Reset State
97	GPIO24/I2C_SCL	GPIO24	I2C_SCL	PVDD_1V8	In/Out	BIDIR	High-Z

Table 6. I²C Pad Details (continued)

2.5. PCM

Note: See section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Alternate Function[11]	Power Group	Direction	Pad type [12]	Reset State
96	GPIO4/PCM_CLK	GPIO4	PCM_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
98	GPIO3/PCM_RXD	GPIO3	PCM_RXD	PVDD_1V8	In/Out	BIDIR	High-Z
99	GPIO5/PCM_FS	GPIO5	PCM_FS	PVDD_1V8	In/Out	BIDIR	High-Z
100	GPIO6/PCM_TXD	GPIO6	PCM_TXD	PVDD_1V8	In/Out	BIDIR	High-Z

Table 7. PCM Pad Details

2.6. SPI

Note: See section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Alternate Function[13]	Power Group	Direction	Pad type [14]	Reset state
3	GPIO7/SPI_SDI	GPIO7	SPI_SDI	PVDD_1V8	In/Out	BIDIR	High-Z
4	GPIO8/SPI_SDO	GPIO8	SPI_SDO	PVDD_1V8	In/Out	BIDIR	High-Z
2	GPIO9/SPI_CLK	GPIO9	SPI_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
5	GPIO10/SPI_CSN1	GPIO10	SPI_CSN1	PVDD_1V8	In/Out	BIDIR	High-Z
7	GPIO11/SPI_CSN2	GPIO11	SPI_CSN2	PVDD_1V8	In/Out	BIDIR	High-Z

Table 8. SPI Pad Details

2.7. GPIO

33 GPIOs are available on the GM02S the first 28 are named GPIO1 to GPIO28 and the last five GPIO31 to GPIO35. The GPIOs listed in Table 9: GPIO pads detail *(on page 9)* are not enabled by default. Their states are controlled by software.

9. Alternate functions will be available in future versions via SW upgrade.
10. I²C pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.
11. Alternate functions will be available in future versions via SW upgrade.
12. PCM pad types's electrical characteristics are detailed Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.
13. Alternate functions will be available in future versions via SW upgrade.
14. SPI pad types' electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.

GPIO Range	Default State
GPIO3 to GPIO11	Disabled
GPIO17 to GPIO28	Disabled
GPIO31 to GPIO32	Disabled

Table 9. GPIO pads detail

The GPIOs are documented in this data sheet according to their shared or assigned function. In addition to the GPIO, five wake signals are also available (see section Other Signals *(on page 9)*).

2.8. Other Signals

Pads Type	Pads Number
GND	1, 6, 37, 38, 50, 51, 52, 54, 56, 58, 59, 61, 64, 65, 71,78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 91, 92, 93
DNC (Reserved)	15, 17, 53, 74, 75, 76, 77, 94

Table 10. GND and DNC pads

Note: See Section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Name	Primary Function	Alternate Function[15]	Power Group	Direction	Pad Type[16]	Reset State
72	ADC1	ADC1 (see below)	N/A	N/A	In	IN	N/A
		Analogue-Digital Converter (ADC, IN)					
12	GPIO1/ STATUS_LED	STATUS_LED	GPIO1	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Status LED (STATUS_LED, OUT)					
13	GPIO2/ PS_STATUS	PS_STATUS	GPIO2	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high.					
14	GPIO28/DTR0	GPIO28	DTR0	PVDD_1V8	In/Out	BIDIR	High-Z
19	GPIO31/PWM0/ PULSE0/ 19M2_OUT	GPIO31	PWM0/ PULSE0/ 19M2_OUT	PVDD_1V8	In/Out	BIDIR	High-Z
18	GPIO32/PWM1/ PULSE1	GPIO32	PWM1/PULSE1	PVDD_1V8	In/Out	BIDIR	High-Z
9	GPIO33/TX_IND	TX_IND	GPIO33	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Transmission indicator (TX_IND, OUT). Active high.					

Table 11. Other Signals (No Interface)

15. Functions will be available in future versions via SW upgrade.
16. Pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.

Pad #	Name	Primary Function	Alternate Function[15]	Power Group	Direction	Pad Type[16]	Reset State
10	GPIO34/ ANT_TUNE0	ANT_TUNE0	GPIO34	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE0, OUT)					
11	GPIO35/ ANT_TUNE1	ANT_TUNE1	GPIO35	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE1, OUT)					
20	RESERVED/ FFF_FFH	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	High-Z, 2 mA
		Boot mode selection (FFF_FFH, IN). This pad needs a pull-down resistor by default.					
46	RESETN	RESETN	N/A	PMU_5V	In	IN	In, Pull-up
		Module HW reset signal. Active low. The minimum duration of a reset pulse on the RESETN signal is 100 µs.					
16	RING0	RING0	N/A	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART0 ring line (RING0, OUT). Enabled by default with inverted polarity.					
48	WAKE0	WAKE0	N/A	PMU_5V	In	IN	High-Z
		Wake #0 input line (WAKE0, IN), disabled by default.					
47	WAKE1	WAKE1	N/A	PMU_5V	In	IN	High-Z
		Wake #1 input line (WAKE1, IN), disabled by default.					
49	WAKE2	WAKE2	N/A	PMU_5V	In	IN	High-Z
		Wake #2 input line (WAKE2, IN), disabled by default.					
55	WAKE3	WAKE3	N/A	PMU_5V	In	IN	High-Z
		Wake #3 input line (WAKE3, IN), disabled by default.					
57	WAKE4	WAKE4	N/A	PMU_5V	In	IN	High-Z
		Wake #4 input line (WAKE4, IN), disabled by default.					

Table 11. Other Signals (No Interface) (continued)

ADC Specifications

The ADC1 pin 72 has the following specifications:

Parameter	Value	Unit
Resolution	14	bit
Dynamic Range	75	dB
Signal-to-Noise Ratio (SNR)	68	dB
Effective Number of Bits	11	bit
Input Signal Bandwidth	1.4	MHz
Full-scale Voltage	1.8	V

Table 12. ADC Specifications

15. Functions will be available in future versions via SW upgrade.
16. Pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.

Parameter	Value	Unit
Input Resistance	40	kΩ

Table 12. ADC Specifications (continued)

2.9. JTAG

Note: See Section Power *(on page 12)* for behaviour of I/Os in Deep Sleep mode.

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type [17]	Reset State
69	JTAG_TCK	JTAG_TCK	PVDD_1V8	In	IN	In, Pull-down, Schmitt-trigger
67	JTAG_TDI	JTAG_TDI	PVDD_1V8	In	IN	In, Pull-up
68	JTAG_TDO	JTAG_TDO	PVDD_1V8	Out	BIDIR	Out, 0
66	JTAG_TMS	JTAG_TMS	PVDD_1V8	In	IN	In, Pull-up
70	JTAG_TRSTN	JTAG_TRSTN	PVDD_1V8	In	IN	In, Pull-down

Table 13. JTAG pads Details

Note: The GM02S does not support boundary scan (IEEE 1149.1) for production testing.

2.10. Antenna

Pad #	Pad Name	Direction	Comments
90	LTE_ANT	In/Out	Main Antenna, for Rx and Tx

Table 14. Antenna pad Details

17. JTAG pad types's electrical characteristics are detailed in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)*.

3. Electrical, RF and Thermal Characteristics

3.1. Power

Important: Details about power consumption can be found in the Software Release note corresponding to the product's software version installed.

Power Pads Characteristics

Note: Pad 1V8 is the reference voltage for I/Os. It can be used to provide power to small devices (100 mA maximum usage). This voltage is not available when the modem is in Deep Sleep mode. When the modem is in standby the voltage drops to 1.62 V as per Table 15: Power Pads *(on page 12)*.

Pad #	Pad Name	Power Group	Direction	Min Value	Typical Value	Max Value
8	1V8 (see Note above)	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
73	SIM_VCC [18]	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
60, 62, 63	V_{BAT}	N/A	In	2.2 V		5.5 V

Table 15. Power Pads

Note: Reference V_{BAT} voltage range is 2.5 V to 5.5 V for RF-compliant operation and 2.2 V to 5.5 V for functional operation with possible degradation of RF performances.

Note: The GM02S does not use any boost or step-up DC/DC converters.

18. See also Section USIM Interfaces *(on page 6)*.

Power-on, Power-off and Reset

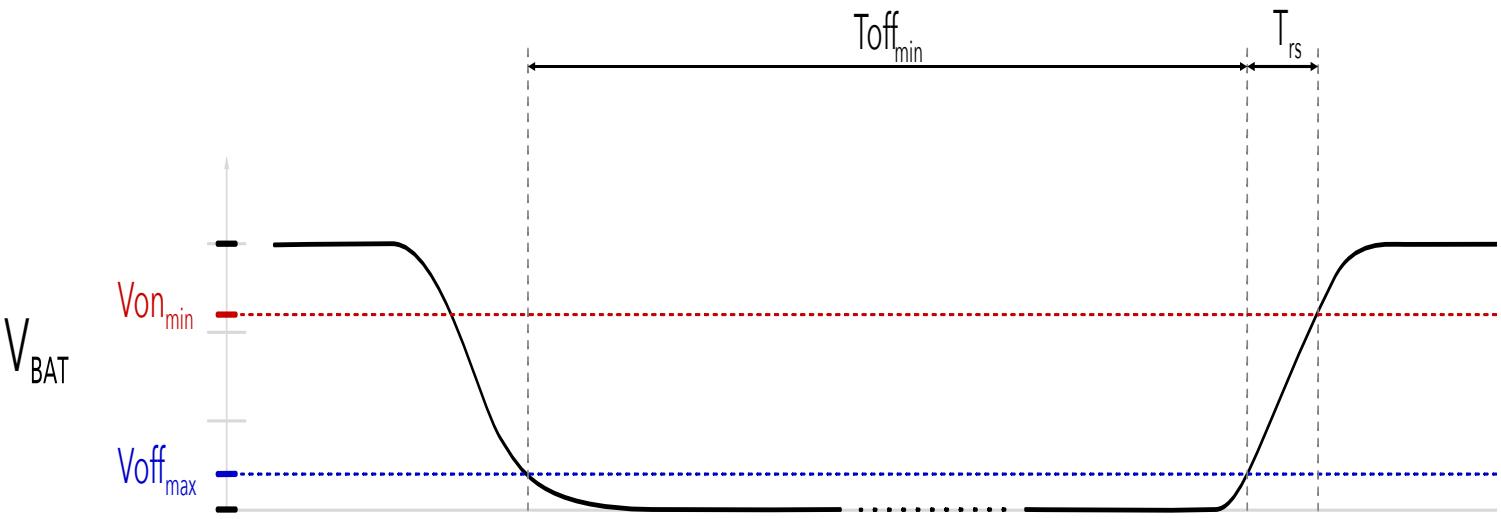

Figure 4. Power Cycle Timing

Name	Description	Min.	Typ.	Max.	Unit
Von_{min}	Minimal ON Voltage	2.2			V
T_{rs}	V_{BAT} Rise Time from $Voff_{max}$ to Von_{min}			10	ms

Table 16. Timing values

The value of $Toff_{min}$ depends on the $Voff_{max}$ voltage. The following table gives three typical figures:

Name	Description	Value
$Toff_{min}$ @ 50 mV	Minimal OFF ($V_{BAT} \leq Voff_{max}$) time to insure complete reset when $Voff_{max}$ = 50 mV	0.1 s
$Toff_{min}$ @ 0.1 V	Minimal OFF ($V_{BAT} \leq Voff_{max}$) time to insure complete reset when $Voff_{max}$ = 0.1 V	0.5 s
$Toff_{min}$ @ 0.2 V	Minimal OFF ($V_{BAT} \leq Voff_{max}$) time to insure complete reset when $Voff_{max}$ = 0.2 V	1 s

Table 17. $Toff_{min}$ vs. $Voff_{max}$

CAUTION: V_{BAT} must **always** be at least equal to Von_{min} during normal operation. Once V_{BAT} has dropped below this threshold, **always** ensure the voltage keeps on dropping down to $Voff_{max}$ and remains low for at least $Toff_{min}$. Failure to comply, as well as failure to meet the maximum V_{BAT} rising time requirement (T_{rs}) during power-on, can result in erratic behaviour.

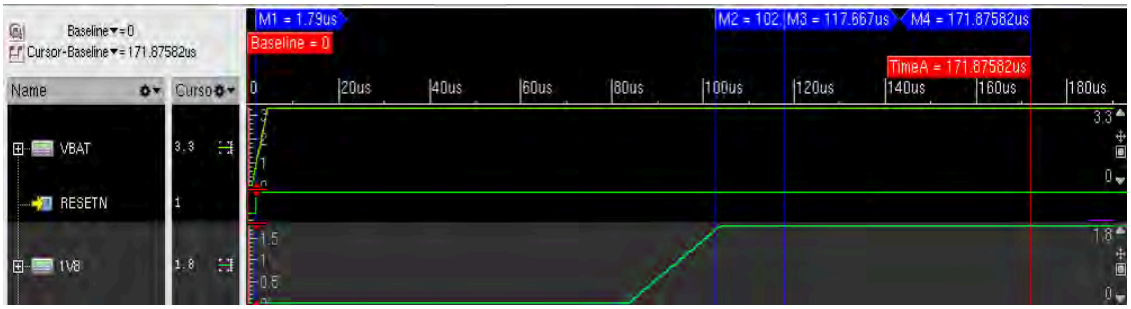

Figure 5. Typical Timing Diagram for Power-Up Sequence

Important: The 1V8 power signal can remain low up to 370 µs after the V_{BAT} rising edge

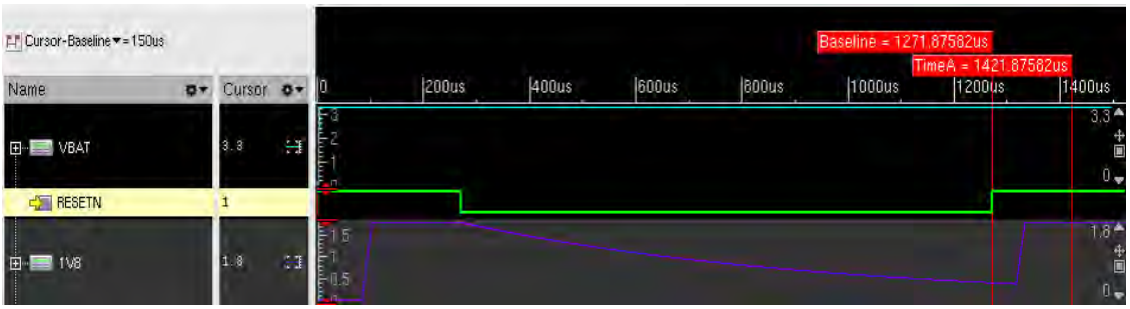

Figure 6. Typical Timing Diagram for Reset Sequence

Note: since RESETN is pulled-up internally, RESETN does not need to be held low after V_{BAT} is established, as shown in Figure 6: Typical Timing Diagram for Reset Sequence *(on page 14)*. There is no timing condition between RESETN and V_{BAT}.

Note: RESETN minimum duration for reliable detection is 100 µs

Power States

Figure 7: Electrical States and Transitions *(on page 15)* represents the electrical states of the module and their transitions.

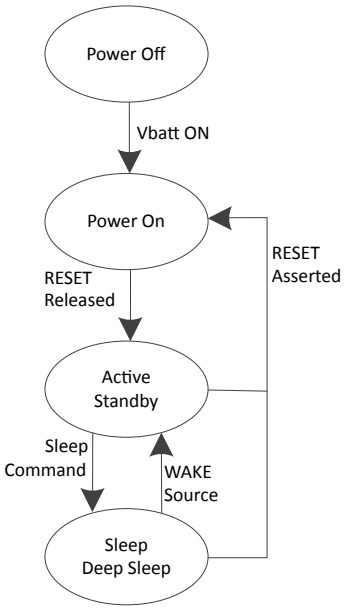

Figure 7. Electrical States and Transitions

There are four possible power modes:

- Active mode: operational, UART on, RF on, LCPU/MCPU/DSP are running. Power consumption depends on workload and transmit power level.
- Standby mode: Same as active mode, except RF off.
- Sleep mode: MCPU/LCPU/DSP are power gated, UART off, RAM content is salvaged. Power level 300 µA circa.
- Deep Sleep Mode: Only the power management unit (PMU) stays active. Power level 1 µA.

More information is given in the table below:

Power Mode	LTE Mode	Available Interfaces
Active	Connected (RF on)	All interfaces
Standby	Connected (RF off)	All interfaces
Sleep	Short eDRX idle duration RRC Idle	WAKE pins (including RTS0/1)
Deep Sleep	PSM idle, Long eDRX idle duration, radio-off, airplane mode	WAKE pins (including RTS0/1)

Table 18. Power Modes Description

PVDD_1V8 BIDIR Pads State in Deep Sleep mode

In Deep Sleep mode, the Digital PVDD_1V8 bi-directional I/Os are completely powered off and behave like 50 MΩ high-impedance pins.

PMU_5V IN Pads State in Deep Sleep mode

In Deep Sleep mode the digital PMU_5V inputs are completely powered off and behave like 180 MΩ high-impedance pins.

Table 19: Measured Leakage Current for the PMU Wake Inputs *(on page 16)* gives the values of the measured leakage current (measurements taken on silicon) for the PMU wake inputs.

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 19. Measured Leakage Current for the PMU Wake Inputs

Table 20: External Pull-up/Pull-down Resistor at PMU Wake Input Pads *(on page 16)* shows values of the external pull-up/pull-down resistor to be used at the PMU wake inputs pads.

Minimum	Typical	Maximum
1 kΩ	10 kΩ	100 kΩ

Table 20. External Pull-up/Pull-down Resistor at PMU Wake Input Pads

Table 21: PMU Wake Input Pulses Detection Mechanism Timings *(on page 16)* details the PMU wake input pulses detection mechanism timings.

Maximum pulse width guaranteed to be ignored	Minimum pulse width guaranteed to be recognised
11.1 ns	100 µs

Table 21. PMU Wake Input Pulses Detection Mechanism Timings

Table 22: Internal Pull-Up Current at RESETN Pad *(on page 16)* provides the internal pull-up current range at RESETN.

Minimum	Typical	Maximum
73.5 nA	100 nA	160.5 nA

Table 22. Internal Pull-Up Current at RESETN Pad

3.2. Digital I/O Characteristics

This section details the voltage and current characteristics of the various I/O pads of the GM02S .

The I/Os belong either one of two power groups:

- PVDD_1V8
- PMU_5V

The operational voltage range of both power groups is described in Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* and Table 24: DC Ratings for Digital I/Os, PMU_5V Power Group *(on page 17)*.

CAUTION: Designers must ensure that the input voltage on any of the I/O pads never exceeds the V_{IH} of the power group they belong to.

See Table 23: DC Ratings for Digital I/Os, PVDD_1V8 Power Group *(on page 17)* for the digital I/O characteristics of the different I/O pads. Refer to each interface of the GM02S in chapter Interfaces *(on page 4)* for the power group and I/O pad type of each pad. Note that IN pads are inputs only whereas BIDIR can be both inputs and outputs.

Symbol	Minimum	Maximum	Unit
V_{IH} – Input HIGH level	1.26	3.3	V
V_{IL} – Input LOW level	0	0.54	V
V_{OH} – Output HIGH voltage	1.44	1.8	V
V_{OL} – Output LOW voltage	0	0.36	V
I_{RPU} – Input pull-up resistor current	15		µA
R_{RPU} – Input pull-up resistance	27	34	kΩ
I_{RPD} – Input pull-down resistor current	15		µA
R_{RPD} – Input pull-down resistance	27	34	kΩ
V_H – Input hysteresis	0.18		V
I_{PAD} – Input leakage current, non-tolerant	-1	1	µA
I_{OZ} – Off-State leakage current		1	µA

Table 23. DC Ratings for Digital I/Os, PVDD_1V8 Power Group

Symbol	Minimum	Maximum	Unit
V_{IH} – Input HIGH level	0.8	V_{BAT} + 0.6 (max. 5.5)	V
V_{IL} – Input LOW level	0	0.2	V

Table 24. DC Ratings for Digital I/Os, PMU_5V Power Group

The total capacitance of the GM02S is 115 µF. Total inductance is 5.3 µH.

3.3. RF Performance

Important: For proper operation, the VSWR at the antenna pad must be better than 2:1 in conducted mode and 3:1 in radiated mode. A higher value could result either in poor RF performance, reduced Tx power or increased sideband/harmonic emission levels. Very high VSWRs can permanently damage the power amplifier.

It is recommended to add a DC blocking capacitor in series with the module RF input/output pad (#90).

RF Sensitivity

The GM02S exhibits the following typical RF sensitivity at 2.5 V:

Technology	Band	Typical Sensitivity
LTE-M	Low Bands: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B71, B85, B106	-105 dBm
	High bands: B1, B2, B3, B4, B25, B66	-106 dBm
NB-IoT	Low Bands: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B71, B85	-108 dBm

Table 25. RF Sensitivity

Technology	Band	Typical Sensitivity
	High bands: B1, B2, B3, B4, B25, B66	-108 dBm

Table 25. RF Sensitivity (continued)

CAUTION: The maximum safe RF input power is 3 dBm.

RF Output Power

The GM02S maximum output power within the recommended operating range (from 2.5 to 5.5 V) is given in Table 26: RF Max Output Power *(on page 18)*.

Bands	Output Power
All Bands	23 dBm ± 1 dB

Table 26. RF Max Output Power

RF performance at 2.2 V

While it is not recommended to operate the GM02S in the range 2.2 to 2.5 V, the RF section will continue to work normally, albeit with reduced TX output power as shown in Table 27: RF Performance at 2.2 V compared to 2.5 V *(on page 18)* below.

Temperature	Sensitivity Loss	Output Power Loss
-30 °C	No loss	1.1 dB
25 °C	No loss	1.1 dB
85 °C	No loss	1.7 dB

Table 27. RF Performance at 2.2 V compared to 2.5 V

3.4. Power Supply Dimensioning

This section provides guidance to designers working on the power supply or selecting a suitable battery to power the GM02S .

Overview

The current consumption of the GM02S peaks before every TX sub-frame as shown in Figure 8: Current Consumption in TX Sub-Frame *(on page 19)*. In this figure, the time division is 50 µs. Around 150 µs from the start, two current pulses peaking 34% higher than the average current consumption during the 23 dBm TX tone which follows can be observed.

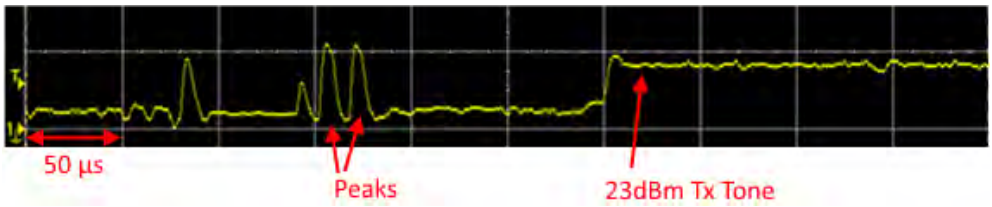

Figure 8. Current Consumption in TX Sub-Frame

Peak Current Measurement Method

Sequans recommends to use the setup represented in Figure 9: Setup for Current Peak Measurement *(on page 19)* for peak current measuring. This setup was used to record the measurements presented in Table 28: Peak Current Measurements *(on page 19)*.

Note that:

1. Voltage probes are placed close to module V_{BAT} input;
2. Voltage probes accuracy is calibrated using a current probe;
3. A large capacitance C_{batt} is placed close to the V_{BAT} pin to simulate a battery and screen the device from the parasitic inductances of the cables and tracks;
4. 2 × 22 µF capacitors (C_{ext}) are placed between the voltage probes and the module V_{BAT} input to soften the current peaks.

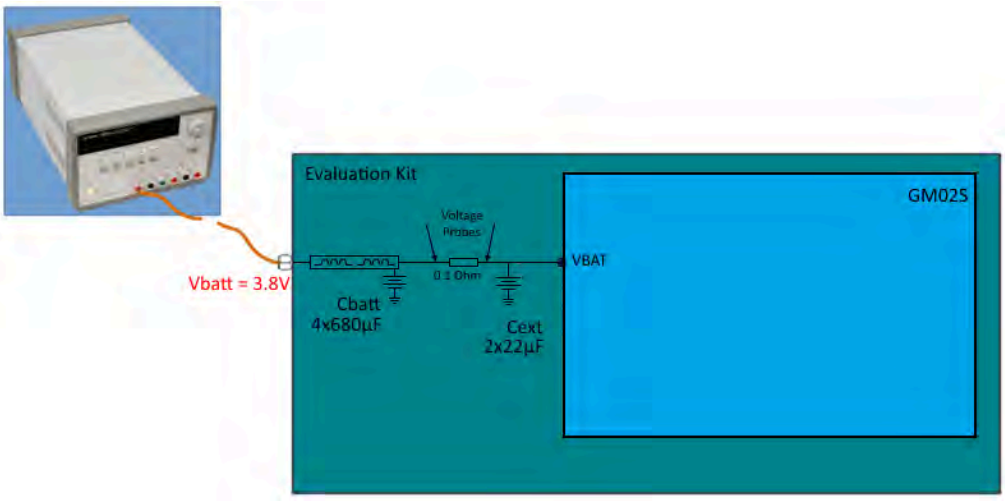

Figure 9. Setup for Current Peak Measurement

Peak Current Measurement

Table 28: Peak Current Measurements *(on page 19)* gives the peak current values measured on the setup shown on Figure 9: Setup for Current Peak Measurement *(on page 19)* for different voltages and temperatures.

Input Voltage	T = -40°C	T = -30°C	T = +25°C	T = +85°C
5.5 V	328 mA	305 mA	263 mA	268 mA
3.8 V	475 mA	438 mA	444 mA	479 mA
2.5 V	705 mA	667 mA	679 mA	741 mA

Table 28. Peak Current Measurements

Input Voltage	T = -40°C	T = -30°C	T = +25°C	T = +85°C
2.2 V	676 mA	640 mA	652 mA	717 mA

Table 28. Peak Current Measurements (continued)

Margin

Important: It is recommended that designs potentially sensitive to the current peaks described in this section use the recommended C_{ext} 2 × 22 µF and dimension the power supply with an extra 20% margin w/r to the values provided in this section.

Module's Total Capacitance and Inductance

The module's sum of internal capacitance (positive side tolerance) is 115 µF.

The module's sum of internal inductance (positive side tolerance) is 5.3 µH.

3.5. Maximum Electrical Ratings

Parameter	Minimum	Maximum
Supply Voltage V_{BAT}	-0.2 V	5.5 V
I/Os in Power Group PVDD_1V8	-0.2 V	4.125 V
I/Os in Power Group PMU_5V	-0.2 V	6.0 V

Table 29. Maximum Electrical Ratings

3.6. Thermal Considerations

Special attention needs to be given to thermal dissipation.

The outer layers of the host board must be covered in as many wide copper areas as possible, and those must be stitched with evenly spaced ground vias. Care must be taken that no air gap exists along the thermal path from the GM02S to the dissipating copper area(s). Gaps can be filled with heat conducting materials such as GapPad™.

The Gxx pads should be tied to a large ground plane on the customer's PCB layer 1. It is also recommended to have the Gxx pads area on the PCB stitched with through ground vias to improve thermal dissipation.

If the host board is piggybacked over a larger board, the aforementioned heat dissipation considerations should be applied to both the main and the daughter board.

4. Mechanical Characteristics

4.1. Package Description

The module footprint is (16.3 ± 0.15) mm × (17.0 ± 0.15) mm × 2.30 mm (max.).

Maximum 'warpage' is 0.13 mm (as per JEITA ED7306).

See below for the other dimensions.

The GM02S weighs 1.42 g.

Hardware Module Dimensions

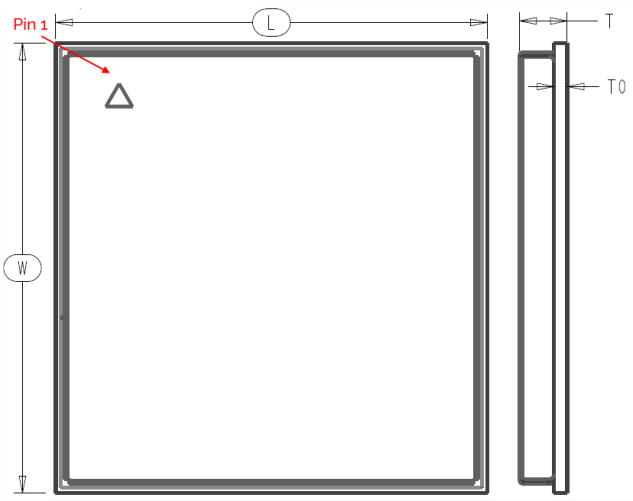

Figure 10. Module Top and Side Views

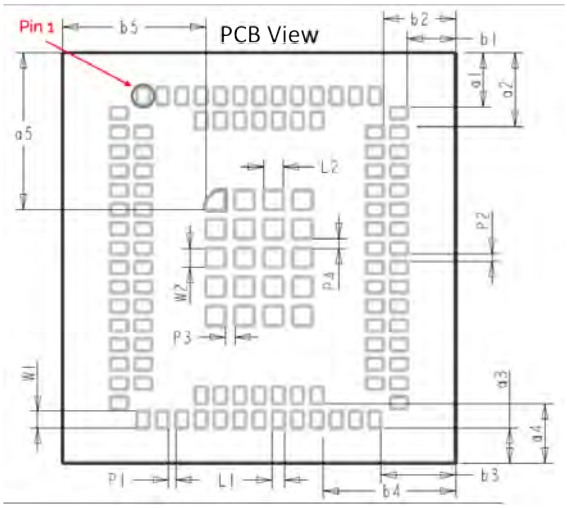

Figure 11. Module PCB Views

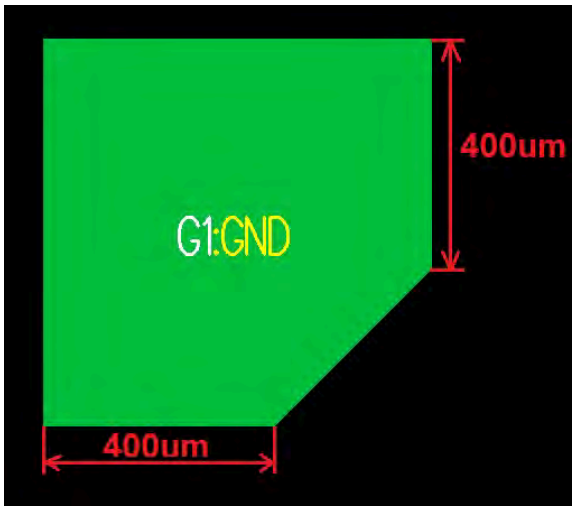

Figure 12. Details of chamfered central ground pad G1

Dimension	Value (mm)
L	16.3 ± 0.15
W	17.0 ± 0.15
T	2.3 max (2.2 typical)
T0	0.8 max
L1	0.5 ± 0.1
W1	0.7 ± 0.1
L2	0.8 ± 0.1
W2	0.8 ± 0.1
a1	2.25 ± 0.1
a2	3.05 ± 0.1
a3	1.45 ± 0.1
a4	2.45 ± 0.1
a5	6.5 ± 0.1
b1	2.0 ± 0.1
b2	3.0 ± 0.1
b3	3.1 ± 0.1
b4	5.5 ± 0.1
b5	5.95 ± 0.1
P1	0.3 ± 0.1
P2	0.3 ± 0.1
P3	0.4 ± 0.1

Table 30. Module Dimensions (mm)

Dimension	Value (mm)
P4	0.4 ± 0.1

Table 30. Module Dimensions (mm) (continued)

Laser Marking

Figure 13. GM02S Laser Marking

Notes on Figure 13: GM02S Laser Marking *(on page 23)*:

1. The triangle in the bottom-right corner provides pin #1 location.
2. FCC ID: 2AAGMGM02SA
3. IC: 12732A-GM02SA
4. IMEI:*XXXXXXXXXXXXXX*
5. S/N:G2P*YYMMDDNNNNSSS* (16 digits)
   - G2P: reserved, value subject to change at Sequans' discretion (3 digits);
   - *YYMMDD*: Manufacturing Date (YY:Year;MM:Month,DD:Day);
   - *NNNN*: Panel counter (from 0001~9999);
   - *SSS*: Piece location on panel (from 001 to 065).
6. 2D marked "a" refer to IMEI Barcode
7. 2D marked "b" refer to S/N Barcode

4.2. Environmental Conditions

GM02S operating conditions:

- Temperature (PCB temperature as measured by on-board thermistor):
  - Operational: -40°C to +85°C;
  - RF compliant: -30°C to +85°C
- Humidity: 10% to 85% (non-condensing)

4.3. Packing

The GM02S is delivered in Tape-and-Reel. Details are provided in the figures below.

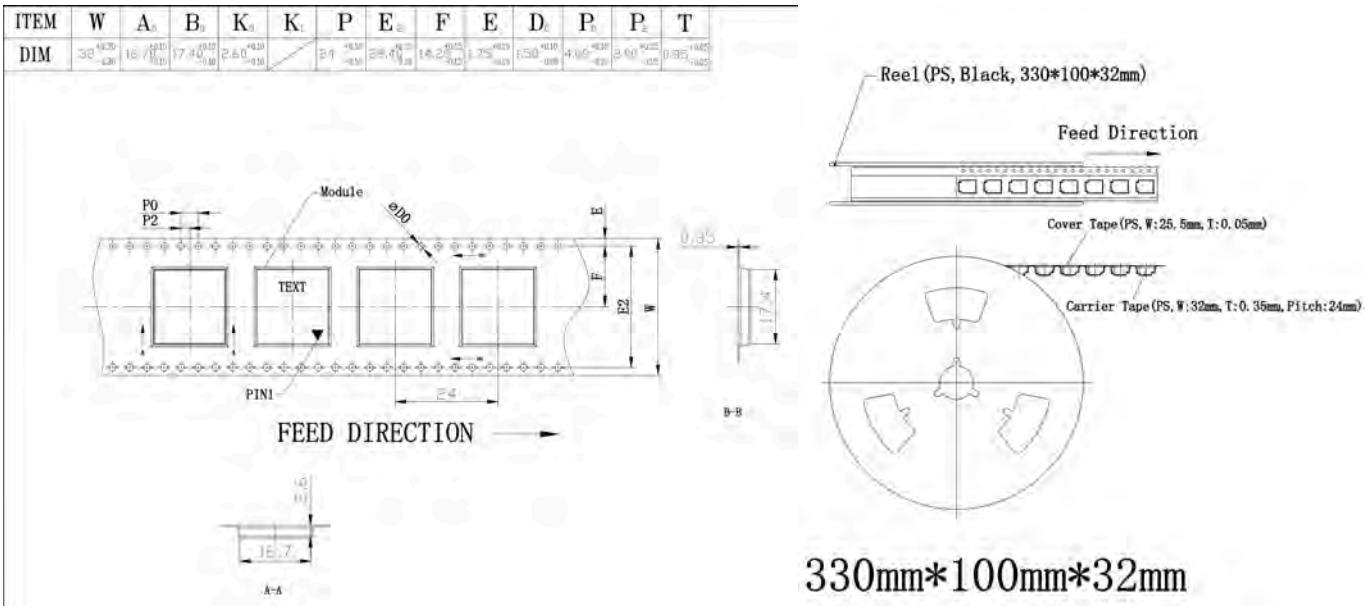

Figure 14. Packing Modules in Reels

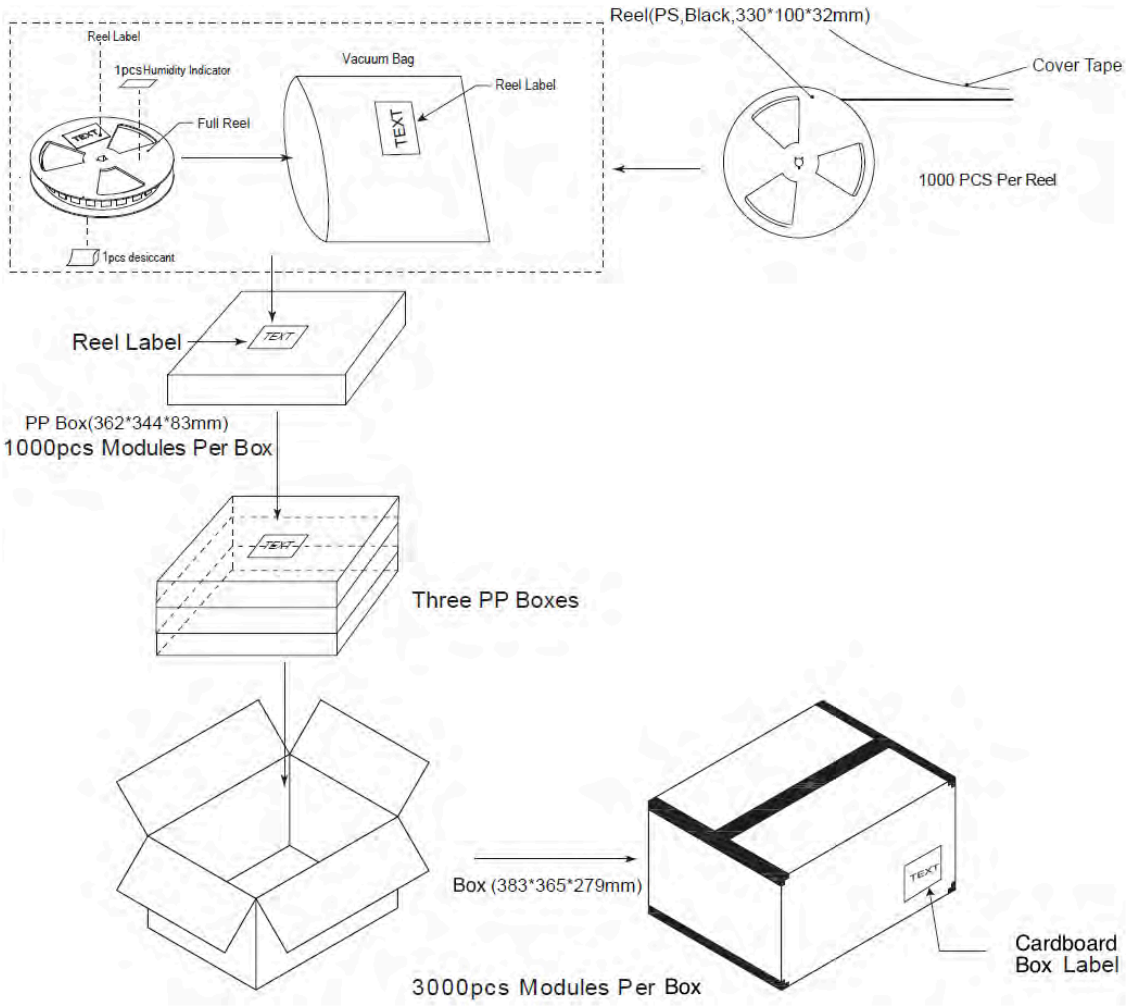

Figure 15. Packing Reels in Boxes

The full box set weights about 5.95 kg.

The label attached to reels, vacuum bags, and the PP boxes is shown in Figure 16: Reel, Vacuum Bag and PP Box Label *(on page 25)*. The label attached to the cardboard box (which contains 3 PP boxes) is shown in Figure 17: Cardboard Box Label *(on page 25)*.

Figure 16. Reel, Vacuum Bag and PP Box Label

Figure 17. Cardboard Box Label

4.4. Storage and Mounting

The GM02S module is Moisture Level 3 rated as per JEDEC industrial standard.

The GM02S is JEDEC J-STD-033D compliant and can be stored at T < 40 °C and relative humidity < 90%.

The GM02S can withstand up to three reflows at a maximum of 250 °C.

Profile Feature	
Solder Paste Alloy	Sn 96.5/Ag 3.0/Cu 0.5 (Lead Free solder paste)
Peak Package Body Temperature	235 °C to 245 °C

Table 31. Reflow Profile

Profile Feature	
Fusion Time	Temp: over 220°C Duration: 60 ~ 90 s
Pre-heat / Soak	Temp: 150 ~ 200 °C Time: 60 ~ 120 s
Ramp-up Rate	< 3 °C/s
Ramp-down Rate	-3 to 0 °C/s
Air composition	N_2, O_2 contents less than 1,500 ppm

Table 31. Reflow Profile (continued)

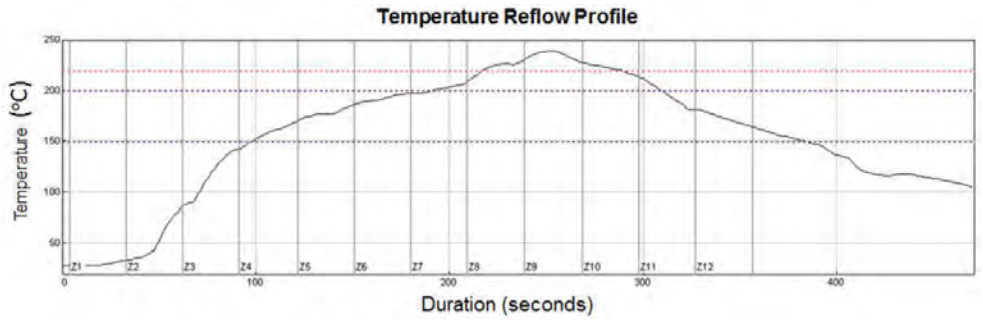

Figure 18. Reflow Profile Parameters

Recommended stencil thickness: 0.1 to 0.13 mm (prefer 0.1 mm). More detail on the PCB land pattern will be provided in a future edition of the document.

Following reflow soldering, the GM02S can be washed with deionised RO water to remove any remaining flux. The module then needs a single backing at 125 °C during 16 hours. The module's package may be slightly discoloured during baking.

4.5. Reliability Specifications for Hardware Rev. 3

The hardware version 3 of the GM02S has been tested against Sequans's industrial reliability specification as described in Table 32: Reliability Test Plan *(on page 26)*.

Item	Test conditions	Standard	#Samples	Result
Preconditioning	(a) Bake: 125°C / 24 hours (b) MSL3: 30°C/60% RH, 192 hrs (c) SAT (CSAM & TSCAN) (d) X-ray (e) Reflow 3 cycles at Tp: 250 ±2°C (f) SAT (CSAM & TSCAN)	JESD22-A113	225	PASS
TC	Temperature Shock Cycling (TC): -40°C to +85°C air to air, 20 minutes, ramp rate 20°C/minute, 1000 cycles	JESD22-A104	25	PASS

Table 32. Reliability Test Plan

Item	Test conditions	Standard	#Samples	Result
THB	Temperature Humidity Bias Test +85°C, 85 % RH, V_{cc} Max, Read Point at 168/500/1,000 hrs	JESD22-A101	25	PASS
HAST	1. 130/100 °C, 85% RH, Vcc max 2. Electrical test	JESD22-A110	25	PASS
Environmental Testing - A Cold	Environmental Testing Test A Cold. -40°C, 500 hrs	IEC60068-2-1 JESD22-A119	25	PASS
Environmental Testing - B Dry Heat	Environmental Testing Test B Dry Heat. +85°C, 500 hrs	IEC60068-2-2 JESD22-A103	25	PASS
HTOL	High Temperature Operating Test 75°C, V_{cc} max, Tx: 50% / Rx: 50%. Read Point at 283/500/1,000 hrs	N/A	50	PASS
LTOL	Low Temperature Operating Test <50°C, V_{cc} max, Tx: 50% / Rx: 50%. Read Point at 283 hrs	JESD22-A108	25	PASS
High Temperature Storage Test (HST)	150 °C/1,000 hours	JESD22-A103	25	PASS
Intermittent Operating Life (IOL)	• Power on/off • 75 °C • 5,000 cycles	N/A	25	PASS
Power and Temperature Cycling	Test Condition A – -40 to +85 °C	JESD22-A105	25	PASS
Shock	Mechanical Shock (MS) (Half Sine, 500G, 1.0 ms, 1 shock for each ±axis)	DIN IEC 68-2-27	15	PASS
Drop	Drop Test: 1. Height: 80 cm; 2. Concrete or steel; 3. All surfaces and edges; 4. 1,500 g / 0.5 ms	DIN IEC 68-2-31 ETS 300019-2-7	15	PASS
Vibration	Vibration Test (Vib) Sweep-Sine Vibration. Sinusoidal, 10 ~ 500 Hz, 1.0 octave/min, 10 sweep cycles for 2 hr for each axis.	DIN IEC 68-2-6 EIA/ TIA 571 §4.1.1.2	15	PASS
ESD	HBM Start: ±1000V, Stop:± 1500V	JS-001JESD22-A114	12	PASS
	CDM Start: ±250V, Stop: ±500V	JS-002STM5.3.1	12	PASS

Table 32. Reliability Test Plan (continued)

Item	Test conditions	Standard	#Samples	Result
TCT	Temperature Change Test 10 cycles; 1 cycle has the following steps (roughly 7+ hrs): • Ramp from ambient (23°C) to -40°C at 3°C/min. • 3 hrs at - 40°C • Ramp to 85°C at 3°C/min • 3 hrs at 85°C • Ramp from 85°C to 23°C at 3°C/min	IEC60068-2-14	25	PASS

Table 32. Reliability Test Plan (continued)

Mean Time To Failure (MTTF)

The MTTF at 60% confidence level is based on the following results/assumptions derived from the 'HTOL' test as described in the table above:

- There was no failure recorded on a cumulative D_h=50,000 hour run (50 devices tested for 1000 hours), which, at a confidence level of 60%, results in a failure rate F_r equal to 0.93.
- Stress test temperature T_s is 75 °C.
- The thermal activation energy E_v is assumed to be 0.7 eV.

The MTTF is given by the following formula: $\text{MTTF} = \frac{A_f \times D_h}{F_r}$ where: $A_f = \exp\left(\frac{E_v}{k}\left(\frac{1}{T_u} - \frac{1}{T_s}\right)\right)$, k being the Boltzmann constant and T_u the usage temperature.

Considering the figures given above, the resulting MTTF for the GM02S at 60% confidence level and a usage temperature T_u of 25°C is 313 years. At a usage temperature T_u of 55°C, this figure drops to 25.9 years.