Technical description

Model: DR263
Description: Smartphone Operated Dalek.
Frequency: 2402MHz – 2480MHz

Technical Description:
The brief circuit description is listed as follows:

The DR263 is a Smartphone Operated Dalek. It is BT version 2.1 + EDR. It can pair with a Bluetooth device as the audio source and control by Dalek's control apps. It operates at frequency range of 2402MHz-2480MHz (79 channels with 1MHz channel spacing). The EUT is powered by internal 6VDC 4 x AA battery.

Antenna Type: Internal integral antenna
Antenna Gain: 0dBi
Nominal rated field strength: 84.7 dBµV/m at 3m
Maximum allowed field strength of production tolerance: +4 to -6dB

U2 – RDA5850 RF IC

U3 – HT9172 DTMF Decoder

U4 - AT9P185A: MCU

Y1- 26 MHz crystal

RDA5850

BLUETOOTH SINGLE CHIP SOLUTION WITH MULTI-MEDIA

Rev.2.1

General Description

RDA5850 is a highly integrated single-chip turnkey Bluetooth radio transceiver and baseband processor with multi-media capability. Bluetooth feature is compliant with Bluetooth 2.1 + EDR specification and provides an optimal solution for data and music application.

1.1 Multi-media Feature

- External SPI Flash interface
- Multi-media Support
  - SBC
  - MP3
  - WMA
  - WAV
- Stereo audio line input
- Supports Serial LCD interface/ LEDs
- Power management
  - Power on reset control
  - Integrated Battery charger
  - Integrated all internal voltage supply from VBAT
- Audio
  - Integrated 1W audio speaker driver
- User Interface
  - supports 3x3 keypad matrix detection
  - Real-time clock
  - I2C
- FM Receiver Integrated
- MMC/SD support
- USB1.2 device only
- IR decode
- ECHO cancel for hands-free
- Voice record
- Bluetooth profiles
  - HFP/HSP
  - OPP
  - A2DP
  - AVRCP

1.2 Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth 2.1 + EDR specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Provides +7dbm transmitting power
- NZIF receiver with -80dBm sensitivity
- Support DCXO with internal oscillator circuit
- Low power consumption

2 Table of Contents

3 Multi-Media SOC Features

Integrating all essential electronic components, including power management, FM receiver onto a single system on chip, RDA5850 offers best in class bill of material, space requirement and cost/feature ratio for complete Bluetooth enabled multi-media system.

Built around a cost effective 32-bit XCPU RISC core running at up to 312MHz with 4k of Instruction cache and 4k of Data cache, RDA5850 offers plenty of processing power for multimedia applications. A high performance proprietary 16/32-bit digital signal processing engine can further improve overall performance and user experience when performing complex multimedia tasks.

It is also packed with impressive connectivity for easy scalability of the system, including SDMMC Memory Cards, Serial LCD and USB (slave, full speed).

3.1 Analog Module

- Differential 13 bit Audio ADC and 16 bit stereo DAC
- 1W stereo loudspeaker amplifier
- Audio line in
- Full Speed USB PHY 1.1

3.2 PMU

- Complete integrated power management system
- Integrated LDO voltage regulators
- Implement both LCD back light and keypad LED drivers

3.3 FM Tuner

- Support worldwide frequency band 65-108MHz
- Digital low-IF tuner
- Fully integrated digital frequency synthesizer
- Autonomous search tuning
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
- Programmable de-emphasis (50/75 ms)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control

3.4 System CPU (XCPU)

- RDA RISC Core
  - 32x32 bits Multiplier Accumulator (MAC)
  - 16/32 bit instruction set
- 4 kByte Instruction Cache
- 4 kByte Data Cache

3.5 Keypad

- 3x3 matrix support with de-bouncing and interrupt generation
- Key On input with de-bouncing and interrupt generation

3.6 SD/MMC Card Controller

- SD Card specification Version 2.0
- SDIO Version 1.10
- MMC specification Version 3.1

3.7 IR Controller

- Support NEC protocol
- User code and key code programmable

3.8 LCD Controller

- SPI interface for LCM
- Max size 128x64

4 Bluetooth Section Features

4.1 Radio

- Build-in TX/RX switch
- Fully integrated synthesizer without any external component
- Class2 and class3 transmit output power supported and over 30dB dynamic control range
- Supports π/4 DQPSK and 8DPSK modulation
- High performance in receiver sensitivity and over 80dB dynamic range
- Integrated channel filter
- Support eSCO and AFH
- Support up to Bluetooth v2.1 + EDR

4.2 Bluetooth Stack

- Compliant with Bluetooth 2.1 + EDR specification
- Profile included AVRCP, A2DP, OPP, HSP/HFP

5 Electrical Characteristics

Table 5-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-20	27	+50	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Notes: 1. VIO=1.8~3.3V

Table 5-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-20		+50	°C
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		VIO+0.3	V
V_{lna}	LNA Input Level			+5	dBm
DC Charger			5	7	V

Notes: 1. VIO=1.8~3.3V

Table 5-3 DC Electrical Specification (Power Supply):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT			3.8	4.2	V
VCORE			1.2	1.4	V
V_BUCK_2V4			2.4		V
ADD_2V4			2.4		V
V_BOOST_4V3			4.3		V
V_RTC			1.2		V
V_USB			3.3		V
V_PAD, V_SPIMEM, V_LCD, V_MMC			2.8	3.0	V

Notes: 1. VIO=1.8~3.3V

6 Bluetooth Section Radio Characteristics

Table 6-1 Receiver Characteristics ------ Basic Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Sensitivity @0.1% BER			/	-80	/	dBm
Maximum received signal@0.1% BER			0	/	/	dBm
C/I c-channel			/	+10	/	dB
Adjacent channel selectivity C/I		F=F0 + 1MHz	/	/	-5	dB
		F=F0 - 1MHz	/	/	0	dB
		F=F0 + 2MHz	/	/	-33	dB
		F=F0 - 2MHz	/	/	-30	dB
		F=F0 + 3 MHz	/	/	-45	dB
		F=F0 - 3MHz	/	/	-40	dB
Adjacent channel selectivity C/I		$F=F_{image}$	/	/	0	dB
Out-of-band blocking performance		30MHz–2000MHz	-10	/	/	dBm
		2000MHz–2400MHz	-27	/	/	dBm
		2500MHz–3000MHz	-27	/	/	dBm
		3000MHz–12.5GHz	-10	/	/	dBm
Intermodulation			-35	/	/	dBm
Spurious output level			-150	/	/	dBm/Hz

Notes:

Table 6-2 Transmit Characteristics ------ Basic Data Rate

(VBAT = 4.0V, TA = 27 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Maximum RF transmit power			/	+4	7	dBm
RF power control range			25	/	/	dB
20dB band width			/	0.9	/	MHz
Adjacent channel transmit power		F=F0 + 1MHz	/	-20	/	dBm
		F=F0 - 1MHz	/	-20	/	dBm
		F=F0 + 2MHz	/	-35	/	dBm
		F=F0 - 2MHz	/	-35	/	dBm
		F=F0 + 3MHz	/	-40	/	dBm
		F=F0 - 3MHz	/	-40	/	dBm
		F=F0 + >3MHz	/	/	-46	dBm

	F=F0 - >3MHz	-46	/	/	dBm
△$f1_{avg}$ Maximum modulation		/	164	/	kHz
△$f2_{max}$ Minimum modulation		/	145	/	kHz
△$f2_{avg}$/△$f1_{avg}$		0.80	/	/	/
ICFT		/	+4	/	kHz
Drift rate		/	0.1	/	kHz/50us
Drift (1 slot packet)		/	-2	/	kHz
Drift (5 slot packet)		/	-2	/	kHz

Notes:

Table 6-3 Receiver Characteristics ------ Enhanced Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
π/4 DQPSK					
Sensitivity @0.01% BER		/	-80	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I c-channel		/	/	+13	dB
Adjacent channel selectivity C/I	F=F0 + 1MHz	/	/	+5	dB
	F=F0 - 1MHz	/	/	0	dB
	F=F0 + 2MHz	/	/	-20	dB
	F=F0 - 2MHz	/	/	-20	dB
	F=F0 + 3MHz	/	/	-40	dB
	F=F0 - 3MHz	/	/	-40	dB
Adjacent channel selectivity C/I	F=F_{image}	/	/	-7	dB
8DPSK					
Sensitivity @0.01% BER		/	-80	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I c-channel		/	/	+18	dB
Adjacent channel selectivity C/I	F=F0 + 1MHz	/	/	+5	dB
	F=F0 - 1MHz	/	/	+5	dB
	F=F0 + 2MHz	/	/	-20	dB
	F=F0 - 2MHz	/	/	-20	dB
	F=F0 + 3MHz	/	/	-35	dB
	F=F0 - 3MHz	/	/	-35	dB
Adjacent channel selectivity C/I	F=F_{image}	/	/	0	dB

Notes:

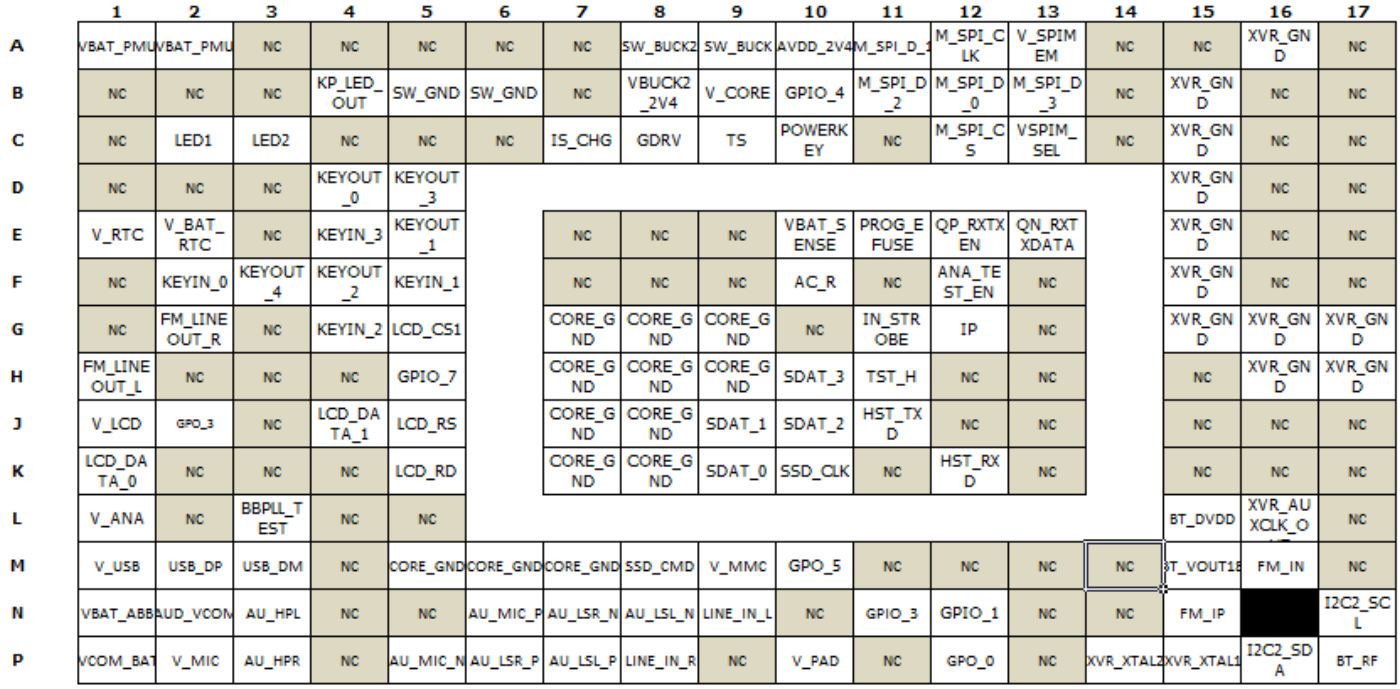
Table 6-4 Transmit Characteristics ------ Enhanced Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications					
Maximum RF transmit power		/	+2	/	dBm
Relative transmit control		/	-1.6	/	dB
					kHz
π/4 DQPSK max w_0		/	+7.4	/	kHz
π/4 DQPSK max w_i		/	+6.7	/	kHz
π/4 DQPSK max $\|w_i + w_0\|$		/	+2.4	/	kHz
8DPSK max w_0		/	+7.1	/	kHz
8DPSK max w_i		/	+4.4	/	kHz
8DPSK max $\|w_i + w_0\|$		/	+2.7	/	kHz
π/4 DQPSK Modulation Accuracy	RMS DEVM	/	4.7	/	%
	99% DEVM	/	/	30	%
	Peak DEVM	/	8.8	/	%
8DPSK Modulation Accuracy	RMS DEVM	/	4.6	/	%
	99% DEVM	/	/	20	%
	Peak DEVM	/	11.3	/	%
In-band spurious emissions	F=F0 + 1MHz	/	-25.0	/	dBm
	F=F0 - 1MHz	/	-25.0	/	dBm
	F=F0 + 2MHz	/	-25.0	/	dBm
	F=F0 - 2MHz	/	-25.0	/	dBm
	F=F0 + 3MHz	/	-30.0	/	dBm
	F=F0 - 3MHz	/	-30.0	/	dBm
	F=F0 +/- > 3MHz	/	/	-32	dBm
EDR Differential Phase Coding		/	100	/	%

Notes:

7 Pins Description



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VBAT_PMU	VBAT_PMU	NC	NC	NC	NC	NC	SW_BUCK2	SW_BUCK	AVDD_2V4	M_SPI_D_1	M_SPI_CLK	V_SPIMEM	NC	NC	XVR_GND	NC
B	NC	NC	NC	KP_LED_OUT	SW_GND	SW_GND	NC	VBUCK2_2V4	V_CORE	GPIO_4	M_SPI_D_2	M_SPI_D_0	M_SPI_D_3	NC	XVR_GND	NC	NC
C	NC	LED1	LED2	NC	NC	NC	IS_CHG	GDRV	TS	POWERKEY	NC	M_SPI_CS	VSPIM_SEL	NC	XVR_GND	NC	NC
D	NC	NC	NC	KEYOUT_0	KEYOUT_3										XVR_GND	NC	NC
E	V_RTC	V_BAT_RTC	NC	KEYIN_3	KEYOUT_1		NC	NC	NC	VBAT_SENSE	PROG_EFUSE	QP_RXTXEN	QN_RXTXDATA		XVR_GND	NC	NC
F	NC	KEYIN_0	KEYOUT_4	KEYOUT_2	KEYIN_1		NC	NC	NC	AC_R	NC	ANA_TEST_EN	NC		XVR_GND	NC	NC
G	NC	FM_LINEOUT_R	NC	KEYIN_2	LCD_CS1		CORE_GND	CORE_GND	CORE_GND	NC	IN_STROBE	IP	NC		XVR_GND	XVR_GND	XVR_GND
H	FM_LINEOUT_L	NC	NC	NC	GPIO_7		CORE_GND	CORE_GND	CORE_GND	SDAT_3	TST_H	NC	NC		NC	XVR_GND	XVR_GND
J	V_LCD	GPO_3	NC	LCD_DATA_1	LCD_RS		CORE_GND	CORE_GND	SDAT_1	SDAT_2	HST_TXD	NC	NC		NC	NC	NC
K	LCD_DATA_0	NC	NC	NC	LCD_RD		CORE_GND	CORE_GND	SDAT_0	SSD_CLK	NC	HST_RXD	NC		NC	NC	NC
L	V_ANA	NC	BBPLL_TEST	NC	NC										BT_DVDD	XVR_AUXCLK_O	NC
M	V_USB	USB_DP	USB_DM	NC	CORE_GND	CORE_GND	CORE_GND	SSD_CMD	V_MMC	GPO_5	NC	NC	NC	NC	BT_VOUT18	FM_IN	NC
N	VBAT_ABB	AUD_VCOM	AU_HPL	NC	NC	AU_MIC_P	AU_LSR_N	AU_LSL_N	LINE_IN_L	NC	GPIO_3	GPIO_1	NC	NC	FM_IP		I2C2_SCL
P	VCOM_BAT	V_MIC	AU_HPR	NC	AU_MIC_N	AU_LSR_P	AU_LSL_P	LINE_IN_R	NC	V_PAD	NC	GPO_0	NC	XVR_XTAL2	XVR_XTAL1	I2C2_SDA	BT_RF

Figure7-1. RDA5850 BGA Ball map (bottom view)

Table 7-1 RDA5850 Pins Description

Pin Name	*I/O*	*Type*	*Usage*	*Power Domain*	*Ball No*
LCD Parallel Interface					
LCD_DATA_0	I/O	D	Data Bus	LCD	K1
LCD_DATA_1	I/O	D	Data Bus	LCD	J4
LCD_RS	O	D	Register Select	LCD	J5
LCD_RD	O	D	Read Strobe	LCD	K5
LCD_CS1	O	D	Chip Select	LCD	G5
External Memory Controller					
M_SPI_CLK	O	D	CLK for SPI flash	MEM	A12
M_SPI_D0	I/O	D	Data0 for SPI flash	MEM	B12
M_SPI_D1	I/O	D	Data1 for SPI flash	MEM	A11
M_SPI_D2	I/O	D	Data2 for SPI flash	MEM	B11
M_SPI_D3	I/O	D	Data3 for SPI flash	MEM	B13
M_SPI_CS	O	D	Chip Select 0 for SPI flash	MEM	C12
I2C2					
I2C2_SCL	I/O	D	I2C2 Clock	STD	N17
I2C2_SDA	I/O	D	I2C2 Data	STD	P16
Memory Card Interface					
SSD_CLK	O	D	SD Clock	MMC	K10
SSD_CMD	I/O	D	SD Command	MMC	M8
SDAT_0	I/O	D	SD data bit 0	MMC	K9
SDAT_1	I/O	D	SD data bit 1	MMC	J9
SDAT_2	I/O	D	SD data bit 2	MMC	J10
SDAT_3	I/O	D	SD data bit 3	MMC	H10
Debug Host					
HST_RXD	I	D	Host data receive.	STD	K12
HST_TXD	O	D	Host data transmit.	STD	J11
KEYPAD					
KEYIN_0	I	D	Key matrix input line 0	STD	F2
KEYIN_1	I	D	Key matrix input line 1	STD	F5
KEYIN_2	I	D	Key matrix input line 2	STD	G4
KEYIN_3	I	D	Key matrix input line 3	STD	E4
KEYOUT_0	O	D	Key matrix output line 0	STD	D4
KEYOUT_1	O	D	Key matrix output line 1	STD	E5
KEYOUT_2	O	D	Key matrix output line 2	STD	F4
KEYOUT_3	O	D	Key matrix output line 3	STD	D5
KEYOUT_4	O	D	Key matrix output line 4	STD	F3

General Purpose I/O					
GPIO_1	I/O	D	GPIO 1	STD	N12
GPIO_3	I/O	D	GPIO 3	STD	N11
GPIO_4	I/O	D	GPIO 4	STD	B10
GPIO_7	I/O	D	GPIO 7	STD	H5
General Purpose Output					
GPO_0	O	D	GPO 0	STD	P12
GPO_3	O	D	GPO 3	STD	J2
GPO_5	O	D	GPO 5	STD	M10
Miscellaneous Pins					
TST_H	ID	D	Test Mode	ANALOG	H11
PLL_TEST	O	D	Digital CLK output for test	ANALOG	L3
USB					
USB_DM	I/O	A	USB D-	ANALOG	M3
USB_DP	I/O	A	USB D+	ANALOG	M2
AUDIO					
AU_MIC_P	I	A	MIC input	ANALOG	N6
AU_MIC_N	I	A	MIC input	ANALOG	P5
AU_HPL	O	A	Headset output L	ANALOG	N3
AU_HPR	O	A	Headset output R	ANALOG	P3
LINE_IN_L	I	A	Stereo Line input	ANALOG	N9
LINE_IN_R	I	A	Stereo Line input	ANALOG	P8
AU_LSL_P	O	A	Loudspeaker Left Out +	ANALOG	P7
AU_LSL_N	O	A	Loudspeaker Left Out -	ANALOG	N8
AU_LSR_P	O	A	Loudspeaker Right Out +	ANALOG	P6
AU_LSR_N	O	A	Loudspeaker Right Out -	ANALOG	N7
VCOM_BAT	I	A	Common mode voltage	ANALOG	P1
AU_VCOM	I	A	Common mode voltage	ANALOG	N2
FM					
FM_LINEOUT_R	O	A	FM audio analog signal output R channel	FM	G2
FM_LINEOUT_L	O	A	FM audio analog signal output L channel	FM	H1
FMIN	I	A	FM RF differential input	FM	M16
FMIP	I	A	FM RF differential input	FM	N15
BT					
BT_RF	O	A	Bluetooth RFIO	BT	P17
BT_DVDD	O	A	Bluetooth DVDD	BT	L15
BT_VOUT18	O	A	Bluetooth VOUT18	BT	M15
Power Management Control					

IN_STROBE	O	A	Analog IN for Test	TEST	G11
IP	O	A	Analog IP for Test	TEST	G12
QP_RXTXEN	I	A	For chip test	TEST	E12
QN_RXTXDATA	I	A	For chip test	TEST	E13
XVR_XTAL1	I	A	26MHz Crystal port Input	TEST	P15
XVR_XTAL2	O	A	26MHz Crystal port Output	TEST	P14
ANA_TEST_EN	I	A	XVR test mode	TEST	F12
XVR_AUXCLK_OUT	O	A	CLK out test pint	TEST	L16
POWERKEY	I	A	Power-on switch enable signal. Active High.	PMU	C10
AC_R	I	A	Input from the AC charger or USB inlet	PMU	F10
GDRV	O	A	Charger drive	PMU	C8
IS_CHG	I	A	Current Sens for Charger Control	PMU	C7
VBAT_SENSE	I	A	Battery voltage ADC detect	PMU	E10
TS	I	A	Battery connection detect	PMU	C9
SW_BUCK	O	A	DC/DC control	PMU	A9
SW_BUCK2	O	A	DC/DC control	PMU	A8
VSPIM_SEL	I	A	Selects V_MEM power supply ('0':2.8V, '1':1.8V).	PMU	C13
PROG_EFUSE	I	A	High voltage input for OTP/EFUSE programming	PMU	E11
LED Drivers					
LED1	I	A	LED driver current sink	PMU	C2
LED2	I	A	LED driver current sink	PMU	C3
POWER					
VBAT_ABB	I	A	Analog Battery Power Supply	ANALOG	N1
AVDD_2V4	O	A	Supplies BT	PMU	A10
VBAT_PMU1	I	A	PMU Battery Power Supply	PMU	A1
VBAT_PMU2	I	A	PMU Battery Power Supply	PMU	A2
V_CORE	O	A	Supplies Core. Out for decoupling / debug / backup	PMU	B9
VBUCK2_2V4	O	A	DCDC power supply	PMU	B8
V_SPIMEM	O	A	Supplies external SPI flash	PMU	A13
V_ANA	O	A	Out for decoupling / debug / backup	PMU	L1
V_PAD	O	A	Supplies Standard PADs I/O ring. Out for decoupling / debug / backup	PMU	P10

V_LCD	O	A	Supplies LCD PADs I/O ring and V_MEM output PAD	PMU	J1
V_MMC	O	A	Supplies MMC PADs I/O ring and V_MEM output PAD	PMU	M9
V_USB	O	A	Supplies USB PHY. Out for debug / backup / decoupling	PMU	M1
V_RTC	O	A	Supplies RTC domain	PMU	E1
V_BAT_RTC	O	A	Charges Backup CAP	PMU	E2
GROUND					
SW_GND		A	DC/DC Switch GND	PMU	B5
SW_GND		A	DC/DC Switch GND	PMU	B6
XVR_GND		A	XVR_GND	PMU	A16
XVR_GND		A	XVR_GND	PMU	B15
XVR_GND		A	XVR_GND	PMU	C15
XVR_GND		A	XVR_GND	PMU	D15
XVR_GND		A	XVR_GND	PMU	E15
XVR_GND		A	XVR_GND	PMU	F15
XVR_GND		A	XVR_GND	PMU	G15
XVR_GND		A	XVR_GND	PMU	G16
XVR_GND		A	XVR_GND	PMU	G17
XVR_GND		A	XVR_GND	PMU	H16
XVR_GND		A	XVR_GND	PMU	H17
CORE_GND		A	CORE_GND	PMU	G7
CORE_GND		A	CORE_GND	PMU	G8
CORE_GND		A	CORE_GND	PMU	G9
CORE_GND		A	CORE_GND	PMU	H7
CORE_GND		A	CORE_GND	PMU	H8
CORE_GND		A	CORE_GND	PMU	H9
CORE_GND		A	CORE_GND	PMU	J7
CORE_GND		A	CORE_GND	PMU	J8
CORE_GND		A	CORE_GND	PMU	K7
CORE_GND		A	CORE_GND	PMU	K8
CORE_GND		A	CORE_GND	PMU	M5
CORE_GND		A	CORE_GND	PMU	M6
CORE_GND		A	CORE_GND	PMU	M7

8 Change List

REV	DATE	AUTHOR	CHANGE DESCRIPTION
V1.0	May 8, 2012	Richard C	Initial version
V2.0	Jun 19, 2012	Richard C	Add Ball map
V2.1	Jun 20,2012	Richard C	Modified according to the latest schematics