Technical Requirements of Tamaggo Sensor PCB V3.1 (IEN0014-07)

Ienso Inc. Feb.15, 2013

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1. RoHS compliant and RoHS assembly process compliant;
2. 8-layer PCB; L1-Top, L2-Layer, L3-Layer, L4-Layer, L5-Layer, L6-Layer, L7-Layer, L8-Bottom; components placed on both of TOP layer and Bottom layer;
3. Via diameter: 14mils; drill hole: 8mils;
4. Traces width: 4mils; clearance: 5mils;
5. Thickness：44mils;
6. Unit dimension：1640mils X 1705mils;
7. Panel pattern：6 units per panel;
8. Surface treatment：gold immersed;
9. Color of solder mask: green;
10. Color of letter strings; white;

11. there is a 7.77mm X 7.77mm square hole in the middle of the PCB board; the 4 edges of square hole should be plated;

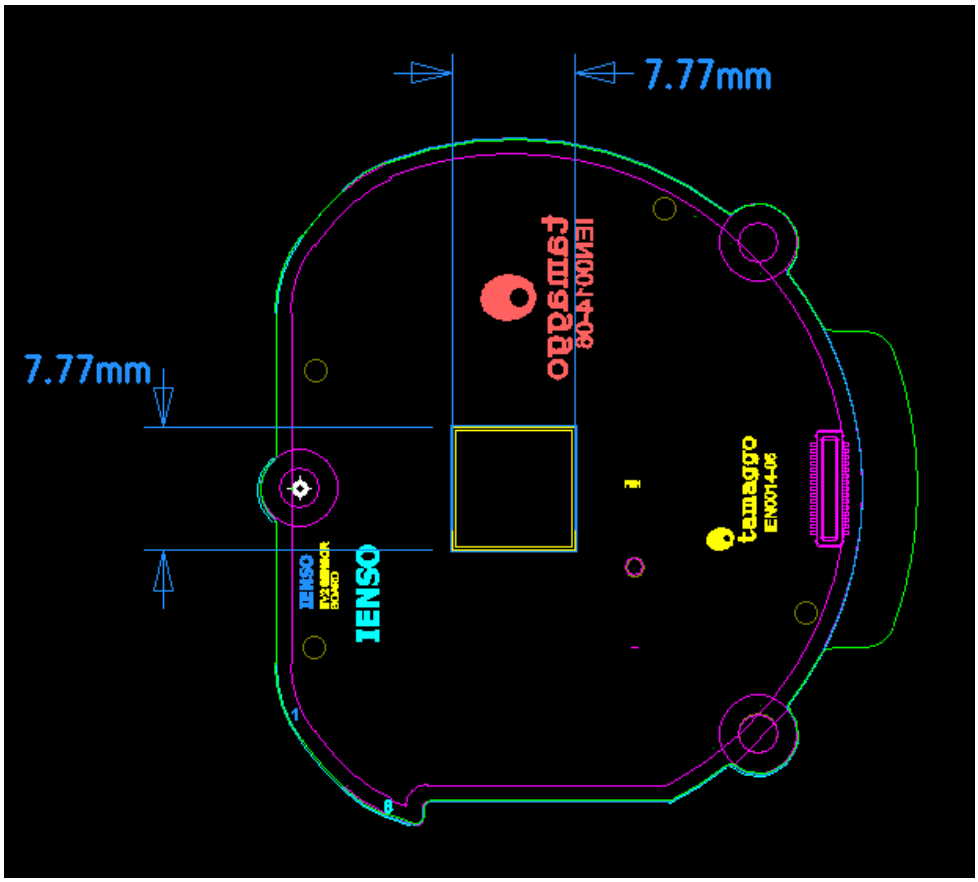


Fig1. a 7.77mm X 7.77mm square hole in the middle

12. Do not be plated the following slot, please refer to the DrillDrawing files for detail;

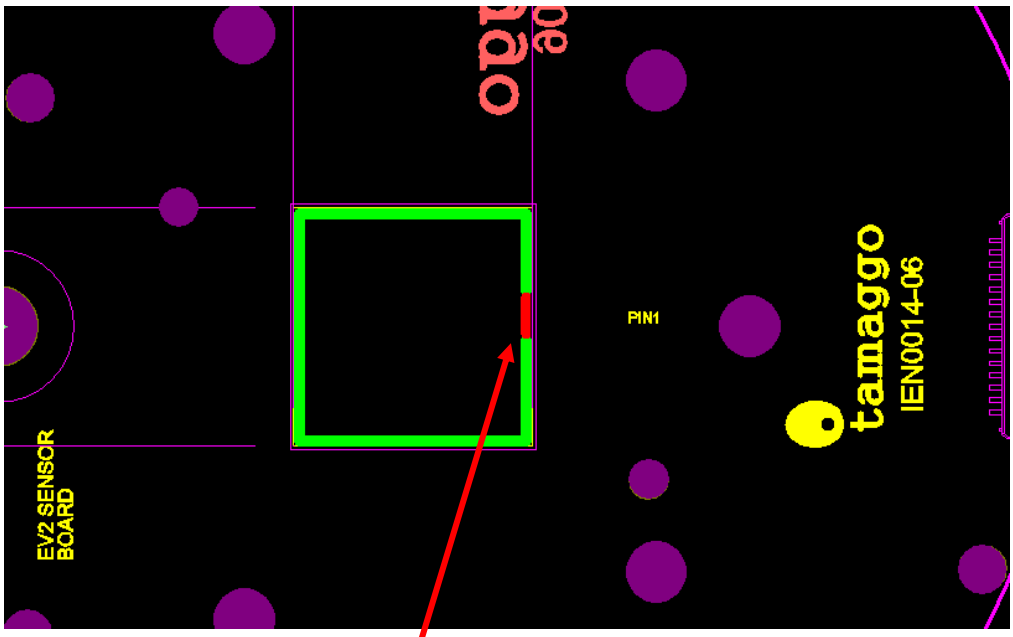


Fig2. Do not be plated the red slot

13 some traces on L3-Layer and L6-Layer need to do impedance control
(a) Impedance is 100 Ohms for differential pairs;, high priority;
(b) Impedance is 50 Ohms for single end high speed signals;
please design the proper layer stack-up to meet the requirement.

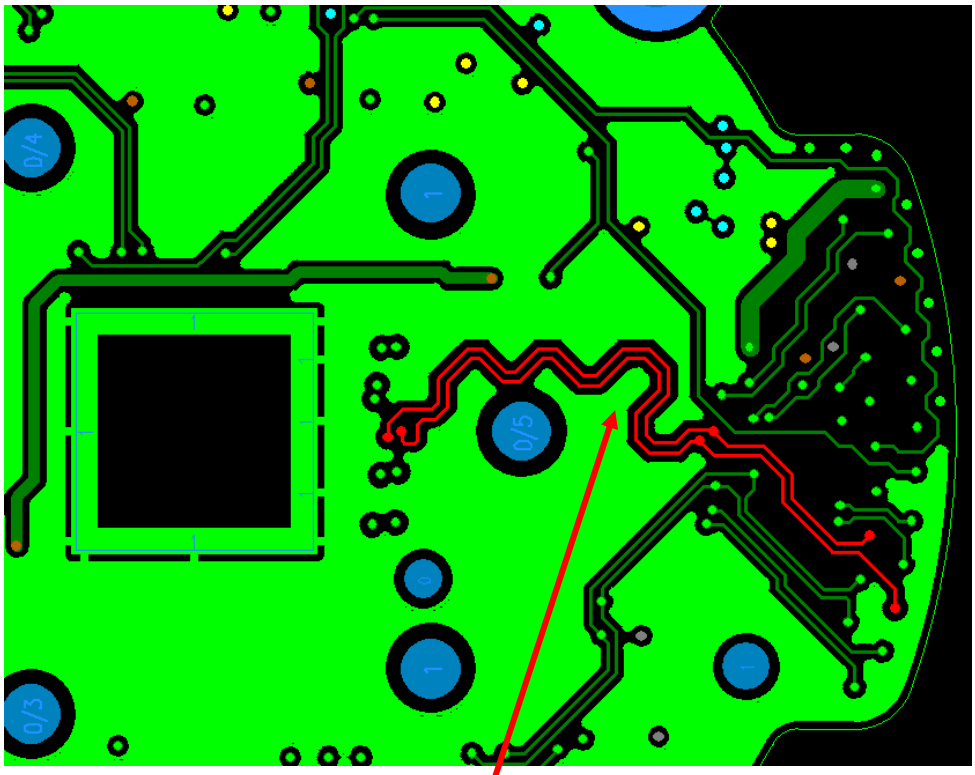


Fig3. impedance controlled high-speed traces

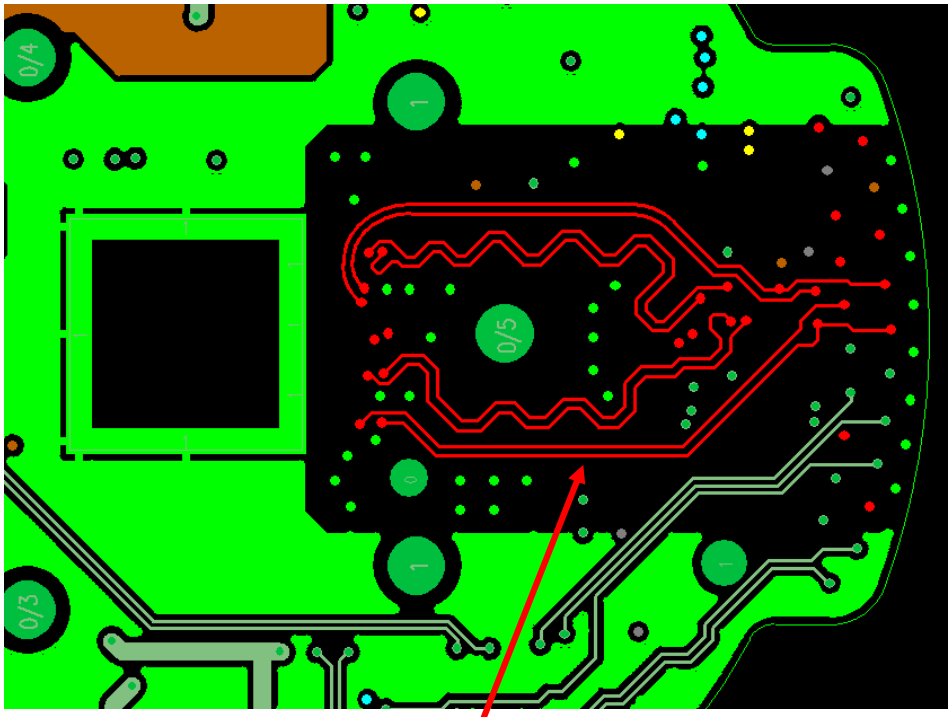
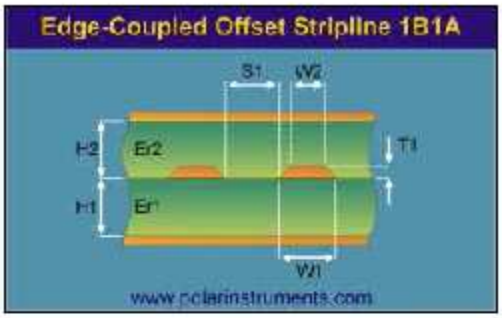


Fig4. impedance controlled high-speed traces

14. Please send the layer stack-up design, including thickness and Er parameters for each layers to us for double-check.
15. Please send the final panel Gerber files back to us for confirmation before PCB fabrication.

[Reference Layer stack-up]

Polar Si8000 Controlled Impedance Quick Solver



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	5.0000	+/-	0.2000	4.8000	5.2000
Substrate 1 Dielectric	Er1	4.0800	+/-	0.2000	3.8800	4.2800
Substrate 2 Height	H2	5.0000	+/-	0.2000	4.8000	5.2000
Substrate 2 Dielectric	Er2	3.9200	+/-	0.2000	3.7200	4.1200
Lower Trace Width	W1	4.0000	+/-	0.2000	3.8000	4.2000
Upper Trace Width	W2	3.0000	+/-	0.2000	2.8000	3.2000
Trace Separation	S1	9.0000	+/-	0.2000	8.8000	9.2000
Trace Thickness	T1	0.7000	+/-	0.1000	0.6000	0.8000

Differential Impedance	Zdiff	98.70	-----	90.47	107.58
Delay (Odd Mode) (ps/in)	D	169.281	-----	173.443	165.012
Odd Mode Impedance	Zodd	49.35	-----	45.24	53.79
Even Mode Impedance	Zeven	51.73	-----	47.25	56.57
Common Mode Impedance	Zcommon	25.86	-----	23.63	28.29

Notes: (First 5 lines will print)

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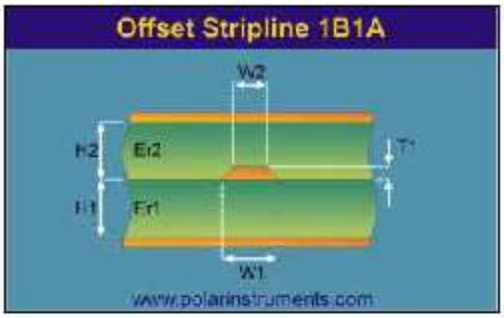

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Impedance	Zo	50.53	-----	46.25	55.18
Delay (ps/in)	D	169.284	-----	173.446	165.015
Inductance (nH/in)	L	8.555	-----	8.021	9.106
Capacitance (pF/in)	C	3.350	-----	3.751	2.990

Notes: (First 5 lines will print)

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