Xinfa Technology Z500-H intelligent module

Product Manual

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Revised Record

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V0.6	1. Updated 1.1 Module storage specifications and part description 2. Updated description in 2.8.2 Remarks 3. Changed 3.1.1 Description and Sorting. 4. Update product model number to Z500-H 5. Update product picture	2023-03-28	De.Cheng

Attention

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catalogue

1. Product overview

1.1 Product Overview

The Z500-H module is a 4G smart module from Xifa Technology, which complies with the 3GPP specification.

- It supports TD-LTE/FDD-LTE/TD-SCDMA/WCDMA/GSM system.
- Support dual-frequency Wi-Fi, BT5.0 short range wireless transmission technology;
- Support GNSS wireless positioning technology;
- Products adopt RF baseband integration design, with high integration, small package size and high reliability characteristics;

Z500-H module contains sub-models of the following regions, which can meet the application requirements of customers in different regions. The modules support a variety of systems and frequency bands. The corresponding systems and frequency bands are as follows:

	Z500-HEU	Z500-HA
Zone	Europe, South America, Korea, Southeast Asia, Australia, India, New Zealand, South Africa	North America
Storage	2GB LPDDR4X+32GB EMMC 3GB LPDDR4X+32GB EMMC 4GB LPDDR4X+64GB EMMC 6GB LPDDR4X+128GB EMMC	2GB LPDDR4X+32GB EMMC 3GB LPDDR4X+32GB EMMC 4GB LPDDR4X+64GB EMMC 6GB LPDDR4X+128GB EMMC

Operating system	Android 13	Android 13
LTE-FDD	B1/2/3/4/5/7/8/20/28	B2/4/5/7/12/13/14/17/25/26/66/71
LTE-TDD	B38/40/41	B38/41
WCDMA	B1/2/4/5/8	B2/4/5
TD-SCDMA	-	-
GSM	850/900/1800/1900	850/1900
WI-FI	2.4 & 5 GHZ, 802.11 a/b/g/n/ac	2.4 & 5 GHZ, 802.11 a/b/g/n/ac
BT	2.1 EDR/3.0 HS/4.2 LE/5.0 LE	2.1 EDR/ 3.0HS / 4.2LE / 5.0LE
GNSS	GPS/Beidou/Glonass /Galileo, four selected three positioning	GPS/Beidou/Glonass /Galileo, four selected three positioning
Coercion/Consistency	Europe: CE	Us: FCC
Other	RoHS/ REACH	RoHS/ REACH

1.2 Key Features

The Z500-H module is designed in LCC+LGA package with a size of only 40.5x40.5x2.8mm. It can run the Android 13 operating system with powerful performance to meet customers' demands for high speed and long life cycle in various business sectors. The module integrates the interface with rich functions, such as LCM, camera, touch screen, microphone, Line Out, UART, USB, I2C and SPI interface, which is suitable for financial intelligent POS, handheld PDA, cash register and other intelligent products.

1.3 Main performance parameters of the module

Performance characteristics	Parameter description
CPU	MT8768, 12nm,Quad-core ARM® Cortex-A53 2.0GHz+ Quad-core ARM® Cortex-53 1.5GHz
GPU	GE8300@650MHZ
Software upgrade	USB/OTA/SD card
Memory	LPDDR4x support up to 6GB EMMC5.1 support
Display interface	1 set of 4data lanes MIPI DSI interfaces supporting up to HD+(20:9) 1600*720@60fps
Camera ports	2 sets of 4data lanes MIPI CSI-2 interfaces - Maximum single group 21MP@30fps is supported - Support up to two groups of 13MP+8MP@30fps - Support YUV422/YUV420/EXIF/JFIF format

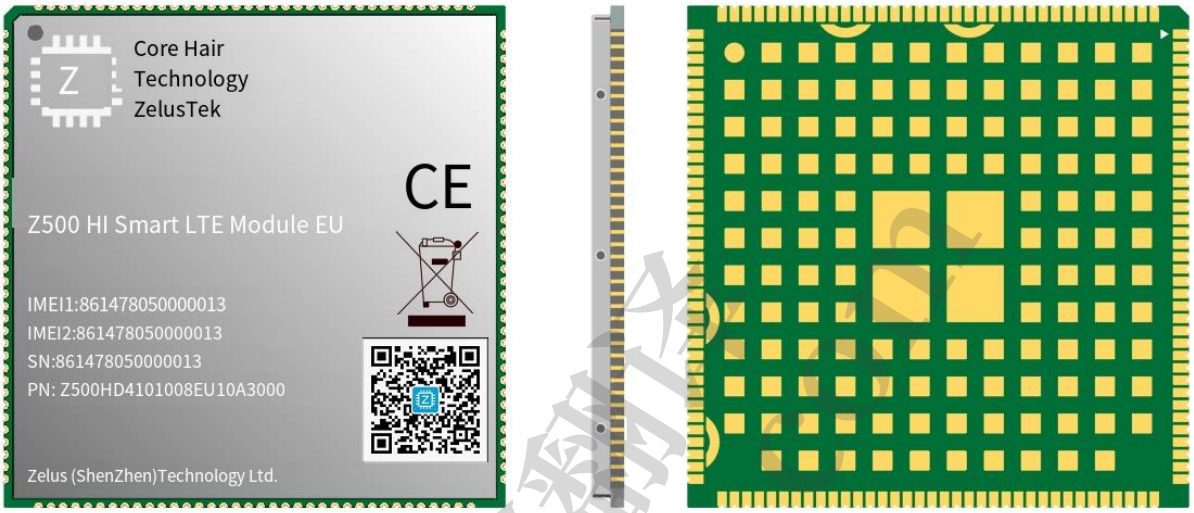
Analog audio interface	Audio input: - Integrated Mic bias output within the module -3 sets of analog microphone inputs (MIC0/MIC2 configurable DMIC) Audio output (power amplifier is not supported within the module) : -1 set of single ended stereo output with a maximum output of 0.93Vrms(S.E.)@32Ω -1 set of differential Line out output, maximum output 1.88Vrms-vd@600Ω -1 differential line out,1.87Vrms-vd@32Ω
Digital I2S audio interface	I2S2 Rx IF -Master mode -1 data wires =>Up to 2-CHs -24bits up to 192KHz(Master) I2S1 Tx IF -Master mode -1 data wires =>Up to 2-CHs -24bits up to 192KHz
USB port	USB2.0 High Speed (HS) with a maximum data transfer rate of 480Mbps - Support OTG mode
(U)SIM port	2 sets of (U)SIM ports support 1.8V/3.3V adaptive - Support dual SIM card dual standby (single pass), support hot swap
SD card interface	1 group of SD card interfaces that do not support the SDIO protocol but support SD/SDHC/MS/MSPRO/MMC - Supports up to 256GB
UART interface	1 set of four-wire functional UART supporting RTS/CTS hardware flow control (UART1) 1 set of 2 wire debug UART, can do function serial port (UART0) -FIFO RX/TX independent FIFO, Max 8K byte - Baud rate 110bps~3844800bps (default 961200)
I2C interface	6 sets of I2C, supporting 100KHz standard mode and 400KHz high speed mode
SPI interface	5 groups of hardware SPIs - Maximum clock rate 27MHz - Minimum data rate 0.8K bit/s - Maximum data rate 27M bit/s
ADC interface	2 Auxiliary ADC sets - Input range 0.05~1.45V -12-bits

	-Sampling rate 3.25/(N+8)MSPS@N-bit
RTC Clock	Support
Antenna interface	Main antenna, DRX antenna, Wi-Fi/BT/GNSS antenna

1.4 RF performance parameters

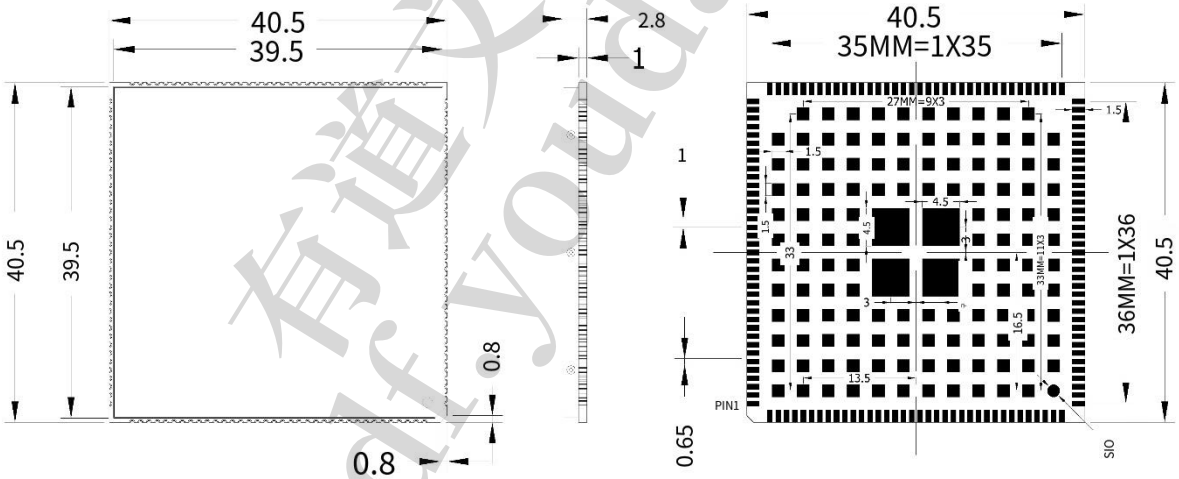
Performance characteristics	Parameter description
Power level	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm+1/-2.7dB) for LTE-FDD bands Class 3 (23dBm+1/-2.7dB) for LTE-TDD bands
GSM/GPRS/EDGE features	R99: CSD transfer rate: 9.6kbps, 14.4kbps GPRS: Supports GPRS multi-slot class 12 Encoding format: CS-1/CS-2/CS-3 and CS-4 Each frame has a maximum of 4 Rx slots EDGE: EDGE multi-slot class 12 is supported GMSK and 8-PSK are supported Uplink encoding formats: CS 1-4 and MCS 1-9 Downstream encoding formats: CS 1-4 and MCS 1-9
WCDMA features	Support for 3GPP R9 Support 16-QAM\QPSK modulation CAT7 HSUPA: Maximum uplink speed 11Mbps CAT14 CAT7 HSDPA: Maximum downstream speed 21Mbps
LTE features	Support for 3GPP R10 Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth downstream support for 2 x 2 MIMO Maximum uplink speed is 50Mbps and maximum downlink speed is 150Mbps
Short message (SMS)	Text and PDU modes point-to-point MO and MT short message cell broadcast

1.5 Product appearance



1.6 Structural dimensions

Module package LCC+LGA 275PIN, size: 40.5mmx40.5mmx2.8mm



Module TOP view size (Unit: mm) Module BOT view size (Unit: mm)

1.7 Module conduction data

1.7.1 EU Edition conducts data

Transmitted power:

Mode	Frequency band	Maximum power (dBm)	Minimum power (dBm)
GSM	850 (GMSK)	33 + 2	5 + 5
	900 (GMSK)	33 + 2	5 + 5
	1800 (GMSK)	30 + 2	0 + / - 5
	1900 (GMSK)	30 + 2	0 + / - 5

GSM	850 (8PSK)	27.0 + / - 3	5 + 5
	900 (8PSK)	27.0 + / - 3	5 + 5
	1800 (8PSK)	26.0 + / - 3	0 + / - 5
	1900 (8PSK)	26.0 + / - 3	0 + / - 5
WCDMA	Band 1	24 + 1/3	< - 49
	Band 2	24 + 1/3	< - 49
	Band 4	24 + 1/3	< - 49
	Band 5	24 + 1/3	< - 49
	Band 8	24 + 1/3	< - 49
LTE FDD	Band 1	23.0 + / - 2	< - 39
	Band 2	23.0 + / - 2	< - 39
	Band 3	23.0 + / - 2	< - 39
	Band 4	23.0 + / - 2	< - 39
	Band 5	23.0 + / - 2	< - 39
	Band 7	23.0 + / - 2	< - 39
	Band 8	23.0 + / - 2	< - 39
	Band 20	23.0 + / - 2	< - 39
	Band 28	23.0 + / - 2	< - 39
LTE TDD	Band 38	23.0 + / - 2	< - 39
	Band 40	23.0 + / - 2	< - 39
	Band 41	23.0 + / - 2	< - 39

Reception sensitivity: to be updated

System	Frequency band	Master set antenna	Diversity antenna	3 GPP standard	Units
GSM	850	- 110.	NA	102.4	dBm
	900	- 111.	NA	102.4	dBm
	1800	- 109.	NA	102.4	dBm
	1900	- 109.	NA	102.4	dBm
WCDMA	Band 1	- 111.	NA	106.7	dBm
	Band 2	- 111.	NA	104.7	dBm

	Band 4	- 111.	NA	106.7	dBm
	Band 5	- 111.	NA	104.7	dBm
	Band 8	- 111.	NA	103.7	dBm
LTE FDD	Band 1 (10MHZ)	98.7	100.1	96.3	dBm
	Band 2 (10MHZ)	99.7	98.9	94.3	dBm
	Band 3 (10MHZ)	99.4	- 100.	93.3	dBm
	Band 4 (10MHZ)	99.8	100.5	96.3	dBm
	Band 5 (10 MHZ)	- 100.	99.7	94.3	dBm
	Band 7 (10MHZ)	97.3	- 98.	94.3	dBm
	Band 8 (10 MHZ)	- 100.	100.6	93.3	dBm
	Band 20 (10MHZ)	99.6	100.2	93.3	dBm
	Band 28 (10MHZ)	- 100.	99.8	94.8	dBm
LTE TDD	Band 38 (10MHZ)	97.9	- 99.	96.3	dBm
	Band 40 (10MHZ)	96.7	100.1	96.3	dBm
	41 (10 MHZ Band,	97.7	98.9	94.3	dBm

1.7.2A version of the data transmission

Transmitted power:

Mode	Frequency band	Maximum power (dBm)	Minimum power (dBm)
GSM	850(GMSK)	33 + 2	5 + 5
	1900(GMSK)	30 + 2	0 + / - 5
GSM	850(8PSK)	27.0 + / - 3	5 + 5
	1900(8PSK)	26.0 + / - 3	0 + / - 5
WCDMA	Band 2	24 + 1/3	< - 49
	Band 4	24 + 1/3	< - 49
	Band 5	24 + 1/3	< - 49
LTE FDD	Band 2	23.0 + / - 2	< - 39
	Band 4	23.0 + / - 2	< - 39
	Band 5	23.0 + / - 2	< - 39
	Band 7	23.0 + / - 2	< - 39
	Band 12	23.0 + / - 2	< - 39
	Band 13	23.0 + / - 2	< - 39
	Band 14	23.0 + / - 2	< - 39
	Band 17	23.0 + / - 2	< - 39
	Band 25	23.0 + / - 2	< - 39
	Band 26	23.0 + / - 2	< - 39
	Band 66	23.0 + / - 2	< - 39

	Band 71	23.0 + / - 2	< - 39
LTE TDD	Band 38	23.0 + / - 2	< - 39
	Band 41	23.0 + / - 2	< - 39

Reception sensitivity:

System	Frequency band	Master set antenna	Diversity antenna	3GPP standard	Units
GSM	850	- 110.	-	102.4	dBm
	1900	109.5	-	102.4	dBm
WCDMA	Band 2	110.5	-	104.7	dBm
	Band 4	109.5	-	106.7	dBm
	Band 5	- 111.	-	104.7	dBm
LTE FDD	Band 2 (10MHZ)	99.7	99.8	94.3	dBm
	Band 4 (10MHZ)	- 100.	99.7	96.3	dBm
	Band 5 (10MHZ)	99.1	98.6	94.3	dBm
	Band 7 (10MHZ)	96.8	97.3	94.3	dBm
	Band 12 (10MHZ)	98.4	98.9	93.3	dBm
	Band 13 (10MHZ)	98.1	99.4	93.3	dBm
	Band 14 (10MHZ)	99.1	100.5	93.3	dBm
	Band 17 (10MHZ)	98.6	98.7	93.3	dBm
	Band 25 (10MHZ)	99.3	99.4	92.8	dBm
	Band 26 (10MHZ)	99.5	99.2	93.8	dBm
	Band 66 (10MHZ)	97.3	99.2	95.8	dBm
	Band 71 (10MHZ)	99.2	- 99.	93.5	dBm
LTE TDD	Band 38 (10MHZ)	97.9	- 99.	96.3	dBm
	Band 41 (10MHZ)	97.7	98.9	94.3	dBm

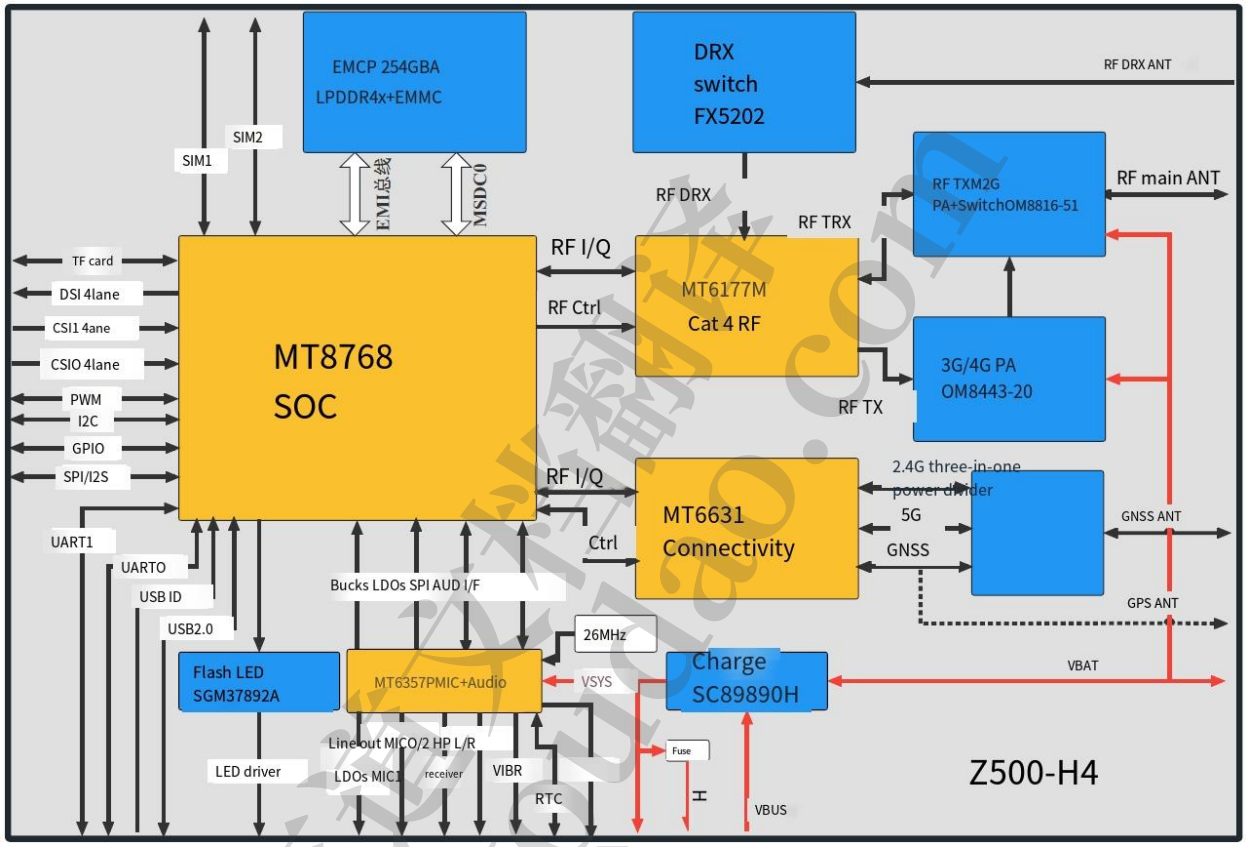
1.8 Operating and storage temperature

project		Specifications	Remarks
Work environment	Operating temperature	-35℃ ~ +75℃	

Storage environment	Storage temperature	-40℃ to 90℃	
Protection class		/	
Environmental certification		RoHS	

2. Hardware introduction

2.1 Hardware architecture



2.2 RF band

2.2.1A version of the spectrum

Frequency Bands	Uplink(UL)	Downlink(DL)	Unit	Duplex Mode
GSM	850		MHz	
GSM	1900		MHz	
WCDMA B2	1852 ~ 1908	1932 ~ 1988	MHz	
WCDMA B4	1712 ~ 1753	2112 ~ 2153	MHz	
WCDMA B5	824 ~ 849	869 ~ 894	MHz	
LTE B2	1850 ~ 1910	1930 ~ 1990	MHz	FDD
LTE B4	1710 ~ 1755	2110 ~ 2155	MHz	FDD
LTE B5	824 ~ 849	869 ~ 894	MHz	FDD
LTE B7	2500 ~ 2570	2620 ~ 2690	MHz	FDD
LTE B12	699 ~ 716	729 ~ 746	MHz	FDD
LTE B13	777 ~ 787	746 ~ 756	MHz	FDD
LTE B14	788 ~ 798	758 ~ 768	MHz	FDD
LTE B17	704 ~ 716	734 ~ 746	MHz	FDD
LTE B25	1850 ~ 1915	1930 ~ 1995	MHz	FDD
LTE B26	814 ~ 849	859 ~ 894	MHz	FDD
LTE B66	1710 ~ 1780	2110 ~ 2200	MHz	FDD

LTE B71	663 ~ 698	617 ~ 652	MHz	FDD
LTE B38	2570 ~ 2620	2570 ~ 2620	MHz	TDD
LTE B41	2535 ~ 2655	2535 ~ 2655	MHz	TDD

2.2.2 GNSS operating frequency

Type	Frequency
GPS	1575.42 + / - 1.023 MHz
Glonass	1597.5 ~ 1605.8 MHz
Beidou	1561.098 + / - 2.046 MHz
Galileo	1575.42 + / - 1.023 MHz

2.2.3 GNSS receiving mode

GNSS receive at the same time	GPS/Glonass/Beidou
	GPS/Glonass/Galileo
	GPS/Beidou/Galileo

2.2.4 RF data transfer rate

FDD-LTE	Uplink(UL)	50Mbps
	Downlink(DL)	150Mbps
TDD-LTE	Uplink(UL)	30Mbps
	Downlink(DL)	117Mbps
UMTS	HSUPA Uplink(UL)	5.76 Mbps
	DC-HSDPA Downlink(DL)	21Mbps
	WCDMA Uplink(UL)	384Kbps
	WCDMA Downlink(DL)	384Kbps
GPRS	Uplink(UL)	85.6 Kbps
	Downlink(DL)	85.6 Kbps
EDGE	Uplink(UL)	236.8 Kbps
	Downlink(DL)	236.8 Kbps

2.3 Wi-Fi performance metrics

Transmit power:

frequency	System	rate	Bandwidth (MHz)	Transmission power (dBm)
2.4 G	802.11 b	1Mbps	20	17 + 3
		11Mbps	20	17 + 3
	802.11 g	6Mbps	20	16 plus or minus 3
		54Mbps	20	13 + / - 3

	802.11 n	MCS0	20	15 + / - 3
		MCS7	20	13 + / - 3
5G	802.11 a	6Mbps	20	15 + / - 3
		54Mbps	20	13 + / - 3
	802.11 n	MCS0	20	15 + / - 3
		MCS7	20	13 + / - 3
	802.11 n	MCS0	40	15 + / - 3
		MCS7	40	13 + / - 3
	802.11 ac	MCS0	20	15 + / - 3
		MCS8	20	12 + 2
	802.11 ac	MCS0	40	15 + / - 3
		MCS9	40	12 + 2
	802.11 ac	MCS0	80	15 + / - 3
		MCS9	80	12 + 2

Receiving sensitivity:

Frequency	System	Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4 G	802.11 b	1Mbps	20	- 92.
		11Mbps	20	- 85.
	802.11 g	6Mbps	20	- 90.
		54Mbps	20	73.5
	802.11 n	MCS0	20	87.5
		MCS7	20	- 72.
5G	802.11 a	6Mbps	20	- 92.
		54Mbps	20	75.5
	802.11 n	MCS0	20	- 90.
		MCS7	20	71.5
	802.11 n	MCS0	40	- 87.
		MCS7	40	68.5
	802.11 ac	MCS0	20	92.5
		MCS8	20	- 71.
	802.11 ac	MCS0	40	- 87.
		MCS9	40	- 69.
	802.11 ac	MCS0	80	- 86.
		MCS9	80	- 64.

2.4 Bluetooth performance Indicators

Type	DH-5	2-DH5	3-DH5	BLE	Units
Transmitted power	9.5	2.5	2.5	5.27	dBm
The sensitivity	- 90.	89.5	83.5	1M:-85 2M:-83 S=2:-86 2 = 8: - 85	dBm

2.5 GNSS conduction data

Characteristics of the	Description	Typical values	Units
Sensitivity	Cold start	147	dBm
	Reacquisition	157	dBm
	Tracking	156	dBm
TTFF	Cold start	33.7	S
	Warm start	6.6	S
	Hot start	1.2	S
Static Drift	CEP-50	0.7	m

2.6 Antenna specifications

2.6.1 RF antenna specifications

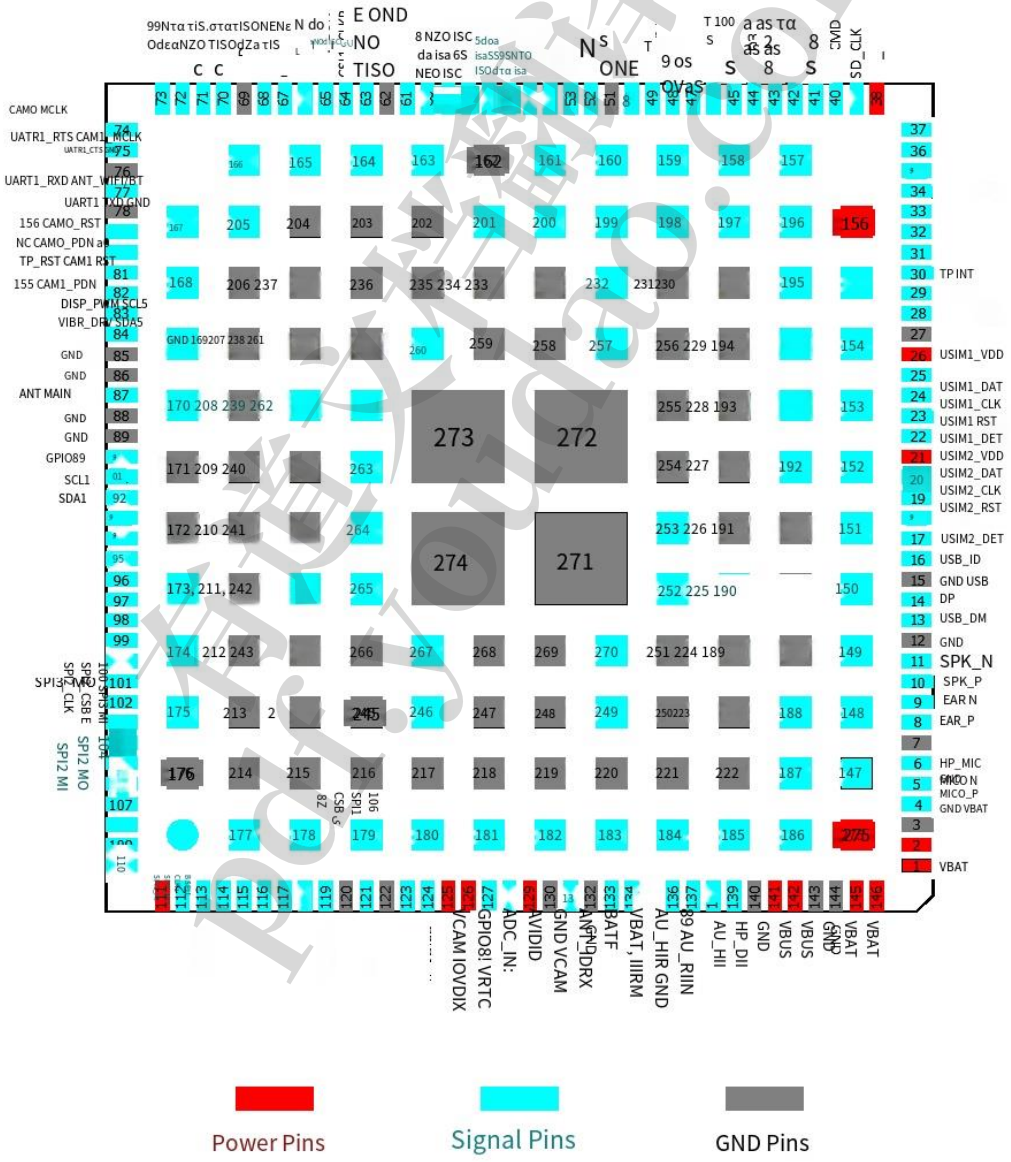
Parameter	Requirements
Operating Frequency	See 2G/3G/4G *Operating Frequency*
Direction	Omni Directional
Gain	> -3dBi(Avg)
Impedance	50 Ω
Efficiency	> 50%
Max. Input Power	50W
VSWR	< 2
Isolation	20dB is preferred
Cable Insertion Loss <1GHz	< 1dB
Cable Insertion Loss 1GHz to 2.2GHz	< 1.5dB
Cable Insertion Loss 2.3GHz to 2.7GHz	< 2dB
Cable Insertion Loss 3.3GHz to 6GHz	< 2.5dB

2.6.2 GNSS antenna specifications

Parameter	Requirement
Operating Frequency	1559~1609MHZ
Direction	Hemisphere, face to sky
Antenna Gain	> 2dB
Impedance	50 Ω
Efficiency	> 50%

Max. Input Power	50W
VSWR	< 2
Polarization	RHCP or Linear
Noise Figure for Active Antenna	< 1.5
Total Gain for Active Antenna	< 17 dB
Cable Insertion Loss	< 1.5 dB

2.7 Module PIN assignment



Module PIN distribution map (TOP perspective)

2.8 Module PIN definition

2.8.1 Distribution of the Pin definition

1	VBAT	93	UART0_RXD	185	ADC_IN3
2	VBAT	94	UART0_TXD	186	GPIO172
3	GND	95	VOL+	187	CS_N
4	MIC0_P	96	VOL-	188	CS_P
5	MIC0_N	97	GPIO10	189	GND
6	HP_MIC	98	GPIO9	190	GND
7	GND	99	SPI3_CSB/I2S2_BCK	191	GND
8	EAR_P	100	SPI3_CLK/I2S2_DI	192	VCAMD_PMU
9	EAR_N	101	SPI3_MO/I2S2_LRCK	193	VLDO28_PMU
10	SPK_P	102	SPI3_MI/I2S2_MCK	194	GPIO_GPS_LNA_EN
11	SPK_N	103	SPI2_CSB	195	CHG_LED
12	GND	104	SPI2_CLK	196	CSI0_CLKP
13	USB_DM	105	SPI2_MO	197	CSI0_LN0P
14	USB_DP	106	SPI2_MI	198	CSI0_LN1P
15	GND	107	SPI1_CSB/I2S1_BCK	199	CSI0_LN2P
16	USB_ID	108	SPI1_CLK/I2S1_DO	200	CSI0_LN3P
17	USIM2_DET	109	SPI1_MO/I2S1_LRCK	201	GPIO168
18	USIM2_RST	110	SPI1_MI/I2S1_MCK	202	GND
19	USIM2_CLK	111	VIO18_PMU	203	GND
20	USIM2_DAT	112	GPIO150	204	GND
21	USIM2_VDD	113	GPIO151	205	SDA2
22	USIM1_DET	114	PWRKEY	206	GND
23	USIM1_RST	115	GPIO3	207	GND
24	USIM1_CLK	116	SPI0_CLK	208	GND
25	USIM1_DAT	117	SPI0_CSB	209	GND
26	USIM1_VDD	118	SPI0_MO	210	GND
27	GND	119	SPI0_MI	211	GND
28	VIBR_DRV	120	GND	212	GND
29	DISP_PWM	121	ANT_GNSS	213	GND
30	TP_INT	122	GND	214	GND
31	TP_RST	123	GPIO88	215	GND
32	NC	124	GPIO160	216	GND
33	GPIO6	125	VCAM_IOVDD	217	GND
34	UART1_TXD	126	VRTC	218	GND
35	UART1_RXD	127	GPIO87	219	GND
36	UART1_CTS	128	ADC_IN2	220	GND
37	UART1_RTS	129	VCAM_AVDD	221	GND
38	SD_VDD	130	GND	222	GND
39	SD_CLK	131	ANT_DRX	223	GND
40	SD_CMD	132	GND	224	GND

41	SD_D0	133	BAT_P	225	SYSRSTB
42	SD_D1	134	VBAT_THERM	226	GND
43	SD_D2	135	GND	227	GND
44	SD_D3	136	AU_HPR	228	GND
45	SD_DET	137	AU_REFN	229	GND
46	USB_BOOT	138	AU_HPL	230	GND
47	SCL0	139	HP_DET	231	GND
48	SDA0	140	GND	232	GPIO164
49	LCD_RST	141	VBUS	233	GND
50	DSI_TE	142	VBUS	234	GND
51	GND	143	GND	235	GND
52	DSI_CKN	144	GND	236	GND
53	DSI_CKP	145	VBAT	237	GND
54	DSI_D0N	146	VBAT	238	GND
55	DSI_D0P	147	MICBIAS0	239	GPIO169
56	DSI_D1N	148	MIC2_P	240	GND
57	DSI_D1P	149	MIC2_N	241	GND
58	DSI_D2N	150	NC	242	SPI4_CSB
59	DSI_D2P	151	VCDT	243	GND
60	DSI_D3N	152	NC	244	GND
61	DSI_D3P	153	GPIO7	245	GND
62	GND	154	GPIO8	246	NC
63	CSI1_CLKN	155	MICBIAS1	247	GND
64	CSI1_CLKP	156	VIO28_PMU	248	GND
65	CSI1_D0N	157	CSI0_CLKN	249	LED_B
66	CSI1_D0P	158	CSI0_LN0N	250	GND
67	CSI1_D1N	159	CSI0_LN1N	251	GND
68	CSI1_D1P	160	CSI0_LN2N	252	LED_G
69	GND	161	CSI0_LN3N	253	LED_R
70	CSI1_D3N	162	GND	254	NC
71	CSI1_D3P	163	GPIO107	255	GND
72	CSI1_D2N	164	GPIO109	256	GND
73	CSI1_D2P	165	GPIO108	257	NC
74	CAM0_MCLK	166	SCL2	258	GND
75	CAM1_MCLK	167	SCL3	259	GND
76	GND	168	SDA3	260	BPI_BUS5
77	AN_WI-FI/BT/GNSS	169	SCL4	261	GND
78	GND	170	SDA4	262	BPI_BUS6
79	CAM0_RST	171	GND	263	NC
80	CAM0_PDN	172	GND	264	SPI4_MO
81	CAM1_RST	173	BPI_BUS7	265	SPI4_MI
82	CAM1_PDN	174	NC	266	GND
83	SCL5	175	NC	267	GPIO152

84	SDA5	176	GND	268	GND
85	GND	177	GPIO165	269	GND
86	GND	178	GPIO176	270	SPI4_CLK
87	ANT_MAIN	179	GPIO167	271	GND
88	GND	180	FLASH_LED	272	GND
89	GND	181	NFC_CLK	273	GND
90	GPIO89	182	GPIO166	274	GND
91	SCL1	183	NC	275	VSYS
92	SDA1	184	VPH_PWR		

2.8.2 Pin Function Description

Pin name	Pin number	Electrical characteristics	Pin function Description	Remarks
Power port				
VBUS	141142	Input	USB VBUS/ charging power input	The input ranges from 5 to 12V
VBAT	1,2,145,146	Input/output	Battery interface	Support high voltage battery 4.35V
VCDT	151	Input	VBUS detects partial voltage interruption	Refer to VCDT divider shunt resistor design
VIO18_PMU	111	Output	System 1.8V I/O power supply	Cannot be used to power external devices Can only be used for IO pull-up level
VIO28_PMU	156	output	System 2.8V I/O power supply	Cannot be used to power external devices Can only be used for IO pull-up level
VPH_PWR	184	The output	VSYS output power supply	Max output 1000mA
VSYS	275	Input/output	VSYS power supply	Access system power when using the external charging feature
VLDO28_PMU	193	output	2.8V LDO power supply	2.8/3.0 V @ 400 ma
VRTC	126	Input/Output	RTC clock power supply	Max 3.3V@2mA
VCAM_IOVDD	125	Output	1.8V power supply for MIPI camera	1.8V@300mA, cannot be used for other purposes
VCAM_AVDD	129	Output	MIPI camera simulates power supply	1.8/2.5/2.7/2.8/3.0/2.9/2.95 V @ 200 ma default 2.8 V output, can't do other purposes

VCAMD_PMU	192	Output	MIPI Camera Digital power supply	1.0/1.05/1.1/1.2 V @ 300 ma Default 1.2V output, cannot be used for other purposes
GND	3,7,12,15 27,51,62,6 9,76,78,85 ,86,88,89, 120,122,13 0,132,135, 140,143,14 4,162,171, 172,176,18 9,190 1912022032 0420620720 8209210211 2122132142 1521621721 8219220221 2222232242 26 2272282292 3023123323 4235236237 2382402412 4324424524 7248250251 2552562582 59 2612662682 6927127227 3274	Ground wire	Ground wire	
Battery interface				
CS_P	188	Input	PMIC internal coulommeter sampling positive	The CS_P/N series is grounded with 0 ohm resistance when not using the internal coulommeter
CS_N	187	The input	PMIC internal coulommeter sampling negative	
BAT_P	133	Input	PMIC internal ADC sampling	Input voltage 2.5~4.5V
VBAT_THERM	134	Input	Battery NTC sampling	Default: NTC=10K+/ -1% B - Constant (25 ° C - 50 ° C) (K)

				=3380K +/-3% or +/-1% Input range is 0.1 to 2.8V
CHG_LED	195	Output	Charge indicator control	Connect the negative pole of the LED light and turn on at a low level by default
Analog audio interface				
MICBIAS0	147	Output	MIC0/MIC2 offset voltage	
MIC0_P	4	Input	Analog MIC0 input positive terminal	
MIC0_N	5	Input	Analog MIC0 input negative terminal	
MIC2_P	148	Enter	Analog MIC2 input positive terminal	
MIC2_N	149	Input	Simulate MIC2 input negative terminal	
EAR_P	8	Output	Differential handset outputs positive terminal	
EAR_N	9	Output	Differential handset output negative	
SPK_P	10	Output	Difference line out the output positive terminal	An external power amplifier inputs the positive terminal
SPK_N	11	output	Output negative differential line out	Connect the external power amplifier to the input negative
AU_HPR	136	Output	Headphones simulate right track output	
AU_REFN	137	Enter	Input the earphone reference ground	Earphone single point loop reference
AU_HPL	138	Output	Headphones simulate left track output	
HP_DET	139	Enter	Headset plug and unplug detection	The default high level indicates earphone insertion
HP_MIC	6	Enter	Headphones simulate MIC input	
MICBIAS1	155	Output	Headphones simulate MIC bias voltage	
USB port				
VBUS	141142	Input/output	USB VBUS/ charging power input	The input ranges from 5 to 12V
USB_DM	13	Data IO	USB2.0 Data DM	

USB_DP	14	Data IO	USB2.0 data DP	
USB_ID	16	Enter	USB OTG mode switch	Default hardware pull up 100K resistors inside the module
USIM				
USIM1_DET	22	Input	SIM card 1 Hot swap detection interrupt	USIM_VDD 1.7/1.8/1.86/2.76/3.0/3.1 V @ 200 ma default 1.86 V Two sets of SIM card signals should only be used for SIM card purposes and not for other purposes
USIM1_RST	23	Output	SIM Card 1 Reset the output	
USIM1_CLK	24	Output	SIM Card 1 Clock output	
USIM1_DAT	25	Data IO	SIM Card 1 Data	
USIM1_VDD	26	Output	SIM card 1 Power output	
USIM2_DET	17	Enter	SIM card 2 hot plug detection	
USIM2_RST	18	Output	SIM card 2 Reset the output	
USIM2_CLK	19	Output	SIM Card 1 Clock output	
USIM2_DAT	20	Data IO	SIM Card 1 Data	
USIM2_VDD	21	Output	SIM card 1 Power output	
SD Card				
SD_VDD	38	Output	SD card power output	3.3/2.9/3.0 V @ 800 ma Default 3.0V
SD_CLK	39	Output	SD card clock output	
SD_CMD	40	Output	SD card command output	
SD_D0	41	Data IO	SD card data IO	
SD_D1	42	Data IO	SD card data IO	
SD_D2	43	Data IO	SD card data IO	
SD_D3	44	Data IO	SD card data IO	
SD_DET	45	Data IO	SD card hotplug detection	TF card detection, low level insertion by default
MIPI display interface				
DSI_CKN	52	Output	DSI differential clock negative	
DSI_CKP	53	Output	DSI differential clock positive	
DSI_D0N	54	Output	DSI Differential data 0 negative	
DSI_D0P	55	Output	DSI differential data 0 positive terminal	
DSI_D1N	56	Output	DSI Differential Data 1 negative	
DSI_D1P	57	Output	DSI Differential Data 1 positive	

DSI_D2N	58	Output	DSI Differential Data 2 negative	
DSI_D2P	59	Output	DSI differential data 2 positive electrode	
DSI_D3N	60	The output	DSI Differential Data 3 negative	
DSI_D3P	61	The output	DSI Differential Data 3 positive	
LCD_RST	49	Output	MIPI Screen reset output	1.8V I/O level
DSI_TE	50	input	MIPI screen Tearing Effect input	
DISP_PWM	29	Output	Main display backlight PWM control	
Camera 1 interface				
CSI1_CLKN	63	Output	CSI1 Differential clock negative	
CSI1_CLKP	64	The output	CSI1 Differential clock positive	
CSI1_D0N	65	Enter	CSI1 Differential Data 0 negative	
CSI1_D0P	66	Input	CSI1 Differential data 0 positive	
CSI1_D1N	67	Enter	CSI1 Differential Data 1 negative	
CSI1_D1P	68	The input	CSI1 Differential Data 1 positive	
CSI1_D2N	72	Input	CSI1 Differential Data 2 negative	
CSI1_D2P	73	Input	CSI1 Differential Data 2 positives	
CSI1_D3N	70	Input	CSI1 Differential Data 3 Negative	
CSI1_D3P	71	Input	CSI1 Differential Data 3 positives	
CAM1_MCLK	75	Output	Camera sensor master clock output	Default 24MHz
CAM1_RST	81	Output	Camera sensor reset output	1.8 V I/O level
CAM1_PDN	82	Output	Camera sensor Enables output	
Camera 0 interface				
CSI0_CLKN	157	output	CSI0 differential clock negative	
CSI0_CLKP	196	Output	CSI0 differential clock positive	

CSI0_LN0N	158	Input	CSI0 Differential data 0 negative	
CSI0_LN0P	197	Input	CSI0 Differential data 0 positive pole	
CSI0_LN1N	159	Input	CSI0 Differential Data 1 negative	
CSI0_LN1P	198	Input	CSI0 Differential Data 1 positive	
CSI0_LN2N	160	Input	CSI0 Differential Data 2 negative	
CSI0_LN2P	199	Input	CSI0 Difference Data 2 positive	
CSI0_LN3N	161	Input	CSI0 Differential Data 3 negative	
CSI0_LN3P	200	Input	CSI0 Differential Data 3 positive	
CAM0_MCLK	74	Output	Camera sensor master clock output	Default 24MHz
CAM0_RST	79	Output	Camera sensor reset output	1.8V I/O level
CAM0_PDN	80	The output	Camera sensor Enables output	
Camera flash interface				
FLASH_LED	180	Output	FLASH LED light positive output	Maximum driving current 700mA
Capacitive touch screen interface				
SCL0	47	Output	I2C0 clock output	
SDA0	48	Data IO	I2C0 Data I/O	
TP_INT	30	Enter	Touch screen interrupt input	
TP_RST	31	Output	Touch screen reset output	
UART interface				
UART1_TXD	34	Output	UART1 data Send	
UART1_RXD	35	Input	UART1 Data reception	
UART1_CTS	36	output	UART1 Data Request	
UART1_RTS	37	Enter	UART1 Data Answer	
UART0_RXD	93	Input	UART0 data reception	Default system debug, can support functional UART
UART0_TXD	94	Output	UART0 data send	
I2C interface				
SCL1	91	Output	I2C1 clock output	
SDA1	92	Data IO	I2C1 data I/O	
SCL2	166	Output	I2C2 clock output	
SDA2	205	Data IO	I2C2 data I/O	

SCL3	167	Output	I2C6 Clock Output	Compatible Z600-H motherboard must do external pull-up resistor, Z500 fixed for I2C function
SDA3	168	Data IO	I2C6 Data I/O	
SCL4	169	The output	I2C4 Clock Output	
SDA4	170	Data IO	I2C4 Data I/ OS	
SCL5	83	Output	I2C5 Clock output	
SDA5	84	Data IO	I2C5 Data I/O	
SPI interface				
SPI0_CSB	117	Output	SPI1 piece select output	
SPI0_CLK	116	output	SPI1 clock output	
SPI0_MO	118	Output	SPI1 data output	
SPI0_MI	119	The input	SPI1 data entry	
SPI1_CSB	107	The output	SPI4 selected output	Reuse I2S1_OUT
SPI1_CLK	108	Output	SPI4 clock output	
SPI1_MO	109	Output	SPI4 data output	
SPI1_MI	110	Input	SPI4 data entry	
SPI2_CSB	103	Output	SPI2 piece select output	
SPI2_CLK	104	The output	SPI2 clock output	
SPI2_MO	105	Output	SPI2 data output	
SPI2_MI	106	Enter	SPI2 data entry	
SPI3_CSB	99	Output	SPI3 piece select output	Reuse I2S0_IN
SPI3_CLK	100	Output	SPI3 clock output	
SPI3_MO	101	Output	SPI3 data output	
SPI3_MI	102	Input	SPI3 data entry	
SPI4_CSB	242	Output	SPI4 piece select output	
SPI4_CLK	270	The output	SPI4 clock output	
SPI4_MO	264	Output	SPI4 data output	
SPI4_MI	265	The input	SPI4 data entry	
I2S output interface				
I2S3_MCK	110	Output	I2S master clock output	Multiplexing SPI1
I2S3_LRCK	109	Output	I2S or so clock output	
I2S3_BCK	107	Output	I2S bit clock output	
I2S3_DO	108	The output	I2S data output	
I2S input interface				
I2S0_MCK	102	Output	I2S master clock output	Multiplexing SPI3
I2S0_LRCK	101	Output	I2S or so clock output	
I2S0_BCK	99	The output	I2S bit clock output	
I2S0_DI	100	Input	I2S data input	

ADC interface				
ADC_IN2	128	Input	ADC analog sampling input	The input ranges from 0.05 to 1.45V
ADC_IN3	185	Input	ADC analog sampling input	The input ranges from 0.05 to 1.45V
Button interface				
PWRKEY	114	Input	On-off key input	The level equals VBAT voltage
VOL+	95	Input	Volume + key signal input	
VOL-	96	The input	The volume - key signal input	
USB_BOOT	46	The input	Force upgrade key input	Enter high level to enter upgrade mode
SYSRSTB	225	input	System reset signal input	
LED status light				
LED_R	253	Output	LED light negative	It is recommended to add current limiting resistance to the positive LED pole of the motherboard
LED_G	252	Output	LED light negative	
LED_B	249	Output	LED light negative	
Motor interface				
VIBR_DRV	28	Output	Vibration motor positive	1.2 V / 1.3 V / 1.5 V / 1.8 V / 2.0 V / 2.8 V / 3.0 V / 3.3 V @ 200 ma, the default 2.8 V output
Antenna port				
AN_WI-FI/BT/GNSS	77	Input/output	WI-FI/BT/GNSS 3-in-1 antenna	Default 3-in-1 antenna
ANT_GNSS	121	Input	GNSS stand-alone antenna	Default NC
ANT_MAIN	87	Input/output	RF main set antenna	
ANT_DRX	131	Input	RF diversity antenna	
RF Tuner control interface				
BPI_BUS5	260	Output	Antenna Tuner switch control	Tuner switch is special, can't do other purposes
BPI_BUS6	262	Output	Antenna Tuner switch control	
BPI_BUS7	173	Output	Antenna Tuner switch control	
External GPS LNA enabled				

GPIO91	194	Output	The mainboard GPS LNA can control	GPS active power supply "is special, can't do other purposes
GPIO interface				
GPIO166	182	Input/output		
GPIO165	177	Input/output		
GPIO176	178	Input/Output		
GPIO167	179	Input/output		
GPIO89	90	Input/output		
GPIO10	97	Input/Output		
GPIO3	115	Input/output		
GPIO88	123	Input/output		
GPIO160	124	Input/output		
GPIO87	127	Input/Output		
GPIO7	153	Input/Output		
GPIO8	154	Input/Output		
GPIO172	186	Input/Output		
GPIO168	201	Input/Output		
GPIO164	232	Input/Output		
GPIO169	239	Input/Output		
GPIO152	267	Input/output		
GPIO107	163	Input/output		
GPIO109	164	Input/output		
GPIO108	165	Input/output		
Other features				
NFC_CLK	181	The output	Clock output	

NC	In 32150, 152174175 183246254 257263			

2.9 Electrical parameters

2.9.1 Power supply characteristics

Parameter	Description	Min	Type	Max	Unit
VBAT	Power Supply	3.5	3.8	4.4	V
I_{peak}	Peak current			3000	mA
I_{sleep}	Current in sleep mode			TBD	mA
$I_{leakage}$	Current in power off mode			TBD	uA

2.9.2 I/O electrical characteristics

Voltage Domain	Parameter	Min	Type	Max
VOH	High level output	1.35 V	1.8 V	1.98 V
VOL	Low level output	0V	-	0.45 V
VIH	High level input	1.26 V	1.8 V	1.98 V
VIL	Low level input	0V	-	0.54 V

2.9.3 Module power consumption

To be updated

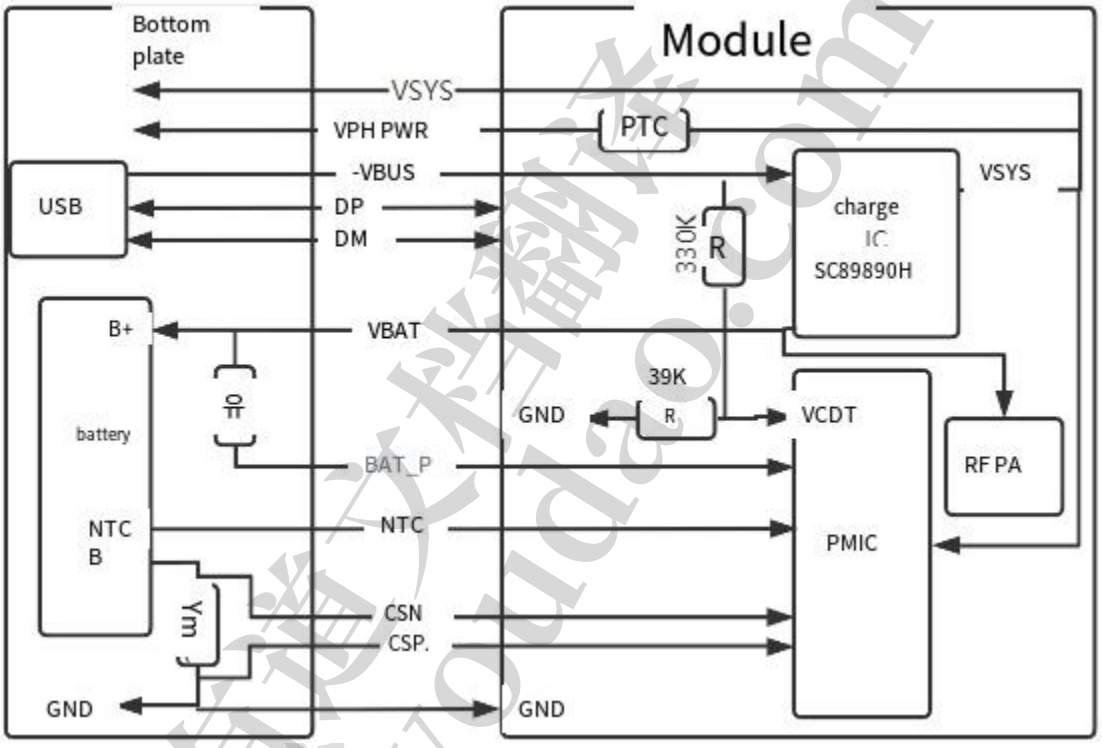
Parameter	Description	Conditions	Typ.	Unit
I_{BAT}	OFF state	Power down		uA
	Sleep state			

3. Hardware interface design

3.1 Power interface design

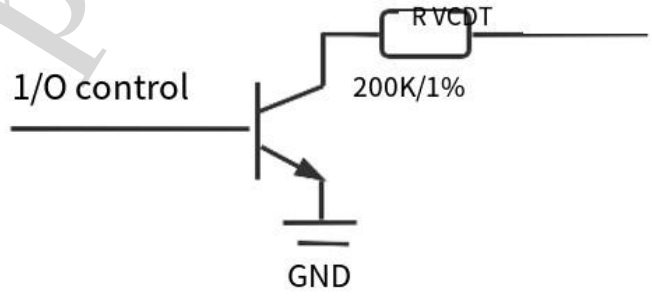
- Charging module contains functions that can be compatible with external and internal battery design, internal default module with the function of charging;
- Module internal VPH_PWR output capacity of 1000 ma.

- Module internal charging function supports single-cell battery, the default NTC resistance of the battery side is 10K;
- Suggest Mr 10 sampling resistor placed near the battery interface, CSN/CSP current sampling (coulometer) signal design difference stereo package;
- BAT_P voltage sampling should be connected to a single point close to the battery interface, the input voltage range is 2.5-4.5V;



Module internal charging IC design

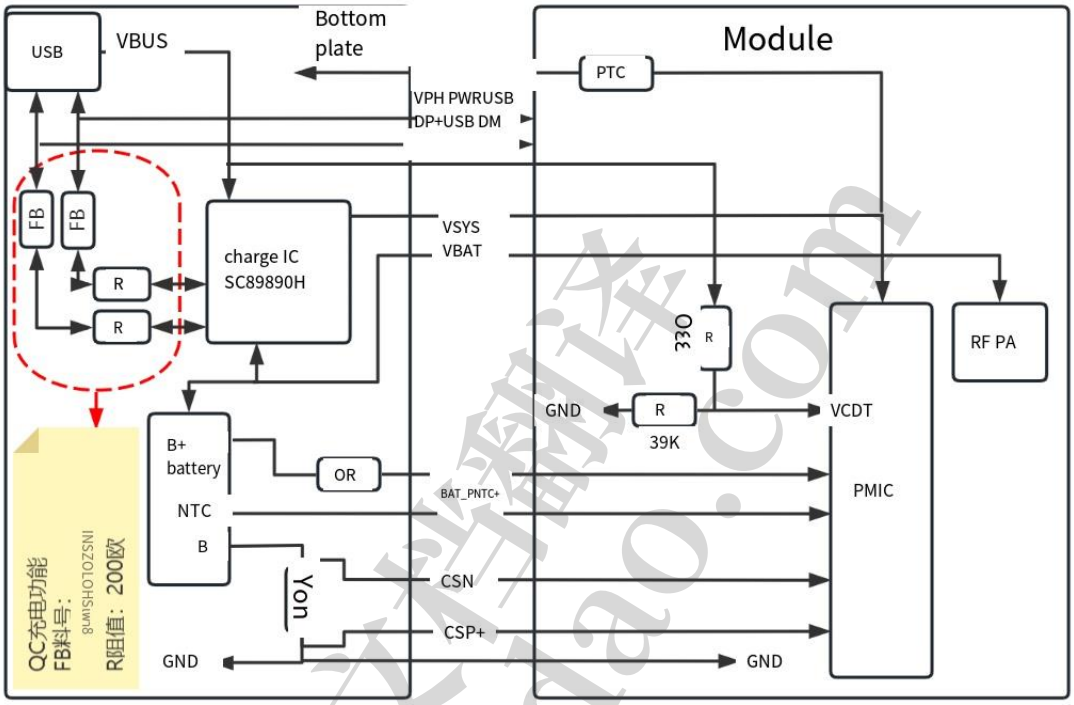
- VBUS 5 ~ 12 V input voltage range, shutdown condition VBUS default input is greater than 10.5 V (VCDT HW OVP value of 10.5 V), the need to increase VCDT partial pressure shunt resistance design;



VCDT partial voltage shunt resistance design

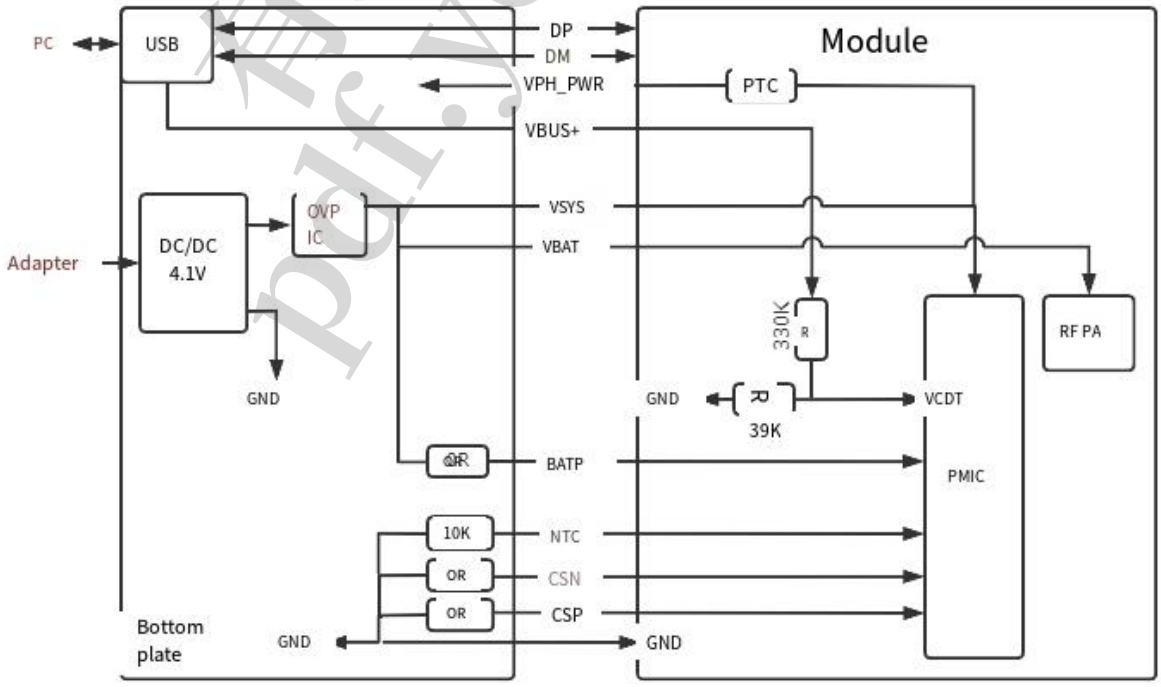
- When the motherboard does QC charging function, USB (DP/DM) signal PCB wiring needs to take Daisy chain form, USB signal wiring can not produce branch, avoid

signal reflection, data transmission is unstable;



Motherboard charging function design

- The design of no-charge function must add OVP protection at the input end of VBAT&VSYS, and the protection voltage is < 4.45V;
- The VBAT&VSYS input voltage range is 3.5V~4.35V@3000mA, typical value is 3.8V;

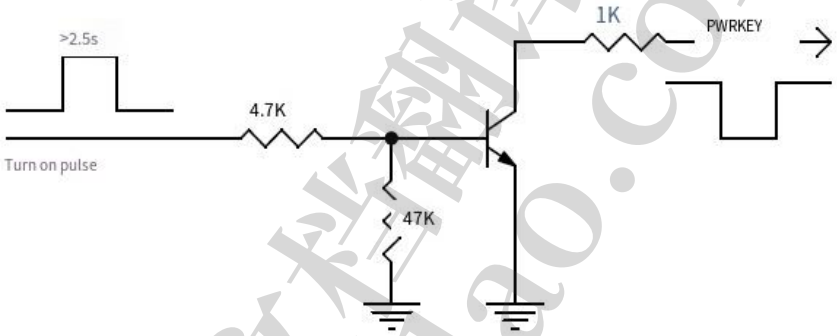


No charging function design

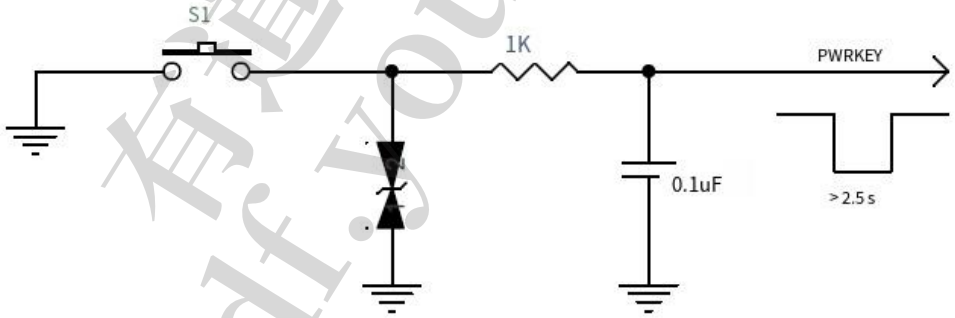
3.2 Module switch machine control

3.2.1 Module power on

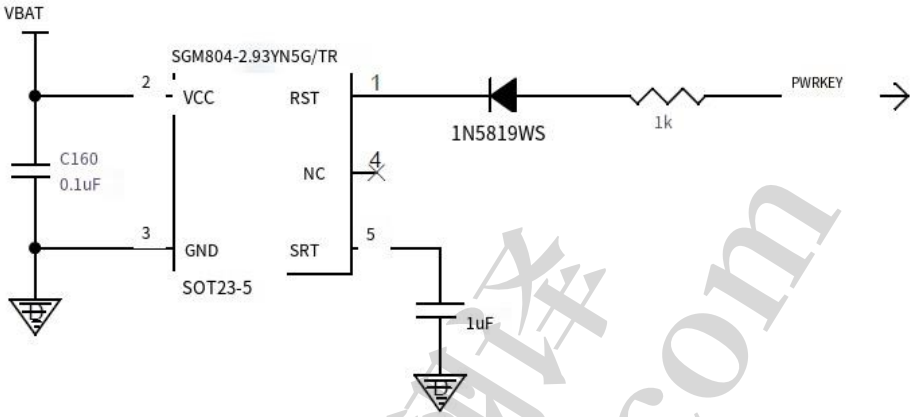
- After the VBAT is powered on, pull down the PWRKEY for at least 2.5 seconds to turn the module on;
- PWRKEY signal PMIC internal pull up to VBAT voltage, motherboard can not be connected to the pull resistance;
- After the PWRKEY signal is turned on, it needs to return to the high level and cannot be pulled down all the time (it will shut down or restart);



Power-on mode 1



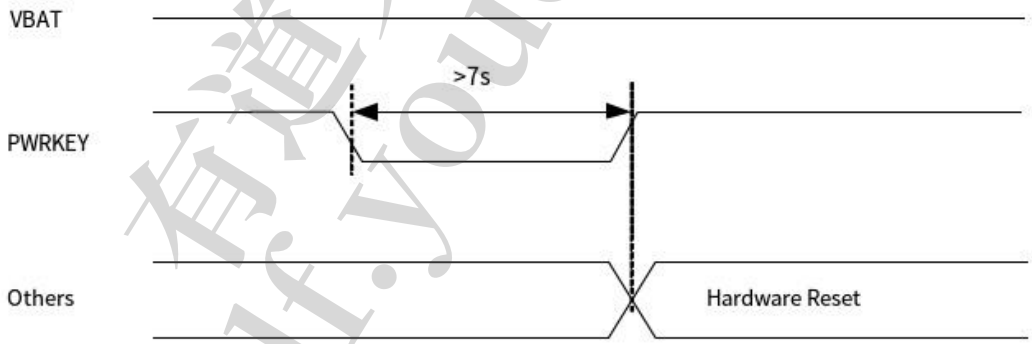
Boot mode 2



Boot Method 3 (Power on automatically)

3.2.2 Module to turn it off

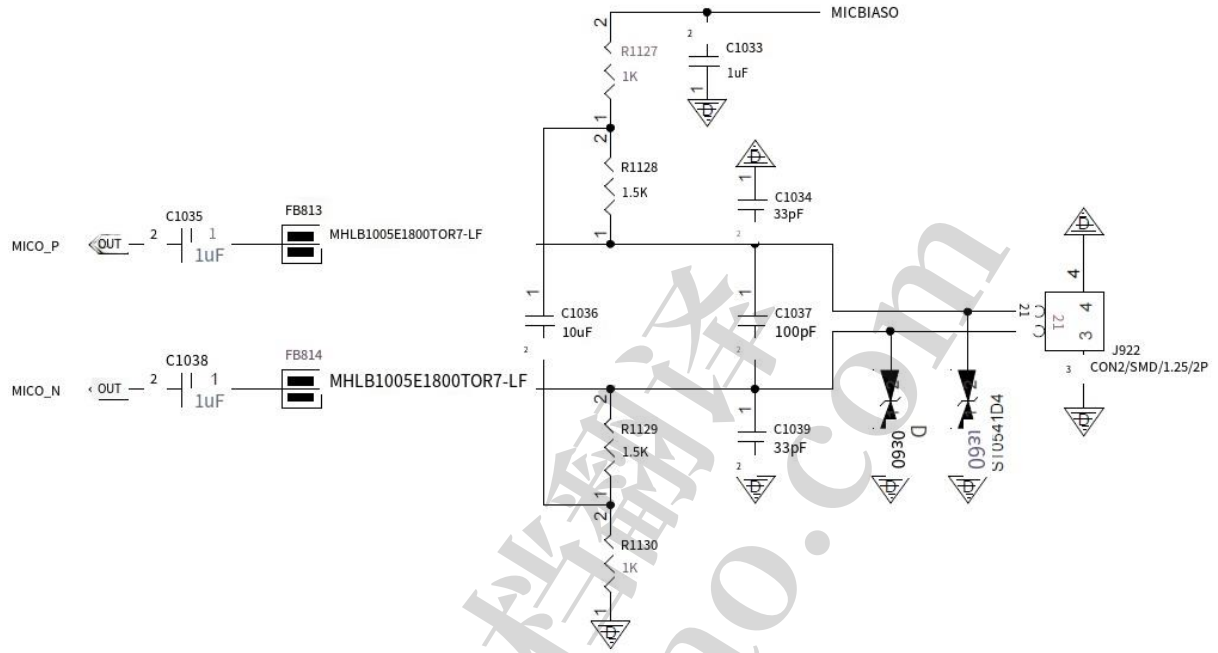
- When the PWRKEY is lowered for more than 1 second in the startup state, the Android system will have a prompt window pop up, and the user will confirm and click the shutdown menu to shut down (you can also force the restart by lowering the PWRKEY for 7 seconds);



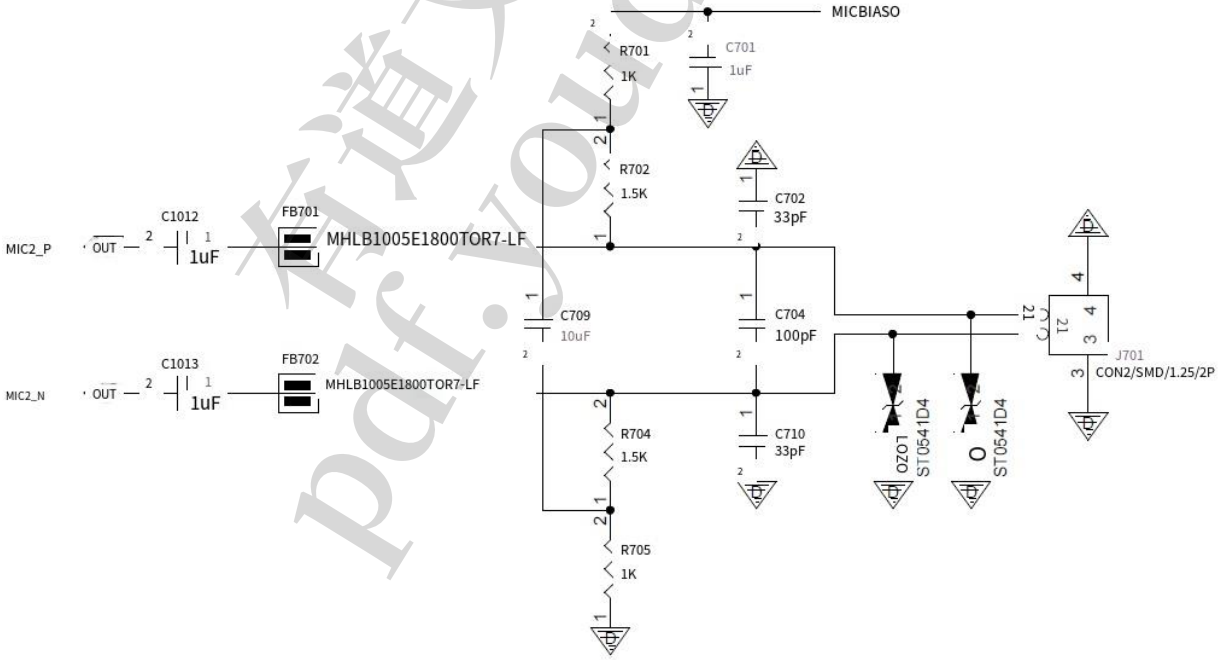
3.3 Analog audio interface

3.3.1 Analog MIC input

- Module supports 2 sets of analog MIC inputs;
- Integrated Micbias voltage output;
- MIC_P/N signal differential stereoscopic envelop;
- Micbias paranoid power pack;

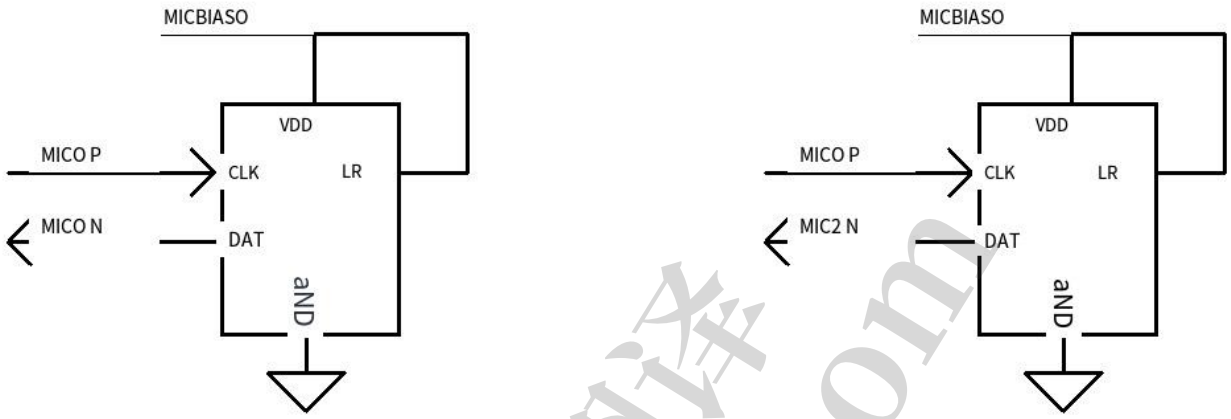


Analog MIC0 input



Simulation MIC2 input

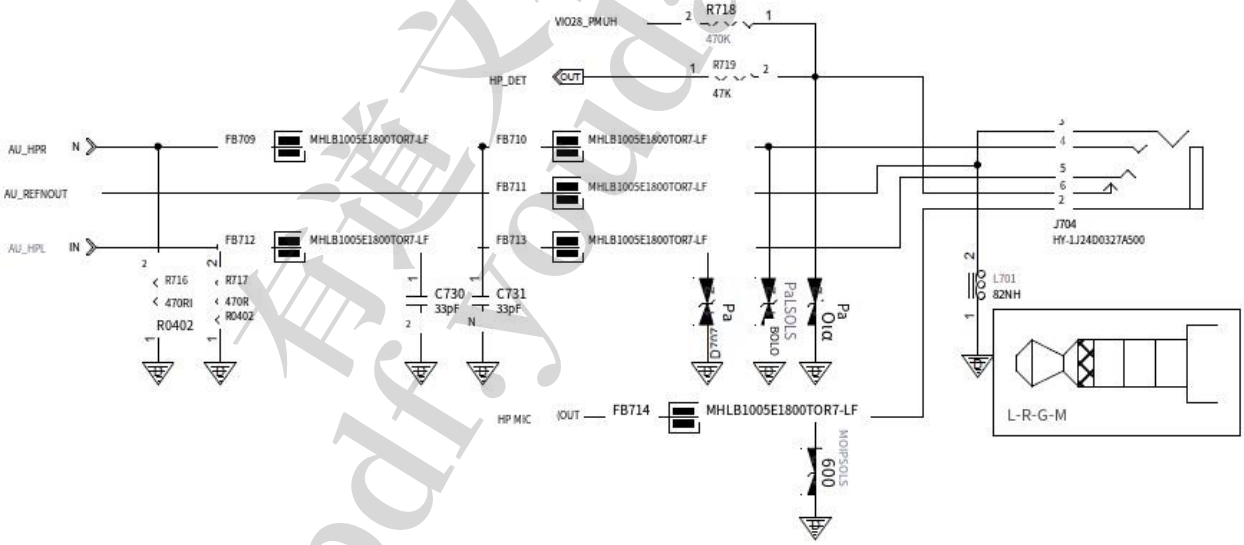
3.3.2 Digital DMIC input



Digital DMIC input

3.3.3 To simulate the headphone output

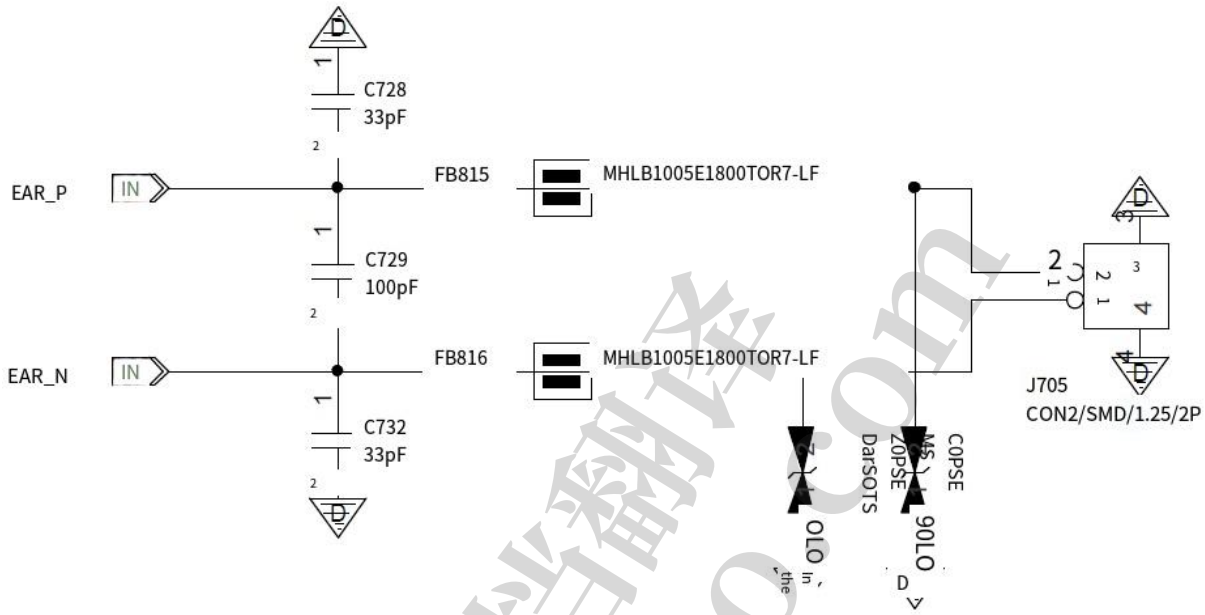
- Headphone plug and unplug detection signal pull-up level VIO28_PMU;
- AU_HPR AU_REFN/AU_HPL signal parallel three-dimensional package;
- HP_MIC signal stereo package;



Analog headphone output (with MIC)

3.3.4 Analog handset output

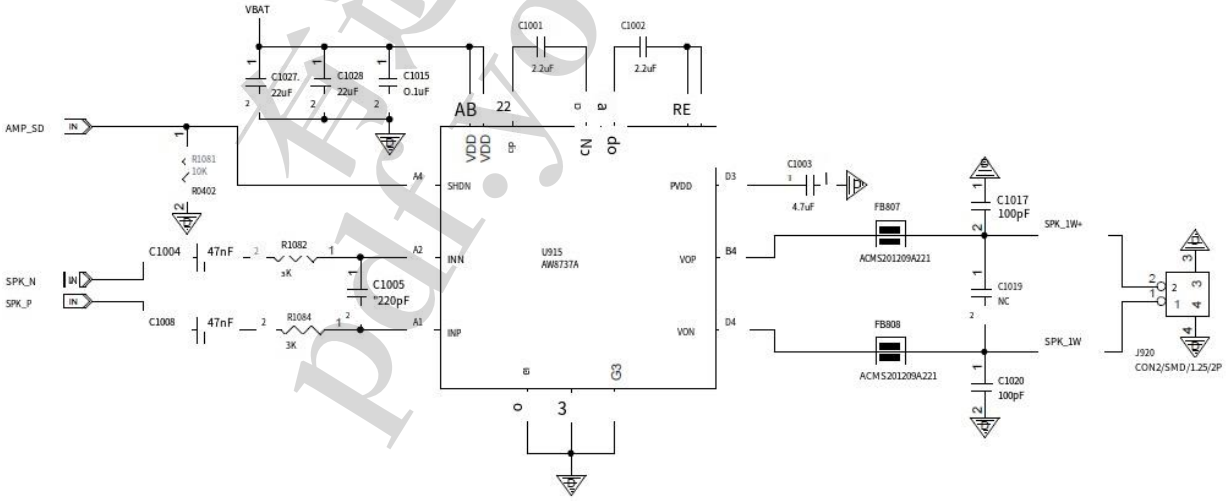
- EAR_P/EAR_N signal differential stereoscopic envelop;



The receiver output

3.3.5 Line out speaker output

- EAR_P/EAR_N signal differential stereoscopic envelop;
- Away from RF antenna \DC-DC and other interference sources;



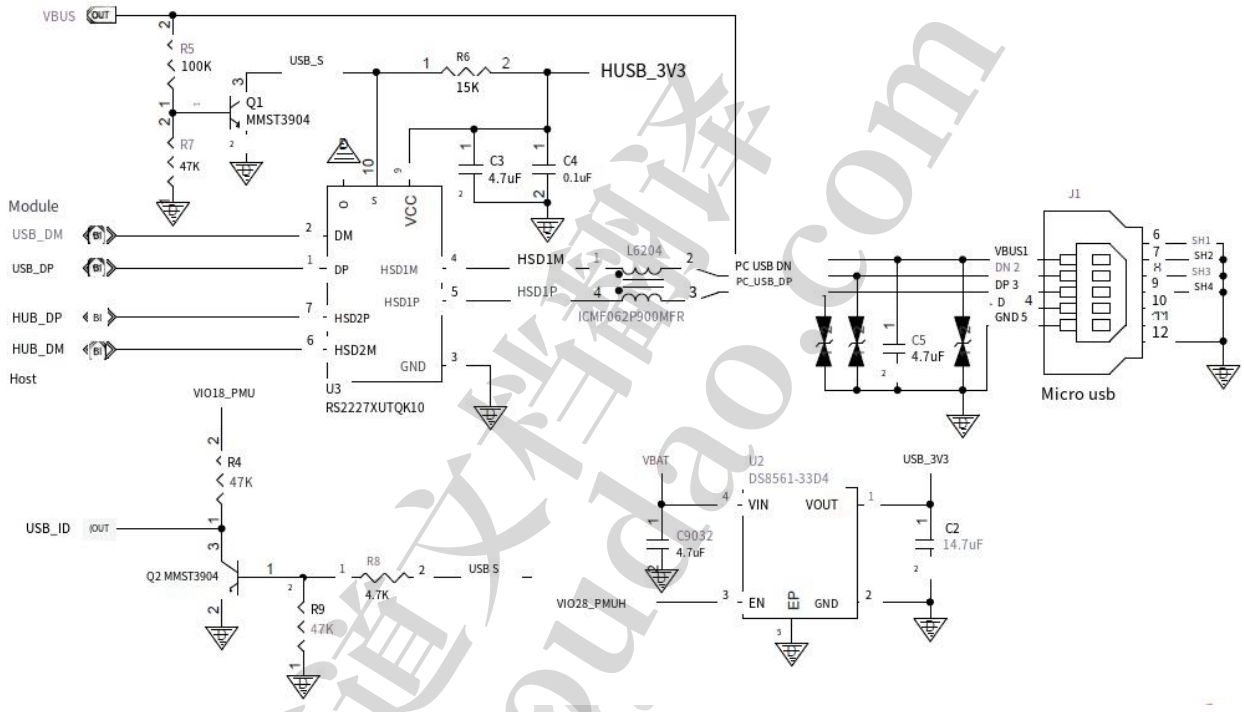
Line out horn output

3.4 USB interface design

- USB interface complies with USB2.0 specification and supports USB2.0 high-speed 480Mbps;
- USB interface is used for software upgrade and development debugging;
- Support USB OTG mode, USB_ID switch between Device and Host mode, USB_ID Device mode in high power hours, USB_ID Host mode in low power hours, Device and Host cannot be

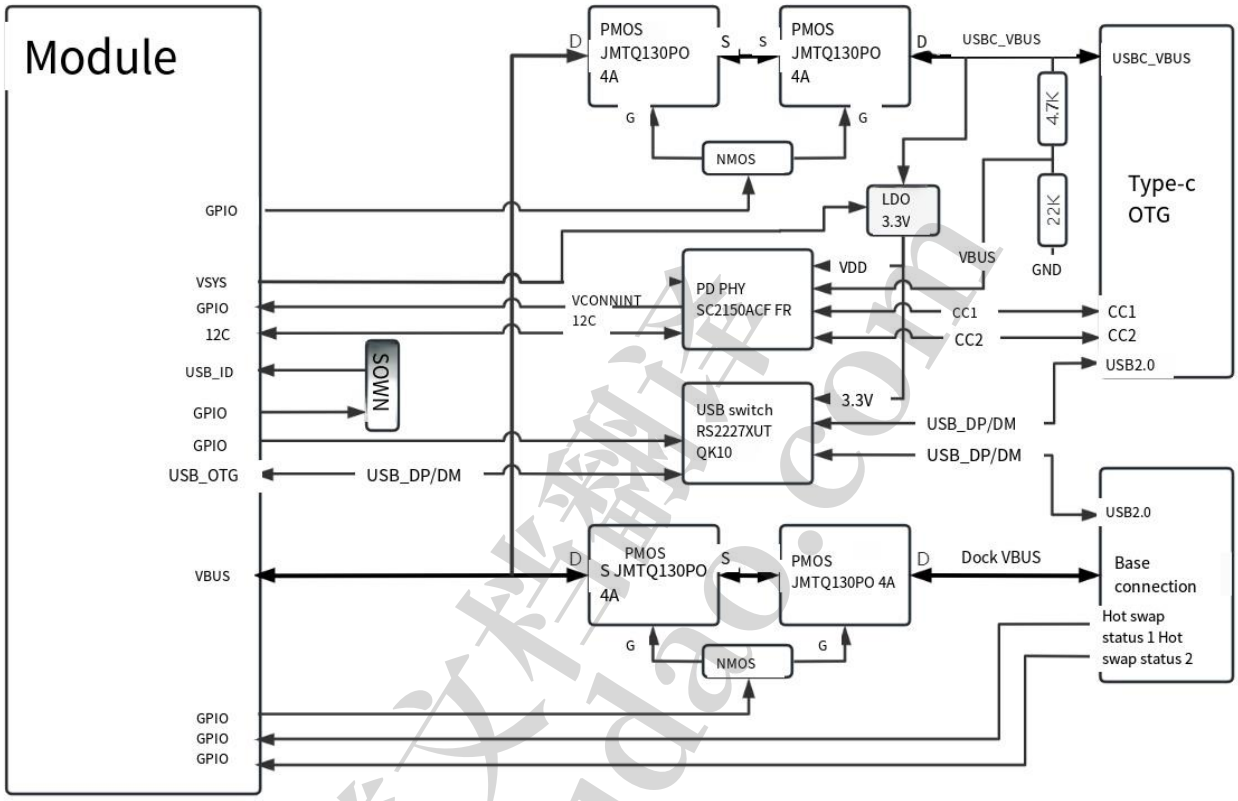
used at the same time;

- VBUS supports 5V power output (requires charging inside the module);
- USB DP/DM signal motherboard PCB needs differential wiring and three-dimensional ground processing and differential impedance control 90Ω±5Ω;



No charging function USB interface design

Note: Design without charging function Vbus power access will automatically switch USB electronic switch and USB_ID to Device status



Type-c interface with Dock dock dock design

Note:

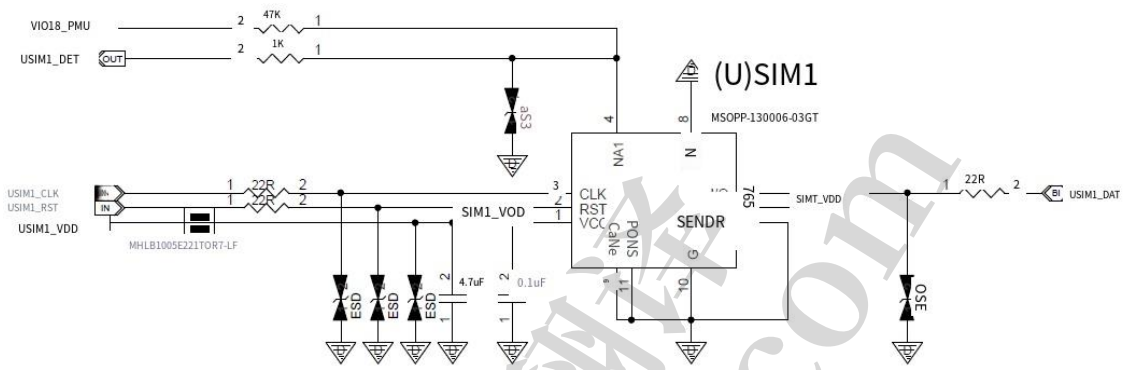
1. The Type - c interface and using the dock

2. The Dock for fixed 5 v charging voltage

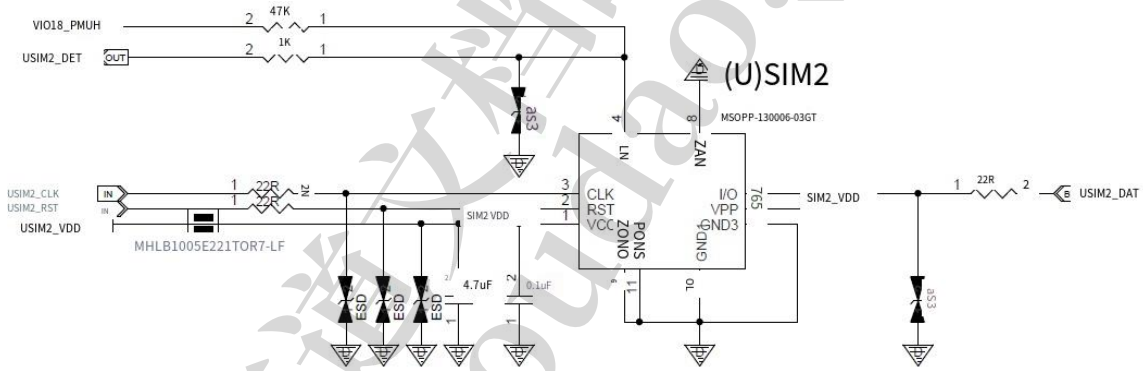
3.5 (U) Design of SIM card interface

- Module support double card double wait, single pass;
- (U) the SIM card is powered from inside the module and automatically recognizes the class of 1.8V or 2.95V card;
- Two sets of (U)SIM card signals (including hotplug detection) cannot be used for other functional purposes;
- USIM_DET detection interrupt the default high level SIM card inserted;
- The SIM card seat is placed close to the module, and the wiring length of (U)SIM card signal line is not more than 200 mm, and the wiring length in the SIM card signal group is equal, with an error of ±25mil;
- The wiring of the SIM card signal cable is far away from RF and VBAT power cables;
- SIM related device layout booth near the SIM booth put;
- CLK signal shall be independent three-dimensional ground cover to avoid cross-talk with USIM_DATA signal, and data group wiring shall be protected by ground cover.
- SIM card signal selects TVS tube parasitic capacitance < 5 pF;
- A 22-ω resistance in series is required between the module and the SIM card to inhibit stray EMI and enhance ESD protection. The 22-ω resistance is placed close to

the end of the SIM card seat.



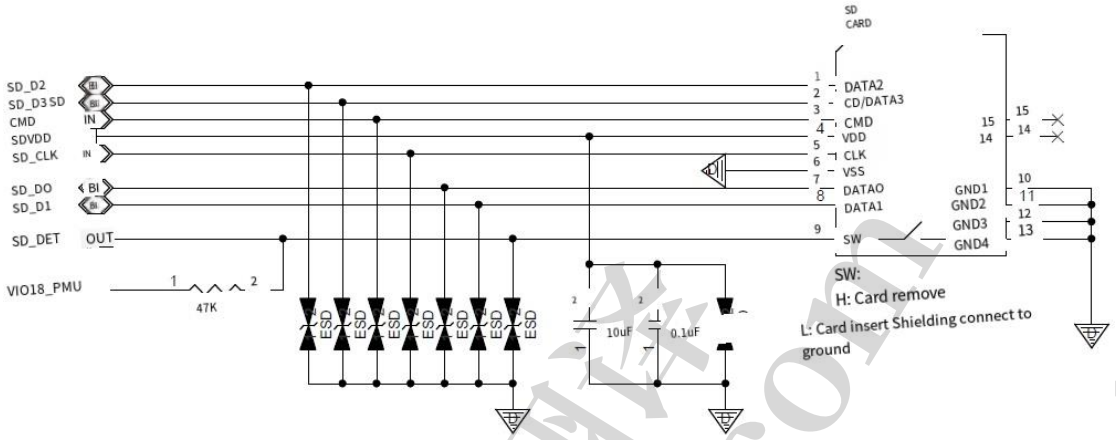
(U)SIM1 design



SIM2 design (U)

3.6 SD Card interface design

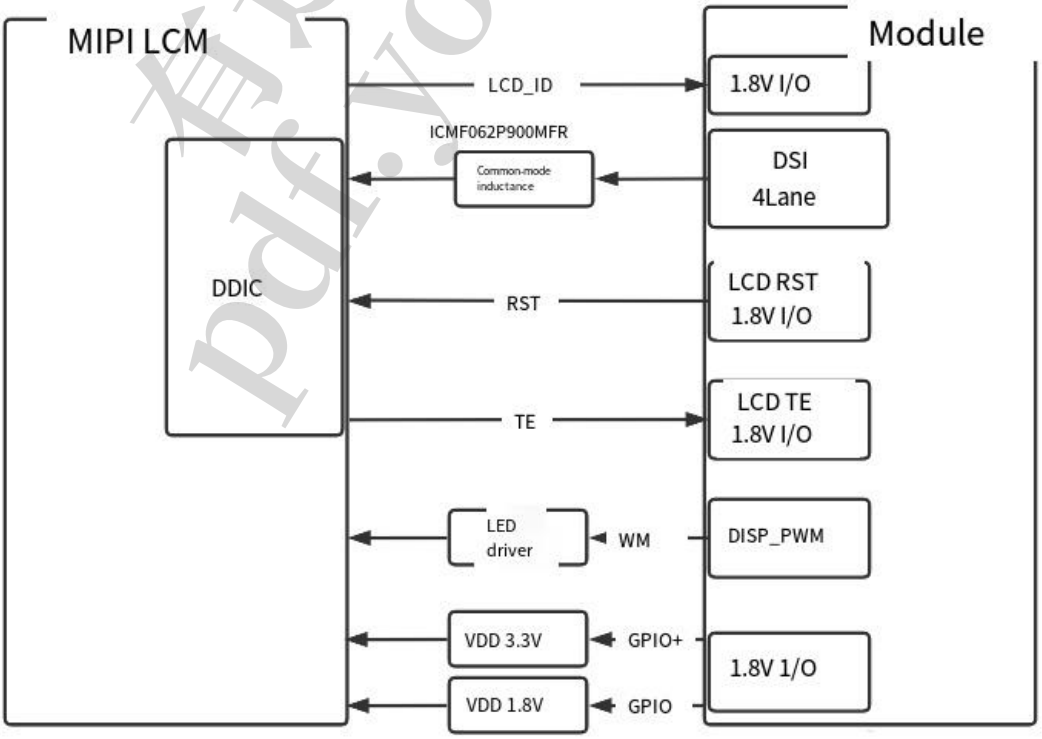
- SD card interface support SDIO2.0/3.0 protocol interface, support SD/SDHC/MS/MSPRO/MMC;
- SD card supports a maximum capacity of 256GB;
- SD cards are powered by 3.0V inside the module;
- SD_DET signal detection software default low-level insert SD card;
- SD card signal selection TVS diode parasitic capacitance < 5 pF;
- The device layout related to SIM card seat is placed close to SIM card seat;
- SD_CLK needs to be processed independently, and SD card bus wiring refers to CLK for intra-group equilength, error ±25mil;



SD card interface design

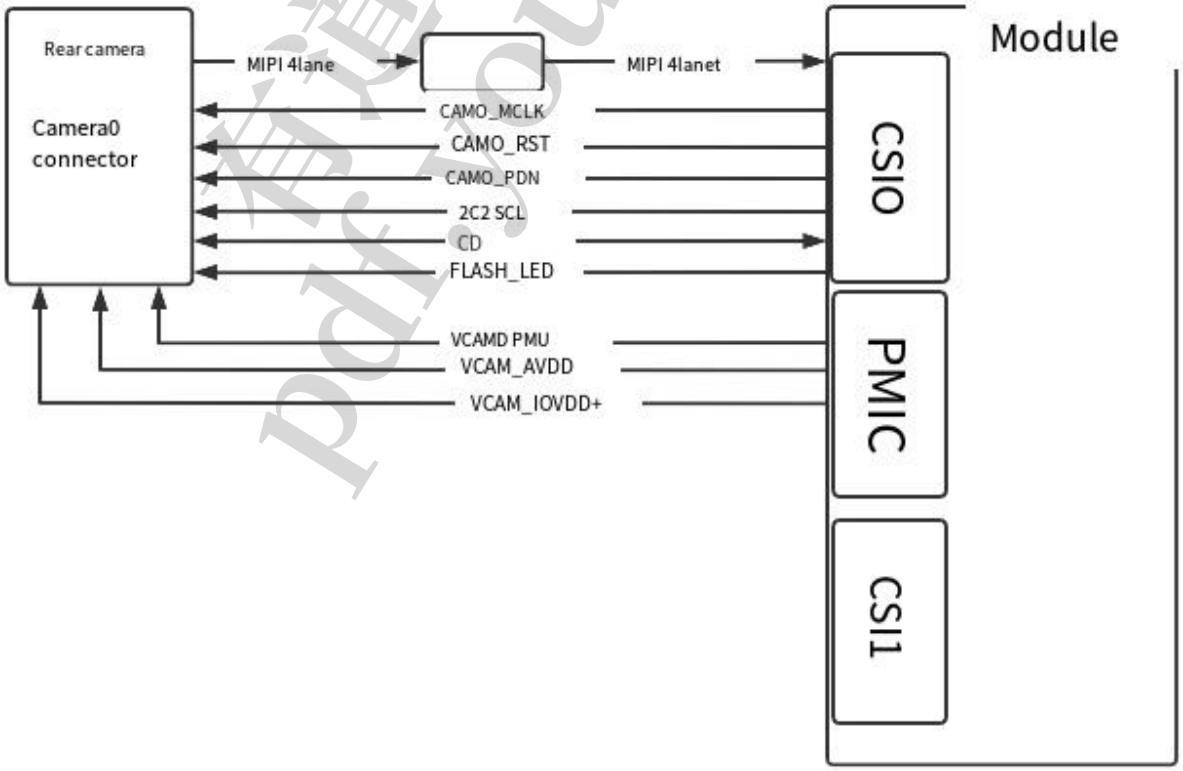
3.7 Display DSI interface design

- DSI 4 lane MIPI high-speed signal;
- 4 lane MIPI high-speed signal increases common-mode inductor;
- Motherboard PCB wiring requirements differential wiring, differential single group to do ground processing, 4 groups of difference need to have a complete reference ground plane, differential impedance control 100Ω±10%;
- 4lane MIPI signals need isometric processing, P/N isometric error is less than 6mil, bus reference CLK isometric error is less than 25mil.
- When MIPI signal is placed in ESD device, TVS parasitic capacitance is < 1pF;
- Total wiring length of MIPI motherboard < 2000mil;

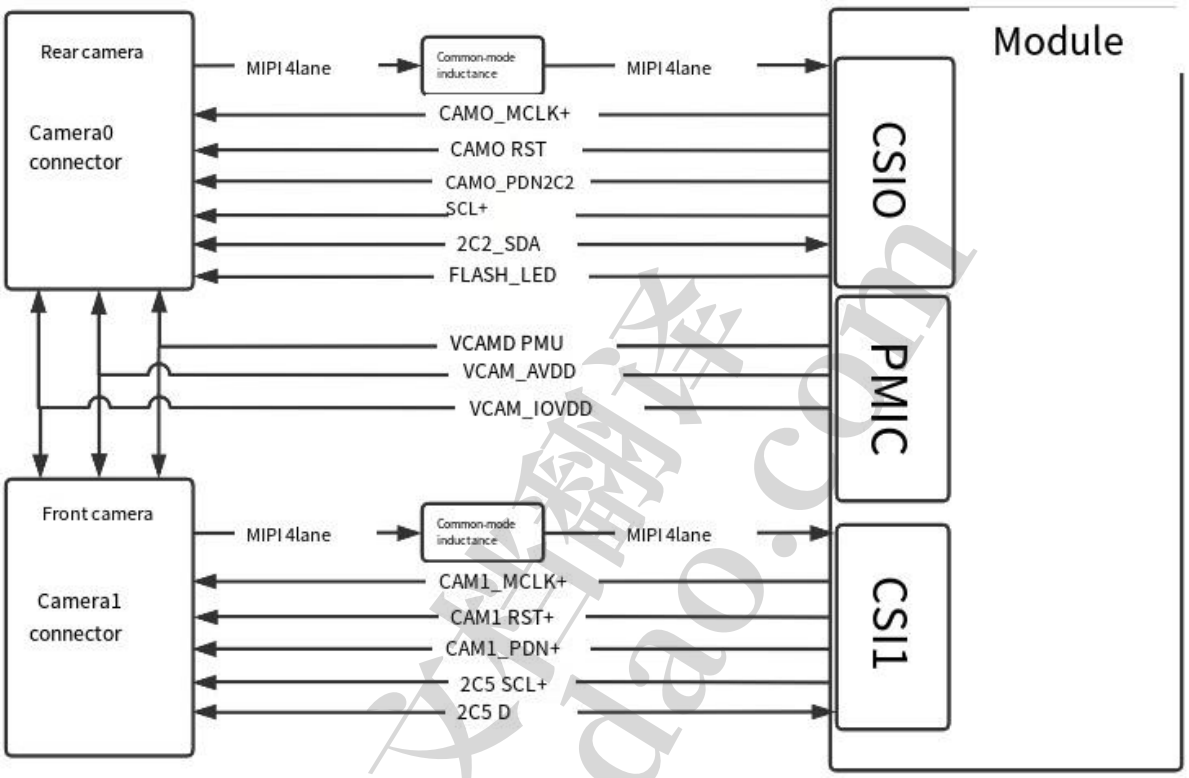


3.8 Camera interface design

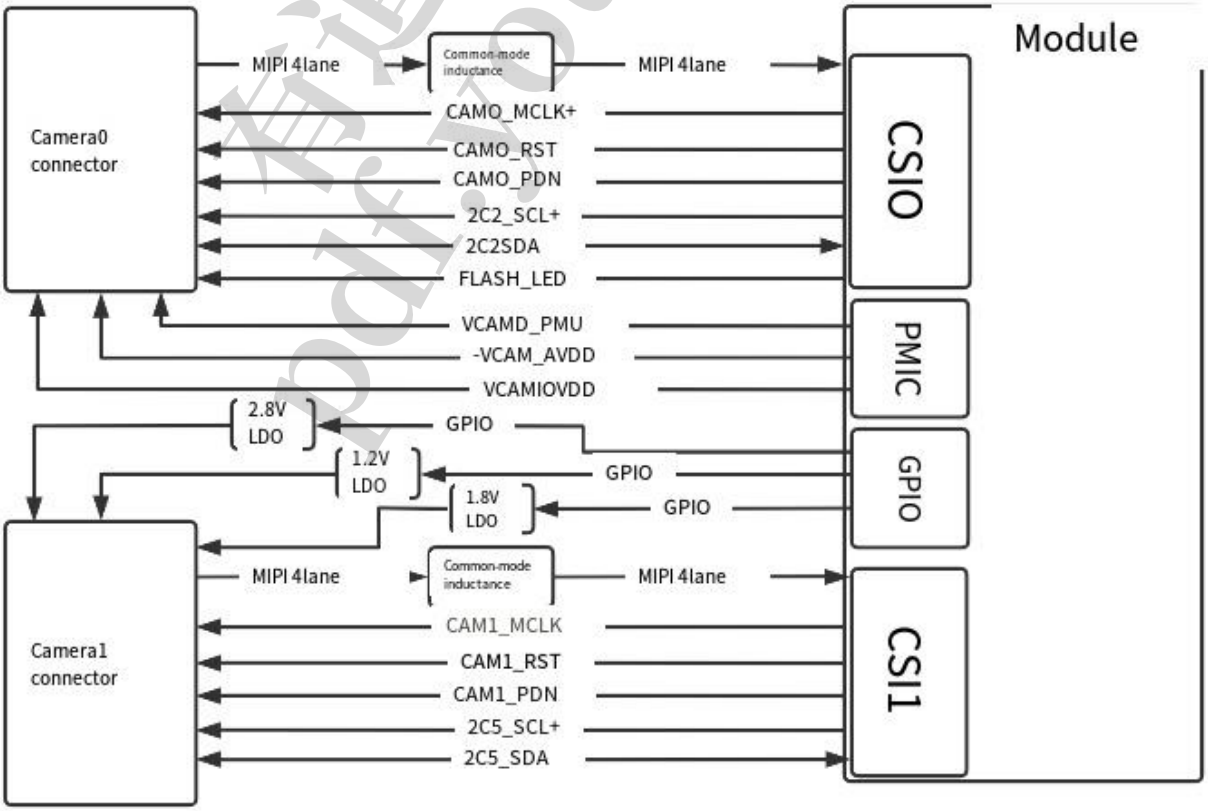
- Two groups of CSI-2 protocol interface, 4lane MIPI high-speed signal;
- 4 lane MIPI high-speed signal increases common-mode inductor;
- Motherboard PCB wiring requirements differential wiring, differential single group to do ground processing, 4 groups of difference need to have a complete reference ground plane, differential impedance control 100Ω±10%;
- 4lane MIPI signal needs equal length processing, P/N single group equal length error < 6mil, bus reference CLK equal length error < 25mil;
- When MIPI signal is placed in ESD device, TVS parasitic capacitance is < 1pF;
- Total wiring length of MIPI motherboard < 2000mil;
- The positive maximum FLASH_LED flash drive current 700 ma, motherboard according to demand design current-limiting resistance;
- VCAMD_PMU/ VCAM_AVDD/ VCAM_IOVDD power supply is a special power supply for the camera, can not be used for other purposes;
- TVS electrostatic tube shall be added for camera power supply and control signal, TVS parasitic capacitor < 5pF, filter capacitor shall be added for VCAMD/VCAM_AVDD/VCAM_IOVDD power supply, and related devices shall be placed close to the camera connector.
- High pixel cameras are connected to CSI0 channel by default;
- Single camera application scenario, the priority use CSI0 channel, dangling CSI1 channels;



Single camera application



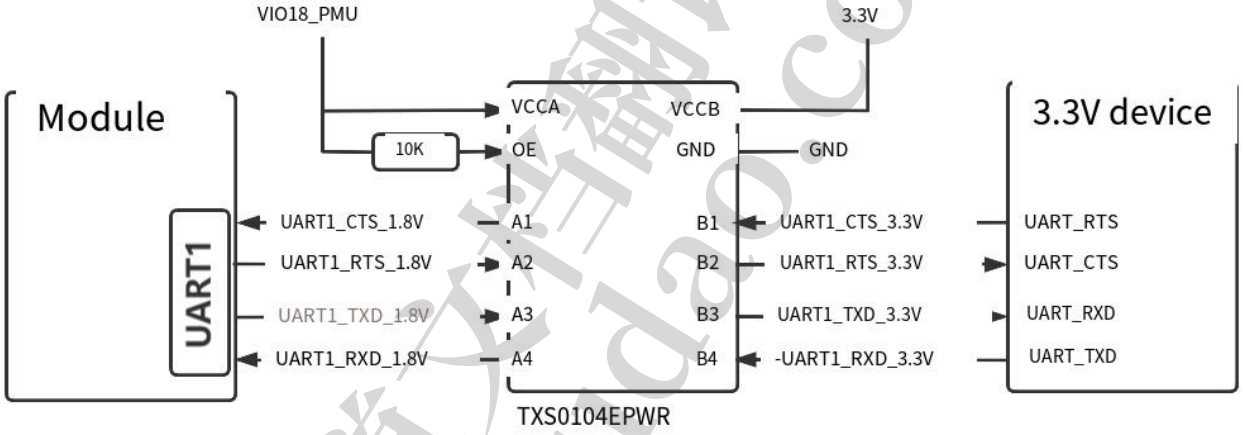
Dual-camera switching application



Dual camera simultaneous application

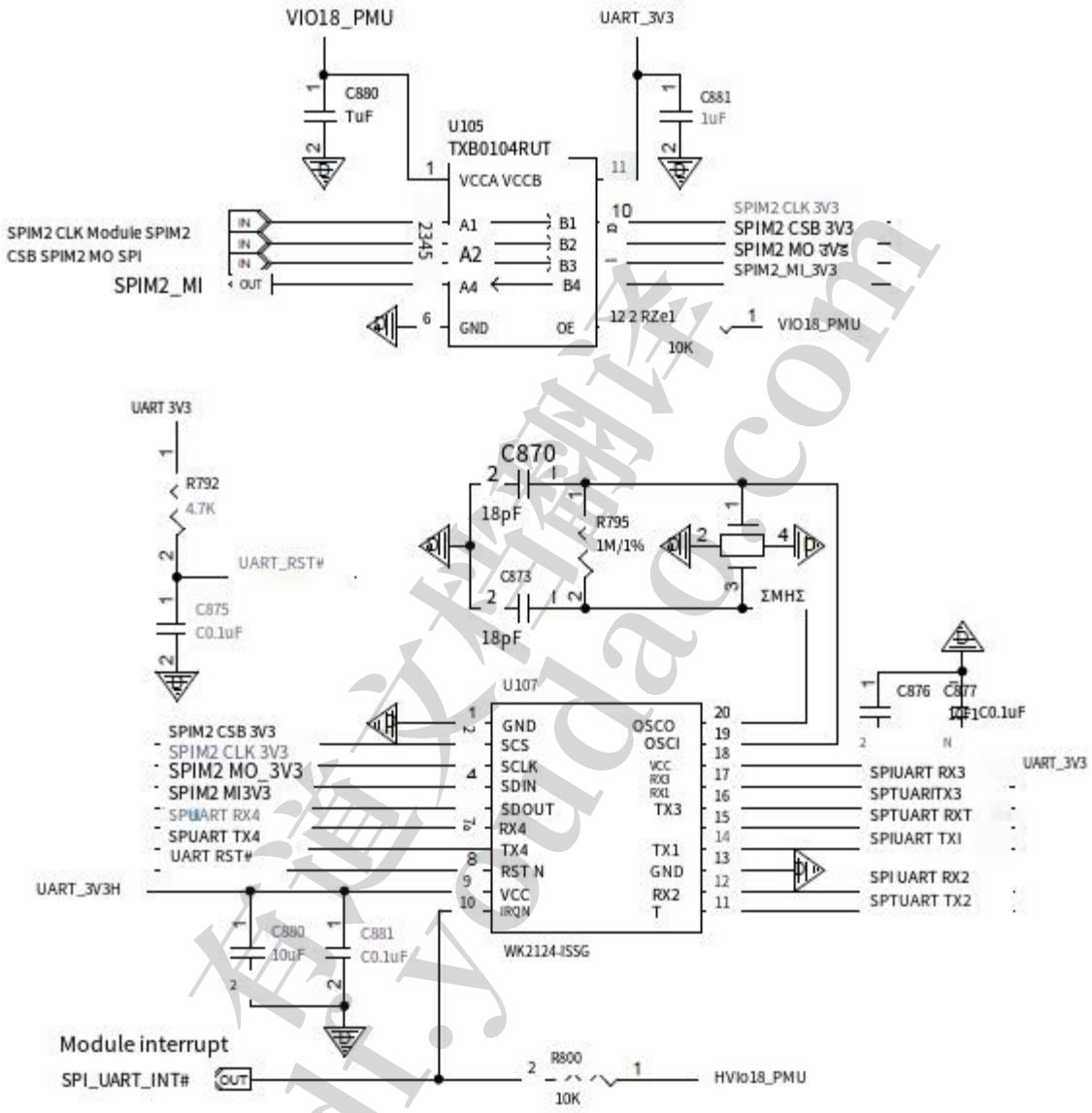
3.9 UART serial port interface design

- Module support 2 groups of UART (UART0/UART1), the default baud rate 961200;
- UART0 is used for system debug by default, modify the software driver can be used as a function serial port, boot in the bootrom stage debug log output, cannot be used for encryption IC and other important devices, encryption IC and other important devices use UART1 communication;
- UART0 signal can not change the Pin pin of the module, fixed 93Pin/94Pin;
- The interface level of UART0/UART1 is 1.8V, and the level conversion IC should be added when 3.3V device is applied;



UART level switching application

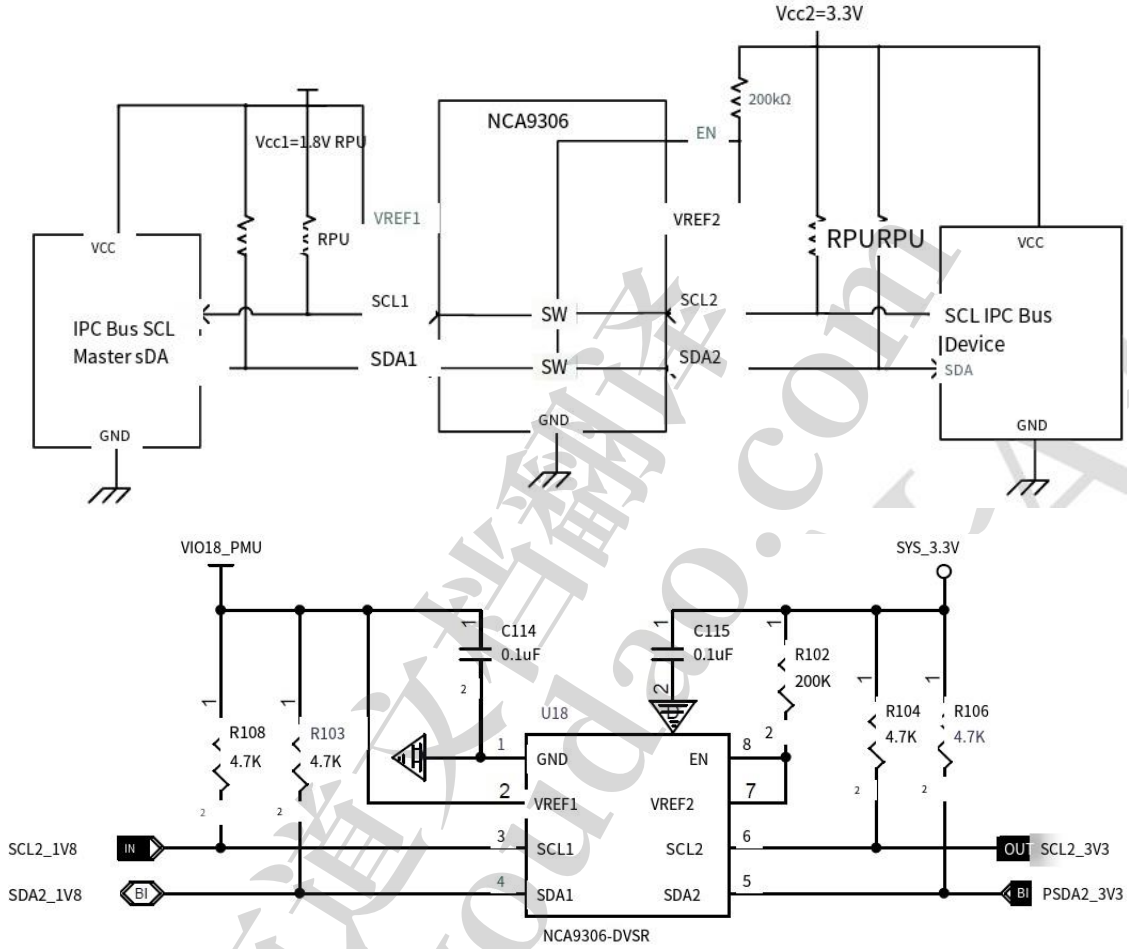
- When the UART serial channel does not meet the demand, please use SPI interface to do the conversion extension UART, which can be extended to 4 channels;



SPI extends 4-channel UART

3.10 I2C interface design

- 5 groups of I2C, support standard mode 100KHz and high speed mode 400KHz;
- I2C1/I2C2/I2C4/I2C5 channel SOC internal hardware pull-up 5KΩ by default, software can change to 1KΩ pull-up or turn off internal pull-up;
- I2C3 channel compatible with Z600-H motherboard design must add external I2C pull-up resistance, software close internal pull-up;
- I2C interface level is 1.8V, 3.3V device application needs to increase the level conversion IC;
- For level conversion IC and MOS tube level conversion, devices with internal pull-up resistance (such as SGM4553 similar IC) should not be used. Please use the IC of NCA9306/PCA9306 with external pull-up resistance of the same specification.
- When designing the circuit of the main board, the I2C channel should retain the design of external pull-up resistance, and the default use of internal pull-up;

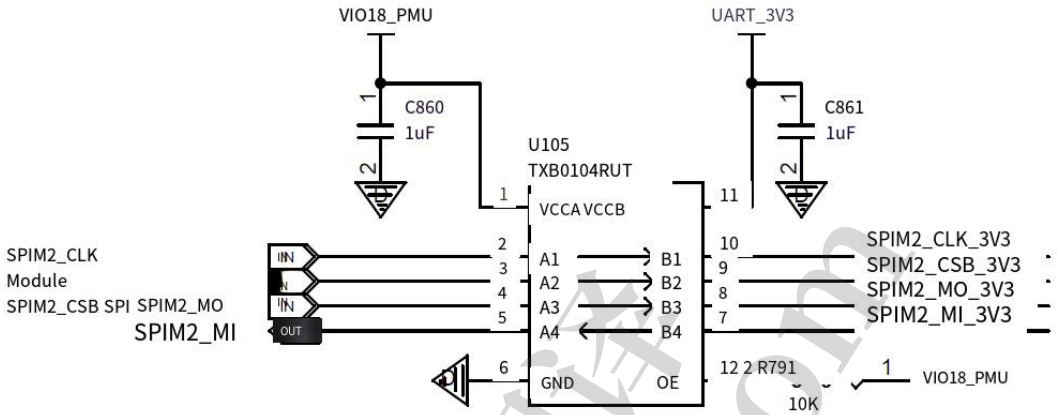


I2C level switching application

3.11 SPI interface design

- Supports 5 groups of SPI interfaces
- Compatible with Z600-H please refer to the module Pin function compatible design table;
- Operating frequency range: 0.8K bit/s ~27M bit/s;
- SPI interface level is 1.8V, 3.3V device application needs to increase the level conversion IC;
- When selecting the level conversion IC, it is necessary to pay attention to the transmission rate required by SPI of the project. If the rate is below 15M, chips of SGM4564 category specifications can be used; if the rate is above 15M (including 15M), chips of TXB0104RUT category specifications should be used

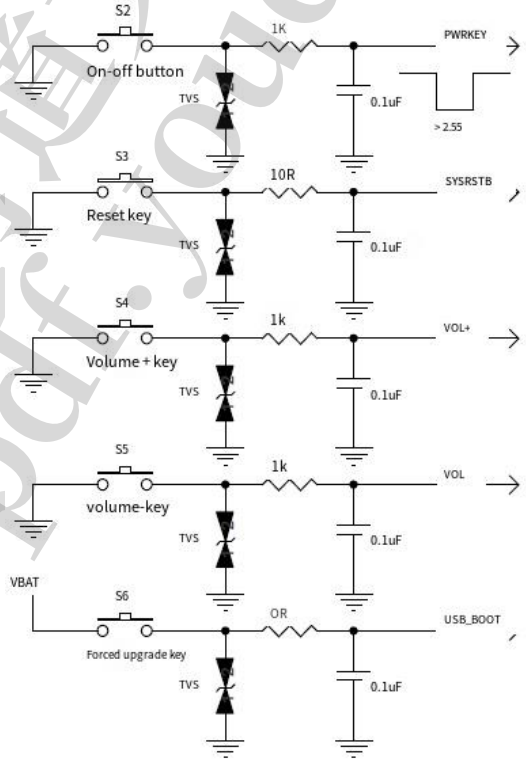
  SPI interface level conversion cannot use SGM4553 class specification chip;



SPI level conversion application

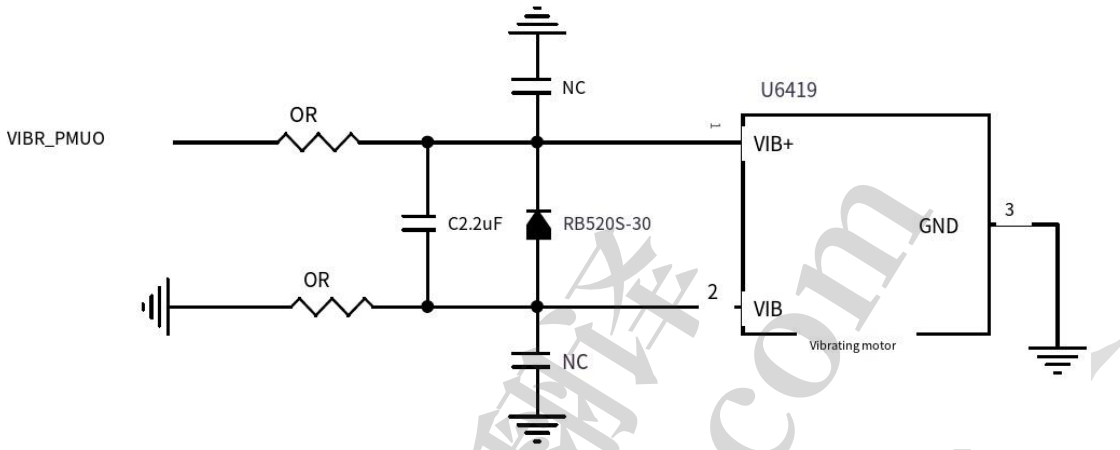
3.12 Key application design

- TVS electrostatic tube should be placed in key design, PWRKEY/VOL+/VOL-/SYSRSTB signal design RC to enhance EDS protection;
- USB_BOOT control signal for the hardware forced upgrade state, press the forced upgrade button and then power on, the module will automatically enter the downloading and burning mode;
- The full-function keyboard can be extended externally by using I2C or SPI interface;



Module keystroke application

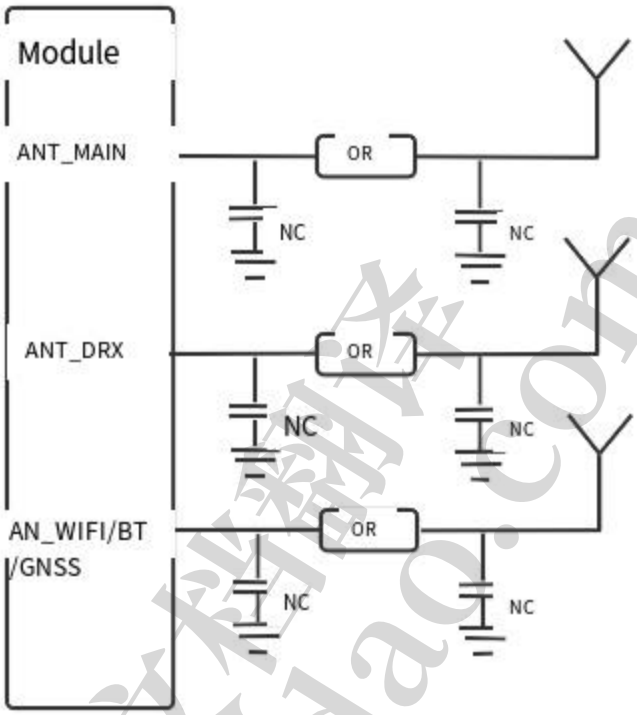
3.13 Vibration motor design



Module vibration motor application

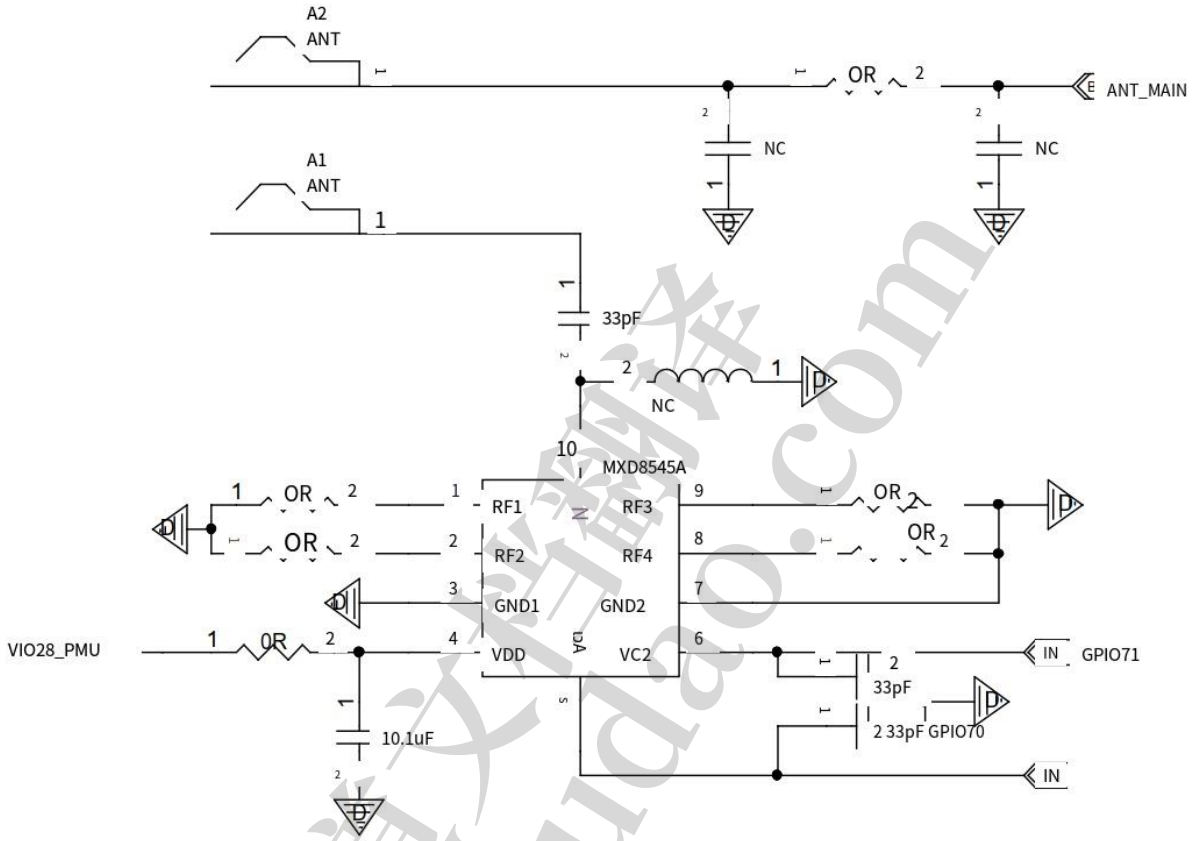
3.14 Antenna port design

- ANT_MAIN main/ANT_DRX Diversity and AN_WI-FI/BT/GNSS 3-in-1 antenna motherboards must do 50Ω impedance control;
- The antenna wiring must have a complete reference GND plane. Add a GND crossing hole around the signal line and the reference ground as much as possible to help improve the RF performance. The distance between the GND crossing hole and the signal line should be at least twice the width of the line (2W).
- The GND pad pin adjacent to the antenna pin should not be made of hot pad, so it should be in full contact with the ground and increase the ground hole as much as possible.
- The path loss from the antenna end to the Module antenna pad must be controlled within 2dB, and the antenna path wiring PCB design should not be drilled through the hole;
- The motherboard near the Pin end of the module antenna must reserve π-type matching circuit, the default patch 0 ohm resistance through;
- Module only supports passive GPS antenna;



Module antenna design

3.15 RF tuner switch design



Z500-HEU version

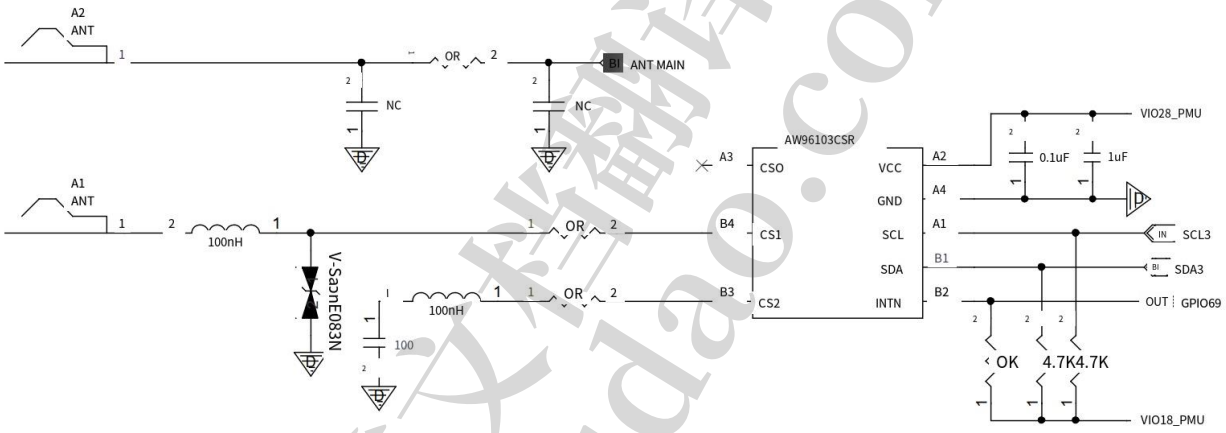
Z500-HEU Version Tuner Switch Design Logic				
Module 262Pin: GPIO70 Module 260Pin: GPIO71				
Single pole four throw switch	Switching port	RF band	GPIO70	GPIO71
	RF1	B8/GSM900/W8	0	0
	RF2	B5/20/GSM850/W5	0	1
	RF3	B28	1	0
	RF4	B1/2/3/4/7/38/40/41/GSM1800/1900/W1/W2	1	1

Z500-HA version

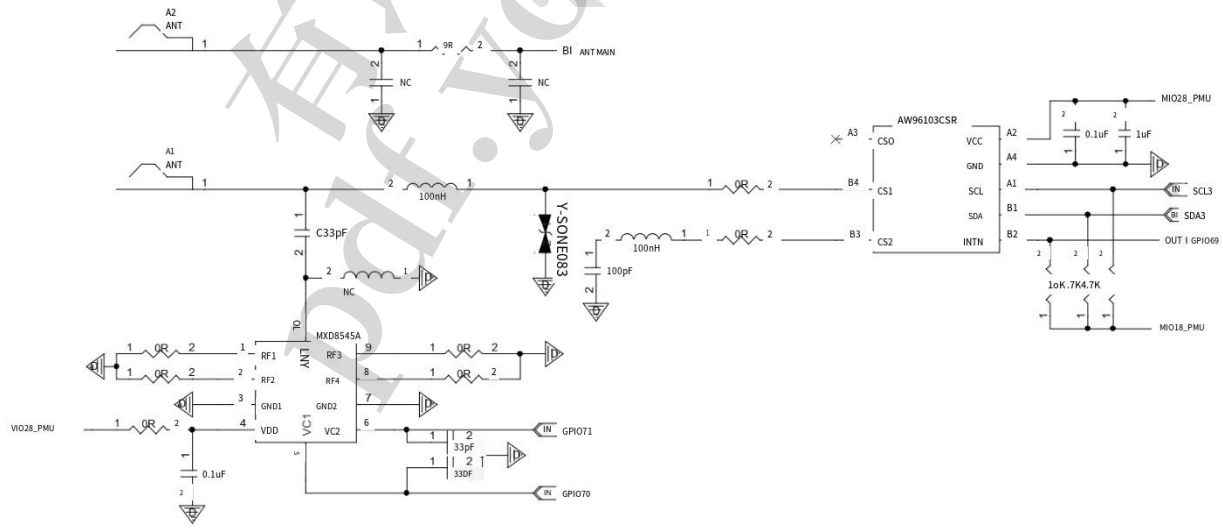
Z500-HA version Tuner Switch design logic				
Module 262Pin: GPIO70 Module 260Pin: GPIO71				
Single pole	Switching port	RF band	GPIO70	GPIO71

four throw switch	RF1		0	0
	RF2	B5/26/GSM850/W5	0	1
	RF3	B12/13/14/17/71	1	0
	RF4	B2/4/7/25/41/66/GSM1900/W2/W4	1	1

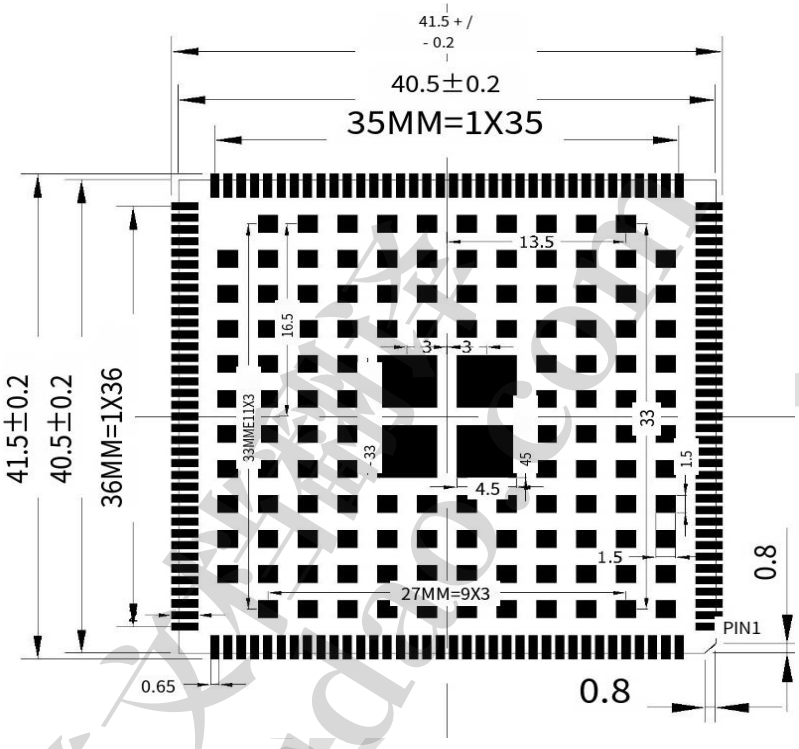
3.16 SAR sensor Design



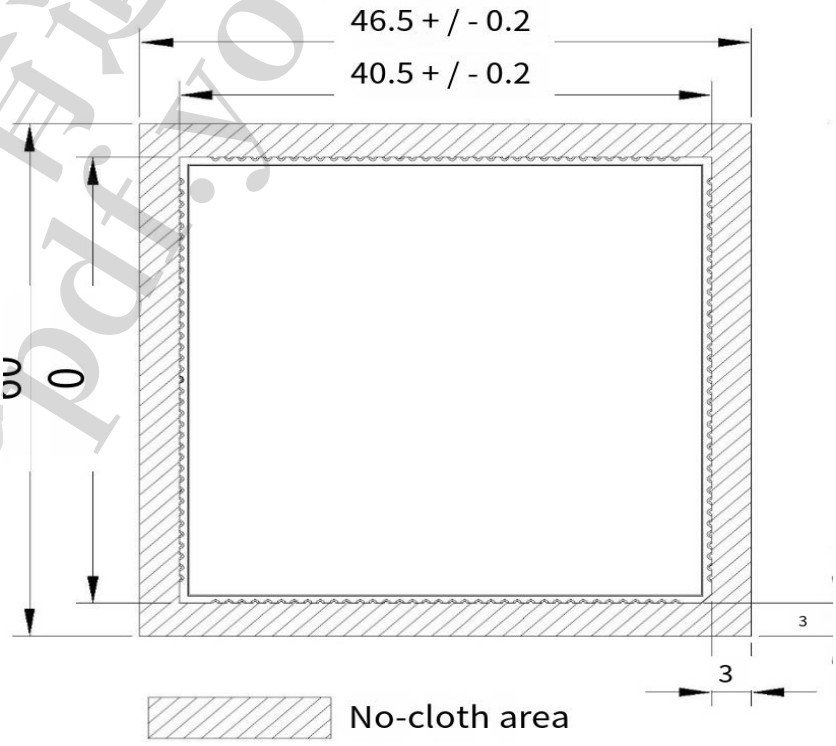
3.17 SAR sensor plus Tuner Switch design



4. Recommended PCB package size



Recommended PCB package size (unit: mm)



Safety spacing (unit: mm)

1. **Integration instructions for host product manufacturers according to KD B 996369 D03 OEM Manual v01**

8.1 List of applicable FCC rules.

Part 15C,15E,22H,24E,27

8.2 Specific operational use conditions

Operating Frequency:part 2.3.1
Z500-H Is a universal GSM WCDMA LTE Wi-FiBTSmart module, with the industry's competitive package size and ultra-low energy consumption technology, designed for mobile devices and Internet of Things applications, Users can connect to the network through GSM, WCDMA, LTE WIFI, network communication, networking functions.
To maintain compliance with FCC RF exposure requirements, Please use the antenna provided with the product.

8.3 Limited Module Procedures. KDB 996369 D03, Section 2.4

not applicable .Please refer to the manual for usage scenarios Single Modular Approval Request

8.4 Trace antenna designs. KDB 996369 D03, Section 2.5

not applicable .without trace antenna

8.5 RF exposure considerations.

RF exposure requirements are fulfilled for mobile configuration. This equipment should be installed and operated with minimum distance between 20cm the radiator your body
The installation of the module is restricted to mobile host devices
For portable applications OEM integrators need SAR evaluation and an own fCC ID.

8.6 Antennas.

The module comes with permanently attached External antennas. The spurious emission requirements are fulfilled (see attached test report).

8.7 Label and compliance information.

See Guidelines for Labeling and User Information for RF Devices –KDB Publication 784748.host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID 2A9FT-Z500-H ” with their finished product.

8.8Information on test modes and additional testing requirements.

The test mode in the report is the module's maximum transmitting power emission for testing

Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

8.9Additional testing, Part 15 Subpart B disclaimer

the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

FCC WARNING

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.

15.105 Information to the user.

(b) For a Class B digital device or peripheral, the instructions furnished the user shall include the following or similar statement, placed in a prominent location in the text of the manual:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

The availability of some specific channels and/or operational frequency bands are country dependent and are firmware programmed at the factory to match the intended destination.

The firmware setting is not accessible by the end user.

The final end product must be labelled in a visible area with the following:

“Contains Transmitter Module 2A9FT-Z500-H”

RF Specification:

Function	Operation Frequency	Max RF output power:
BLE	2402MHz–2480MHz	<10 dBm
BT(BR+EDR)	2402MHz–2480MHz	<10 dBm
WIFI 802.11b/g/ n(HT20/40)	802.11b/g/n(20MHz): 2412~2472MHz; 802.11n(40MHz):2422~2462MHz	<20 dBm
Wi-Fi 5.2G(802.11a/n20/n40 /ac20/ac40/ac80)	802.11a/ n20/ac20:5180MHz~5240MHz 802.11 n40/ac40:5190MHz~5230MHz 802.11 ac80:5210MHz	<20 dBm
Wi-Fi 5.3G(802.11a/n20/n40 /ac20/ac40/ac80)	802.11a/ n20/ac20:5260MHz~5320MHz 802.11 n40/ac40:5270MHz~5310MHz 802.11 ac80:5290MHz	<20 dBm
Wi-Fi 5.6G(802.11a/n20/n40 /ac20/ac40/ac80)	802.11a/ n20/ac20:5500MHz~5700MHz 802.11 n40/ac40:5510MHz~5670MHz 802.11 ac80:55300MHz~5610MHz	<20 dBm
Wi-Fi 5.8G(802.11a/n20/n40 /ac20/ac40/ac80)	802.11a/ n20/ac20:5180MHz~5240MHz 802.11 n40/ac40:5190MHz~5230MHz 802.11 ac80:5210MHz	<20 dBm
GSM/GPRS/EGPRS 900	TX(Uplink):880M-915MHZ; RX(Downlink):925M-960MHZ	<33 dBm
GSM/GPRS/EGPRS 1800	TX(Uplink):1710M-1785MHZ; RX(Downlink):1805M-1880MHZ	<33 dBm
WCDMA B1	TX(Uplink):1920-1980MHz; RX(Downlink):2110-2170MHz	<25 dBm
WCDMA B8	TX(Uplink): 880-915MHz; RX(Downlink):925-960MHz	<25 dBm
LTE FDD B1	TX(Uplink):1920-1980MHz; RX(Downlink):2110-2170MHz	<25 dBm
LTE FDD B3	TX(Uplink) :1710-1785MHz; RX(Downlink):1805-1880MHz	<25 dBm
LTE FDD B7	TX(Uplink) :2500-2570MHz; RX(Downlink):2620-2690MHz	<25 dBm

LTE FDD B8	TX(Uplink): 880MHz to 915 MHz RX(Downlink): 925 MHz to 960 MHz	<25 dBm
LTE FDD B20	TX(Uplink) 832MHz~862MHz; RX(Downlink)791MHz~821MHz	<25 dBm
LTE FDD B28	TX(Uplink) 703 MHz to 748MHz RX(Downlink) 758 MHz to 803 MHz	<25 dBm
LTE TDD B38	TX(Uplink)& RX(Downlink): 2570 MHz to 2620 MHz	<25 dBm
LTE FDD B40	TX(Uplink)& RX(Downlink): 2300 MHz to 2400 MHz	<25 dBm
GPS	Rx(Downlink): 1.57542GHz	--

Warning:

1.Use careful with the earphone maybe possible excessive sound pressurefrom earphones and headphones can cause hearing loss.

2. CAUTION: RISK OF EXPLOSION IF BATTERY IS REPLACED BYAN INCORRECT TYPE. DISPOSE OF USED BATTERIES ACCORDINGTO THE INSTRUCTIONS.

3. The product shall only be connected to a USB interface of version USB2.0.

4. Adapter shall be installed near the equipment and shall be easily accessible.

5. Operation temperature:-30~75ºC.

6. The plug considered as disconnect device of adapter.

7. SAR: The device complies with RF specifications when the device used at 0.5cm from your body (SAR limit 2.0 W/Kg). The device is in compliance with the requirements.

Restrictions in the 5 GHz band:

According to Article 10 (10) of Directive 2014/53/EU, the packaging shows that this radio equipment will be subject to some restrictions when placed on the market in Belgium (BE), Bulgaria (BG), the Czech Republic (CZ),Denmark (DK), Germany (DE), Estonia (EE), Ireland (IE), Greece (EL), Spain(ES), France (FR), Croatia (HR), Italy (IT), Cyprus (CY), Latvia (LV), Lithuania(LT), Luxembourg (LU), Hungary (HU), Malta (MT), Netherlands (NL), Austria(AT), Poland (PL), Portugal (PT), Romania (RO), Slovenia (SI), Slovakia (SK),Finland (FI), Sweden (SE),, Turkey (TR), Norway(NO), Switzerland (CH), Iceland (IS), and Liechtenstein (LI).

The WLAN function for this device is restricted to indoor use only when operating in the 5150 to 5250 MHz frequency range.

	ES	LU	RO	CZ	FR	HU	SI
	DK	HR	BE	BG	DE	EE	IE
	EL	IT	Cy	LV	LT	SK	MT
	NL	AT	PL	PT	FI	SE	TR
	NO	CH	IS	LI			