Xinfa Technology Z400-H3intelligent module

Hardware design guide

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Revision history

Version number	Revised Content	Release time	Revised
V0.1	create	2022-11-03	Bo.wen

note

Due to product version upgrades or other reasons, the content of this document will be updated from time to time. Unless otherwise agreed, this document is provided as a guide for use only and all statements, information and suggestions in this document do not constitute any express or implied warranty.

Contents

1. Product overview

1.1 Product Introduction

Z400-H3 module is a 4Gwireless communicationintelligentmodulelaunched by Xinfa Technology, which complies with3GPPspecifications. SupportTD-LTE/FDD-LTE/WCDMA/GSMSstandardandWiFi/BTshort-rangewireless transmission technology, supportGNSS(GPS/ Beidou/Glonass) wirelesspositioning technology. The product adopts RF baseband integrated design, which has the characteristics of high integration, small packagesizeandhigh reliability.

1.2 KeyFeatures

The Z400-H3moduleis designed inLCC+LGApackagewith dimensions of40.5x40.5x2.8mm,Hseries The module is compatiblewith eachother and canbeseamlesslyreplaced, and themodule is suitable for handheld smart POSand handheld PDA, cash register, robot, drone, smart home, security monitoring, multimedia terminal and other intelligent devices.

1.3Systeminterfaceperformanceparameters

Performance characteristics	Parameter description
CPU	MT8766,12nm,Quad-core ARM® Cortex-A53 2.0GHz
GPU	GE8300@660MHZ
RAM+ROM	eMCP LPDDR3, 1GB+8GB (default), 2GB+16GB (optional).
Z400-H3 operating system	Android12
Software upgrades	USB/OTA/SD card
Display interfaces	1 group of 4data lanes MIPI DSI interface (main screen), maximum support FHD+ 2400* 1080@60fps
Camera interface	2 sets of 4data lanes MIPI CSI-2 interfaces - Maximum support for a single group of 21MP@30fps - Support up to double group 13MP+ 8MP@30fps -Support YUV422/YUV420/EXIF/JFIF format
Analog audio interface	Audio input: -The module integrates a Mic bias output -3 sets of analog microphone input (MIC0/MIC2 configurable DMIC). Audio output (amplifiers are not supported inside the module): -1 single-ended stereo output with a maximum output of 0.93Vrms (S.E.) @32Ω -1 differential LINEout output, maximum output 1.88Vrms-vd@600Ω -1 differential handset output, 1.87Vrms-vd@32Ω
Digital I2S audio interface	**I2S2 Rx IF** -Master mode -1 data wires =>Up to 2-CHs -24bits up to 192KHz(Master) **I2S1 TX IF** -Master mode -1 data wires =>Up to 2-CHs -24bits up to 192KHz
USB interface	USB2.0 High Speed (HS) with a maximum data transfer rate of 480Mbps - Support OTG mode
(U) SIM interface	2 group (U) SIM interfaces supporting 1.8V/3.3 V adaptation -Support dual SIM dual standby (single pass), support hot plugging

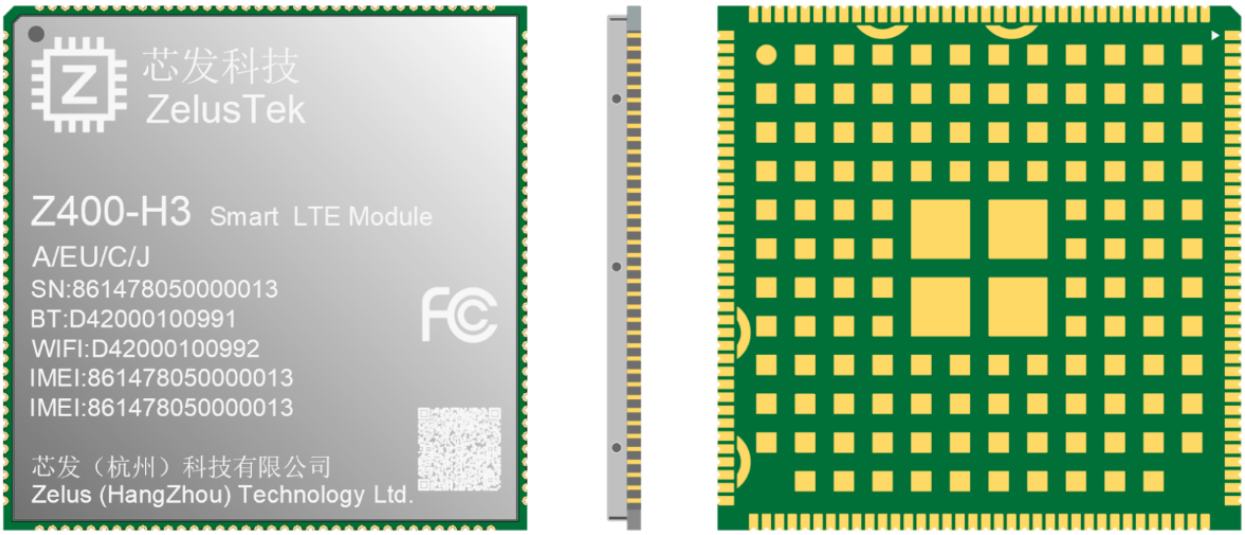
SD card interface	1 group of SDIO2.0/3.0 protocol interfaces, supporting SD/SDHC/MS/MSPRO/MMC - Supports up to 256GB
UART interface	1 set of four-wire function UART, supporting RTS/CTS hardware flow control (UART1). 1 group of two-wire debug UART,can be used as a function serial port (UART0). - FIFO RX/TX Independent FIFO,Max 8K byte -Baud rate 110bps~961200bps -Data bits 5~8bits - Stop bit 1or2stopbit -I/O address/IRQ 0x11020000 None, even, odd, space, mark
I2C interface	6 groups of I2C, supporting standard mode 100KHz and high-speed mode 400KHz -SOC internal hardware pulls up 5 K Ω by default, softwarecan change to1KΩ pull up or turn off pull-up
SPI interface	5 sets of hardware SPI Minimum data rate 0.8K bit/s Maximum data rate 27M bit/s
ADC interface	2 sets of Auxiliary ADC -Input range 0.05~1.45V -12-bits -Sampling rate 3.25/(N+8)MSPS@N-bit
RTC clock	In the tank
Antenna interface	Main antenna, DRX antenna, WiFi/BT/GNSS antenna
Physical characteristics	Dimensions: 40.5mmx40.5mmx2.8mm Package:LCC+LGA Weight:TBD
RoHS	Compliant with RoHs standards

1.4 RFperformanceparameters

Performance characteristics	Parameter description
Power class	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm+1/-2.7dB) for LTE-FDD bands Class 3 (23dBm+1/-2.7dB) for LTE-TDD bands
GSM/GPRS/ EDGE features	R99： CSD transmission rate: 9.6kbps, 14.4kbps GPRS: Supports GPRS multi-slot class 12 Encoding formats: CS-1/CS-2/CS-3 and CS-4 Up to 4 Rx time slots per frame EDGE： EDGE MULTI-SLOT CLASS 12 IS SUPPORTED GMSK and 8-PSK are supported

	Uplink encoding formats: CS 1-4 and MCS 1-9 Downstream encoding formats: CS 1-4 and MCS 1-9
WCDMA characteristics	Supports 3GPP R9 Supports 16-QAM, 64-QAM and QPSK modulation CAT7 HSUPA: Maximum uplink rate 11Mbps CAT14 CAT7 HSDPA: Maximum downstream rate 21Mbps
LTE characteristics	Supports 3GPP R10 Supports FDD/TDD CAT4 Supports 1.4-20M RF bandwidth downlink and supports 2 × 2 MIMO The maximum uplink rate is 50Mbps and the maximum downlink rate is 150Mbps
WLAN characteristics	Support 2.4G, 5G WLAN wireless communication, support 802.11b, 802.11g , 802.11n, 802.11acand other standards, the maximum speed can reach 433Mbps
Bluetooth features	BT5.0(BR/EDR+BLE)
GNSS characteristics	GPS/Beidou/GLONASS/Galileo, 4 out of3 positioning mode
Short message (SMS).	Text and PDU modes point-to-point MO and MT short message cell broadcasts Short message storage: Stored in modules by default

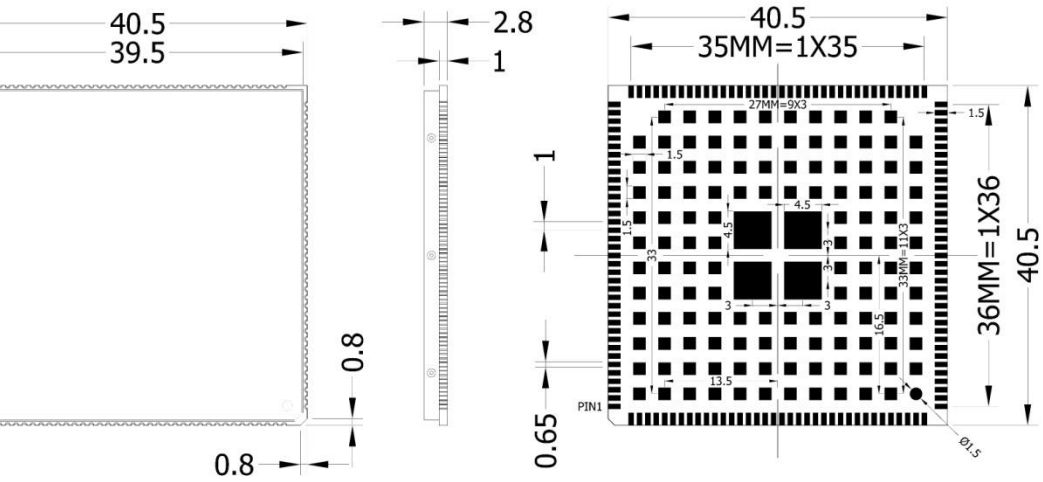
1.5 Product Appearance



2. Introduction to hardware

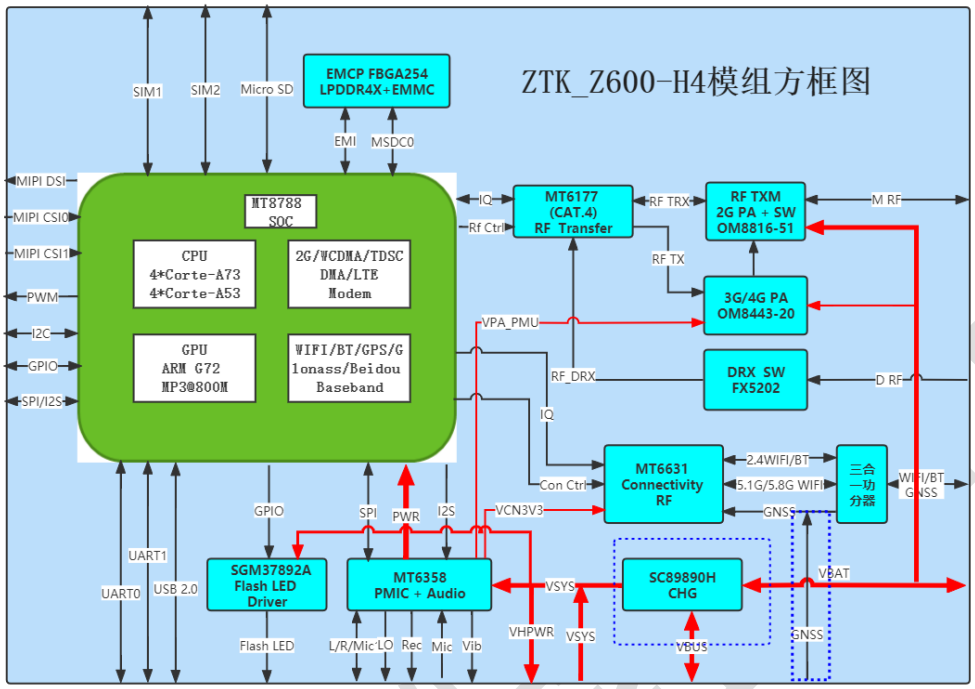
2. 1 Structural dimensions

Module package LCC+LGA 275PIN,size: 405mmx40.5mmx2.8mm



Module TOP view size (Unit: mm) ModuleBOT viewsize(Unit: mm).

2. 2 Hardware architecture to be updated



2.3 RF band

2.3.1 RFoperatingfrequency

Frequency Bands	Uplink(UL)	Downlink(DL)	Unit	Duplex Mode
GSM	850		MHz	
GSM	1900		MHz	
WCDMA B2	1852~1908	1932~1988	MHz	
WCDMA B4	1712~1753	2112~2153	MHz	
WCDMA B5	824~849	869~894	MHz	
LTE B2	1850~1910	1930~1990	MHz	FDD
LTE B4	1710~1755	2110~2155	MHz	FDD
LTE B5	824~849	869~894	MHz	FDD
LTE B7	2500~2570	2620~2690	MHz	FDD
LTE B12	699~716	729~746	MHz	FDD
LTE B13	777~787	746~756	MHz	FDD
LTE B17	704~716	734~746	MHz	FDD
LTE B25	1850~1915	1930~1995	MHz	FDD
LTE B26	814~849	859~894	MHz	FDD
LTE B66	1710~1780	2110~2200	MHz	FDD
LTE B71	663~698	617~652	MHz	FDD
LTE B38	2570~2620	2570~2620	MHz	TDD
LTE B41	2535~2655	2535~2655	MHz	TDD

2.3.2 GNSS operatingfrequency

Type	Frequency
GPS	1575.42±1.023MHz
Glonass	1597.5~1605.8MHz
Beidou	1561.098±2.046MHz

2.3.3 GNSS receivemode

GNSS receives simultaneously	GPS/Glonass/Beidou
	GPS/Glonass/Galileo
	GPS/Beidou/ Galileo

2.3.4 Data transfer rate

FDD-LTE	Uplink(UL)	50Mbps
	Downlink(DL)	150Mbps
TDD-LTE	Uplink(UL)	30Mbps
	Downlink(DL)	117Mbps
UMTS	HSUPA Uplink(UL)	5.76Mbps
	DC-HSDPA Downlink(DL)	21Mbps
	WCDMA Uplink(UL)	384Kbps
	WCDMA Downlink(DL)	384Kbps
GPRS	Uplink(UL)	85.6Kbps
	Downlink(DL)	85.6Kbps
EDGE	Uplink(UL)	236.8Kbps
	Downlink(DL)	236.8Kbps

2.3.5 Module conductiondata*HA versionconduction data*

Transmit power:

mode	Band	Maximum power (dBm).	Minimum power (dBm).
GSM	850 (GMSK)	33±2	5±5
	1900 (GMSK)	30±2	0±5
GSM	850 (8PSK)	27.0±3	5±5
	1900 (8PSK)	26.0±3	0±5
WCDMA	Band 2	24+1/-3	<-49
	Band 4	24+1/-3	<-49
	Band 5	24+1/-3	<-49
LTE FDD	Band 2	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39
	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39
	Band 17	23.0±2	<-39
	Band 25	23.0±2	<-39

	Band 26	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD	Band 38	23.0±2	<-39
	Band 41	23.0±2	<-39

Receive sensitivity: (data to be tested for update).

Standard	Band	Main collector antenna	Diversity antenna	3GPP standard	unit
GSM	850	-110	-	-102	dBm
	1900	-109	-	-102	dBm
WCDMA	Band 2	-110	-	-104.7	dBm
	Band 4	-110	-	-106.7	dBm
	Band 5	-111	-	-104.7	dBm
LTE FDD	Band 2（10MHZ）	-99.7	-98.9	-94.3	dBm
	Band 4（10MHZ）	-100	-99.7	-96.3	dBm
	Band 5（10MHZ）	-99.1	-98.6	-94.3	dBm
	Band 7（10MHZ）	-96.8	-97.3	-94.3	dBm
	Band 12（10MHZ）	-98.4	-98.9	-93.3	dBm
	Band 13（10MHZ）	-98.1	-99.4	-93.3	dBm
	Band 17（10MHZ）	-98.6	-98.7	-93.3	dBm
	Band 25（10MHZ）	-99.3	-99.4	-92.8	dBm
	Band 26（10MHZ）	-100	-98.9	-93.8	dBm
	Band 66（10MHZ）	-97.4	-97.6	-95.8	dBm
	Band 71（10MHZ）	-99.2	-99	-93.5	dBm
	Band 41（10MHZ）	-97.7	-98.9	-94.3	dBm

2.3.5.1 WiFi conductsdata

Transmit power:

frequency	Standard	speed	Bandwidth in MHz	Transmit power (dBm).
2.4G	802.11b	1Mbps	20	17±3
		11Mbps	20	17±3
	802.11g	6Mbps	20	16±3
		54Mbps	20	13±3
	802.11n	MCS0	20	15±3
		MCS7	20	13±3

5G	802.11a	6Mbps	20	15±3
		54Mbps	20	13±3
	802.11ac	MCS0	20	15±3
		MCS7	20	12±2

Receive sensitivity:(data to be tested for update).

frequency	Standard	speed	Bandwidth in MHz	Sensitivity (dBm).
2.4G	802.11b	1Mbps	20	-94.5
		11Mbps	20	-86.5
	802.11g	6Mbps	20	-90
		54Mbps	20	-73.5
	802.11n	MCS0	20	-87.5
		MCS7	20	-69.5
5G	802.11a	6Mbps	20	-95
		54Mbps	20	-78
	802.11ac	MCS0	20	-78
		MCS7	20	-72.5

2.3.5.2 Bluetooth conducts data

BT performance indicator:(data to be tested for update).

type	DH-5	2-DH5	3-DH5	BLE	unit
Transmit power	9.58	-2.54	-2.94	-5.27	dBm
sensitivity	-89	-89.5	-83.5	-86	dBm

2. 3. 5. 3 GNSS conduction data

features	description	Typical value	unit
Sensitivity	Cold start	147	dBm
	Reacquisition	157	dBm
	Tracking	156	dBm
TTFF	Cold start	33.7	S
	Warm start	6.6	S
	Hot start	1.2	S
Static Drift	CEP-50	0.7	m

2.3.6 Antenna specifications

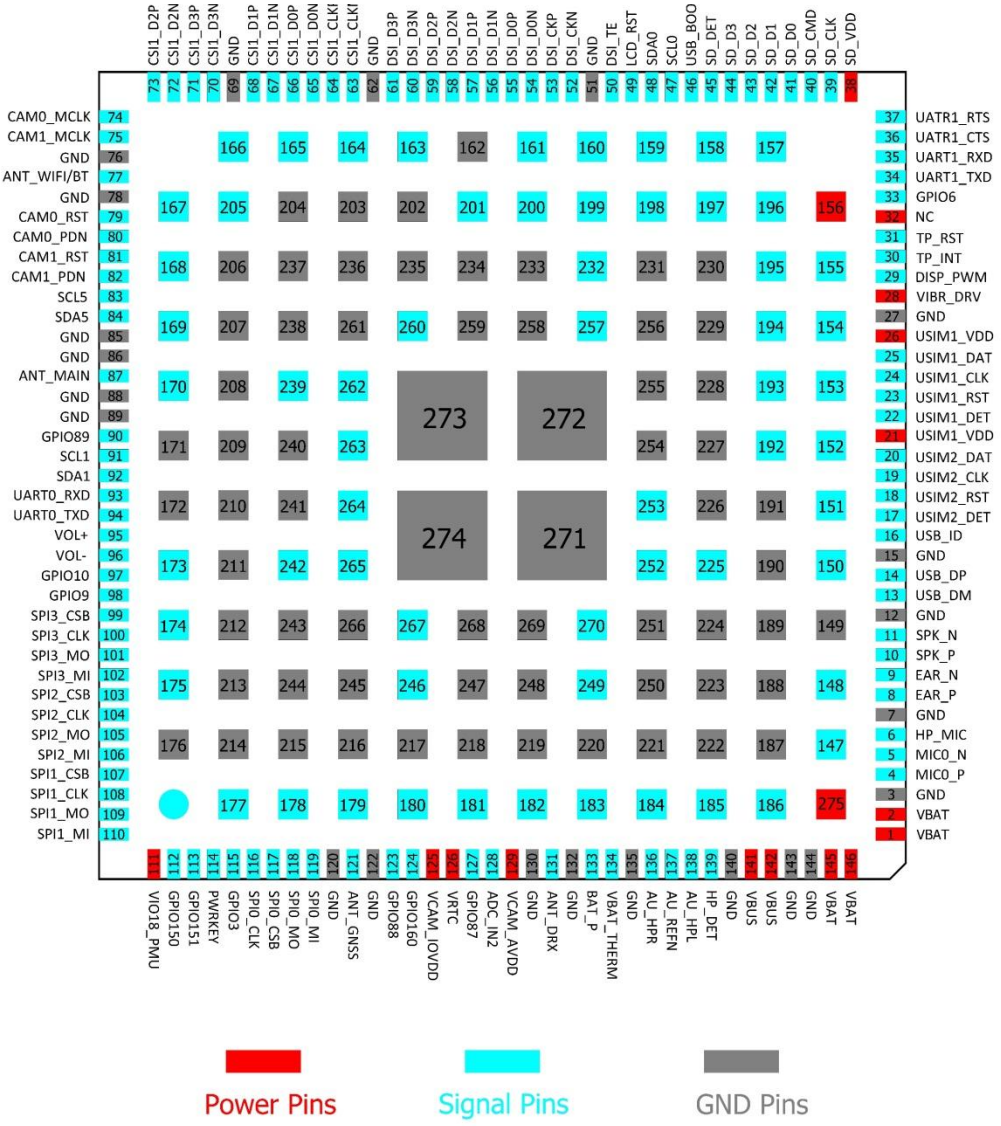
2.3.6.1 RF antennarequirements

Parameter	Requirements
Operating Frequency	See 2G/3G/4G *Operating Frequency*
Direction	Omni Directional
Gain	＞-3dBi(Avg)
Impedance	50 Ω
Efficiency	＞50%
Max. Input Power	50W
VSWR	＜2
Isolation	20dB is preferred
Cable Insertion Loss <1GHz	＜1dB
Cable Insertion Loss 1GHz~2.2GHz	＜1.5dB
Cable Insertion Loss 2.3GHz~2.7GHz	＜2dB
Cable Insertion Loss 3.3GHz~6GHz	＜2.5dB

2.3.6.2 GNSS antennarequirements

Parameter	Requirement
Operating Frequency	1559~1609MHZ
Direction	Hemisphere, face to sky
Antenna Gain	> 2dB
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Polarization	RHCP or Linear
Noise Figure for Active Antenna	< 1.5
Total Gain for Active Antenna	< 17 dB
Cable Insertion Loss	<1.5dB

2. 4 Module PIN assignment



Module PINdistributionmap(TOPperspective).

2.5 MODULOGROUP PINDEFINITION

2.5.1 The PIN definesthe assignment

1	VBAT	93	UART0_RXD	185	ADC_IN3
2	VBAT	94	UART0_TXD	186	GPIO172
3	GND	95	VOL+	187	CS_N
4	MIC0_P	96	VOL-	188	CS_P
5	MIC0_N	97	GPIO10	189	GND
6	HP_MIC	98	GPIO9	190	GND
7	GND	99	SPI3_CSB/I2S2_BCK	191	GND
8	EAR_P	100	SPI3_CLK/I2S2_DI	192	VCAMD_PMU
9	EAR_N	101	SPI3_MO/I2S2_LRCK	193	VLDO28_PMU

10	SPK_P	102	SPI3_MI/I2S2_MCK	194	GPIO_GPS_LNA_EN
11	SPK_N	103	SPI2_CSB	195	CHG_LED
12	GND	104	SPI2_CLK	196	CSI0_CLKP
13	USB_DM	105	SPI2_MO	197	CSI0_LN0P
14	USB_DP	106	SPI2_MI	198	CSI0_LN1P
15	GND	107	SPI1_CSB/I2S1_BCK	199	CSI0_LN2P
16	USB_ID	108	SPI1_CLK/I2S1_DO	200	CSI0_LN3P
17	USIM2_DET	109	SPI1_MO/I2S1_LRCK	201	GPIO168
18	USIM2_RST	110	SPI1_MI/I2S1_MCK	202	GND
19	USIM2_CLK	111	VIO18_PMU	203	GND
20	USIM2_DAT	112	GPIO150	204	GND
21	USIM2_VDD	113	GPIO151	205	SDA2
22	USIM1_DET	114	PWRKEY	206	GND
23	USIM1_RST	115	GPIO3	207	GND
24	USIM1_CLK	116	SPI0_CLK	208	GND
25	USIM1_DAT	117	SPI0_CSB	209	GND
26	USIM1_VDD	118	SPI0_MO	210	GND
27	GND	119	SPI0_MI	211	GND
28	VIBR_DRV	120	GND	212	GND
29	DISP_PWM	121	ANT_GNSS	213	GND
30	TP_INT	122	GND	214	GND
31	TP_RST	123	GPIO88	215	GND
32	NC	124	GPIO160	216	GND
33	GPIO6	125	VCAM_IOVDD	217	GND
34	UART1_TXD	126	VRTC	218	GND
35	UART1_RXD	127	GPIO87	219	GND
36	UART1_CTS	128	ADC_IN2	220	GND
37	UART1_RTS	129	VCAM_AVDD	221	GND
38	SD_VDD	130	GND	222	GND
39	SD_CLK	131	ANT_DRX	223	GND
40	SD_CMD	132	GND	224	GND
41	SD_D0	133	BAT_P	225	SYSRSTB
42	SD_D1	134	VBAT_THERM	226	GND
43	SD_D2	135	GND	227	GND
44	SD_D3	136	AU_HPR	228	GND
45	SD_DET	137	AU_REFN	229	GND
46	USB_BOOT	138	AU_HPL	230	GND
47	SCL0	139	HP_DET	231	GND
48	SDA0	140	GND	232	GPIO164
49	LCD_RST	141	VBUS	233	GND
50	DSI_TE	142	VBUS	234	GND
51	GND	143	GND	235	GND
52	DSI_CKN	144	GND	236	GND
53	DSI_CKP	145	VBAT	237	GND

54	DSI_D0N	146	VBAT	238	GND
55	DSI_D0P	147	MICBIAS0	239	GPIO169
56	DSI_D1N	148	MIC2_P	240	GND
57	DSI_D1P	149	MIC2_N	241	GND
58	DSI_D2N	150	NC	242	SPI4_CSB
59	DSI_D2P	151	VCDT	243	GND
60	DSI_D3N	152	NC	244	GND
61	DSI_D3P	153	GPIO7	245	GND
62	GND	154	GPIO8	246	NC
63	CSI1_CLKN	155	MICBIAS1	247	GND
64	CSI1_CLKP	156	VIO28_PMU	248	GND
65	CSI1_D0N	157	CSI0_CLKN	249	LED_B
66	CSI1_D0P	158	CSI0_LN0N	250	GND
67	CSI1_D1N	159	CSI0_LN1N	251	GND
68	CSI1_D1P	160	CSI0_LN2N	252	LED_G
69	GND	161	CSI0_LN3N	253	LED_R
70	CSI1_D3N	162	GND	254	NC
71	CSI1_D3P	163	GPIO107	255	GND
72	CSI1_D2N	164	GPIO109	256	GND
73	CSI1_D2P	165	GPIO108	257	NC
74	CAM0_MCLK	166	SCL2	258	GND
75	CAM1_MCLK	167	SCL3	259	GND
76	GND	168	SDA3	260	BPI_BUS5
77	AN_WIFI/BT/GNSS	169	SCL4	261	GND
78	GND	170	SDA4	262	BPI_BUS6
79	CAM0_RST	171	GND	263	NC
80	CAM0_PDN	172	GND	264	SPI4_MO
81	CAM1_RST	173	BPI_BUS7	265	SPI4_MI
82	CAM1_PDN	174	NC	266	GND
83	SCL5	175	NC	267	GPIO152
84	SDA5	176	GND	268	GND
85	GND	177	GPIO165	269	GND
86	GND	178	GPIO176	270	SPI4_CLK
87	ANT_MAIN	179	GPIO167	271	GND
88	GND	180	FLASH_LED	272	GND
89	GND	181	NFC_CLK	273	GND
90	GPIO89	182	GPIO166	274	GND
91	SCL1	183	NC	275	VSYS
92	SDA1	184	VPH_PWR		

2.5.2 Description of the PIN feature

Pin name	Pin number	Electrical characteristics	Pin function description	remark
Power connector				
VBUS	141,142	input	USB VBUS/charging power input	Input range 5~12V
VBAT	1,2,145,146	Input/output	Battery interface	Support high voltage battery 4.35V
VCDT	151	input	VBUSdetects the divider interrupt	Refer to the VCDTdivider shunt resistor design
VIO18_PMU	111	output	System 1.8V I/Opower supply	It cannot be used to power external devices Can only be used forIOpull-up levels
VIO28_PMU	156	output	System 2.8V I/Opower supply	It cannot be used to power external devices Only available for IO pull-up levels
VPH_PWR	184	output	VSYS output power supply	Maximum output 1000mA
VSYS	275	Input/output	VSYS power supply	Connect to the system when using the external charging function
VLDO28_PMU	193	output	2.8V LDOpower supply	2.8/ 3.0V@400mA
VRTC	126	Input/output	RTCclock power supply	Max 3.3V@2mA
VCAM_IOVDD	125	output	MIPIcamera1.8V power supply	1.8V@300mA
VCAM_AVDD	129	output	MIPI camera analog power supply	1.8/2.5/2.7/2.8/2.9/2.95/3.0V@200mAdefault2.8Voutput
VCAMD_PMU	192	output	MIPI camera digital power supply	1.0/1.05/1.1/1.2V@300mA Default 1.2Voutput
GND	3,7,12,15 27,51,62,69 ,76,7 8,85,86,88, 89,120,122, 130,132,1 35,140,143, 144,162, 171,172,17 6,189,190 191,202,20 3,204,206,2 07,208,209, 210,211 ,21 2,213,214,2	ground	ground	

	15,2 16,217,218, 219,220 ,22 1,222,223,2 24,226 227,228,22 9,230,231,2 33,234,235, 236,237 ,23 8,240,241,2 43,2 44,245,247, 248,250 ,25 1,255,256,2 58,259 261,266,26 8,269,271,2 72,273,274			
Battery interface				
CS_P	188	input	PMICinternal coulomb meter sampling positive electrode	
CS_N	187	input	PMIC internal coulomb counter sampling negative electrode	
BAT_P	133	input	PMICinternal ADCsampling	
VBAT_THERM	134	input	Battery NTCsampling	
CHG_LED	195	Lose	Charging indicator control	
Analog audio interface				
MICBIAS0	147	output	MIC0/MIC2bias voltage	
MIC0_P	4	input	Analog MIC0inputpositive	
MIC0_N	5	input	Analog MIC0inputnegative terminal	
MIC2_P	148	input	Analog MIC2inputpositive	
MIC2_N	149	input	Analog MIC2inputnegative terminal	
EAR_P	8	output	Differential handset output positive	
EAR_N	9	output	Differential handset output negative pole	
SPK_P	10	output	Differential line out output positive	External amplifier input positive pole
SPK_N	11	output	Differential line out outputs the negative pole	External power amplifier input negative pole
AU_HPR	136	output	The headphones simulate the right channel output	
AU_REFN	137	input	Headphones reference ground input	Headphone single point loop reference
AU_HPL	138	output	The headphones simulate	

			the left channel output	
HP_DET	139	input	Headphone plug and unplug detection	The detection level software is configurable
HP_MIC	6	input	The headphones simulate MICinputs	
MICBIAS1	155	output	The headphones simulate the MICbias voltage	
USB interface				
VBUS	141,142	Input/output	USB VBUS/charging power input	Input range 5~12V
USB_DM	13	DataO	USB2.0dataDM	
USB_DP	14	DataO	USB2.0dataDM	
USB_ID	16	input	USB OTGmode switching	The module internally pulls up100Kresistors by default
USIM				
USIM1_DET	22	input	SIMcard 1 hot-swap detectioninterrupt	USIM_VDD 1.7/1.8/1.86/2.76/3.0/3.1V @200mAdefault1.86V The two sets of S IMcard signals can only be used for SIMcard purposes, not for other purposes
USIM1_RST	23	output	SIMcard 1resets the output	
USIM1_CLK	24	output	SIMcard1clock output	
USIM1_DAT	25	DataO	SIMcard1data	
USIM1_VDD	26	output	SIMcard1power output	
USIM2_DET	17	input	SIM card2hot-swap detectsinterrupts	
USIM2_RST	18	output	SIM card2reset output	
USIM2_CLK	19	output	SIM card1clock output	
USIM2_DAT	20	DataO	SIM card1data	
USIM2_VDD	21	output	SIM card1power output	
SD Card				
SD_VDD	38	output	SDcard power output	2.9/3.0/3.3V@800mA Default3.0V
SD_CLK	39	output	SDcard clock output	
SD_CMD	40	output	SDcard command output	
SD_D0	41	DataO	SDcard dataIO	
SD_D1	42	DataO	SDcard dataIO	
SD_D2	43	Data IO	SD card dataIO	
SD_D3	44	Data IO	SD card dataIO	
SD_DET	45	Data IO	SDcard hot plug detection	
Main MIPIdisplayinterface				
DSI_CKN	52	output	DSIdifferential clock negative pole	
DSI_CKP	53	output	DSI differential clock positive	
DSI_D0N	54	output	DSI differential data0negative terminal	
DSI_D0P	55	output	DSI differential data0positive	
DSI_D1N	56	output	DSI differential data1negative terminal	

DSI_D1P	57	output	DSI differential data1positive	
DSI_D2N	58	output	DSI differential data2negative pole	
DSI_D2P	59	output	DSI differential data2positive	
DSI_D3N	60	output	DSI differential data3negative pole	
DSI_D3P	61	output	DSI differential data3positive pole	
LCD_RST	49	output	MIPIscreen reset output	1.8V I/Olevel
DSI_TE	50	input	MIPIscreenTearing Effectinput	
DISP_PWM	29	output	Main display backlit PWMcontrol	
Camera 1interface				
CSI1_CLKN	63	output	CSIdifferential clock negative terminal	
CSI1_CLKP	64	output	CSI differential clock positive	
CSI1_D0N	65	input	CSI differential data0negative terminal	
CSI1_D0P	66	input	CSI differential data0positive	
CSI1_D1N	67	input	CSI differential data1negative terminal	
CSI1_D1P	68	input	CSI differential data1positive terminal	
CSI1_D2N	72	input	CSI differential data2negative pole	
CSI1_D2P	73	input	CSI differential data2positive pole	
CSI1_D3N	70	input	CSI differential data3negative pole	
CSI1_D3P	71	input	CSI differential data3positive	
CAM1_MCLK	75	output	Sensormaster clock output	DEFAULT 24MHz
CAM1_RST	81	output	Sensor reset output	1.8V I/Olevel
CAM1_PDN	82	output	Sensor enable output	
Camera 0interface				
CSI0_CLKN	157	output	CSI differential clock negative terminal	
CSI0_CLKP	196	output	CSI differential clock positive	
CSI0_LN0N	158	input	CSI differential data0negative terminal	
CSI0_LN0P	197	input	CSI differential data0positive	
CSI0_LN1N	159	input	CSI differential data1negative terminal	
CSI0_LN1P	198	input	CSI differential	

			data1positive terminal	
CSI0_LN2N	160	input	CSI differential data2negative pole	
CSI0_LN2P	199	input	CSI differential data2positive pole	
CSI0_LN3N	161	input	CSI differential data3negative pole	
CSI0_LN3P	200	input	CSI differential data3positive	
CAM0_MCLK	74	output	Sensor master clock output	The default is 24MHz
CAM0_RST	79	output	Sensor reset output	1.8V I/Olevel
CAM0_PDN	80	output	Sensor enable output	
Flash connector				
FLASH_LED	180	output	FLASH LED light positive output	Maximum drive current 700mA
Capacitive touch screeninterface				
SCL0	47	output	I2C0clock output	
SDA0	48	DataO	I2C0dataIO	
TP_INT	30	input	Touch screen interrupt input	
TP_RST	31	output	Touch screen reset output	
UART interface				
UART1_TXD	34	output	UART1data sending	
UART1_RXD	35	input	UART1data reception	
UART1_CTS	36	output	UART1data request	
UART1_RTS	37	input	UART1data response	
UART0_RXD	93	input	UART0data reception	The default system debug can support function UART (changesoftwaredriver).
UART0_TXD	94	output	UART0data sending	
I2C interface				
SCL1	91	output	I2C1 clock output	
SDA1	92	DataO	I2C1 dataIO	
SCL2	166	output	I2C2 clock output	
SDA2	205	DataO	I2C2 dataIO	
SCL3	167	output	I2C6 clock output	Compatible Z600-Hmotherboardsmusthave an external pull-up resistor
SDA3	168	DataO	I2C6 dataIO	
SCL4	169	output	I2C4 clock output	
SDA4	170	Data IO	I2C4 dataIO	
SCL5	83	output	I2C5 clock output	
SDA5	84	DataO	I2C5 dataIO	
SPIinterface				
SPI0_CSB	117	output	SPI1chip select output	
SPI0_CLK	116	output	SPI1clock output	
SPI0_MO	118	output	SPI1data output	
SPI0_MI	119	input	SPI1data entry	
SPI1_CSB	107	output	SPI4 chip select output	Reuse I2S1_OUT
SPI1_CLK	108	output	SPI4 clock output	

SPI1_MO	109	output	SPI4 data output	
SPI1_MI	110	input	SPI4 data entry	
SPI2_CSB	103	output	SPI2chip select output	
SPI2_CLK	104	output	SPI2clock output	
SPI2_MO	105	output	SPI2data output	
SPI2_MI	106	input	SPI2data entry	
SPI3_CSB	99	output	SPI3chip select output	Reuse I2S0_IN
SPI3_CLK	100	output	SPI3clock output	
SPI3_MO	101	output	SPI3data output	
SPI3_MI	102	input	SPI3data entry	
SPI4_CSB	242	output	SPI4chip select output	
SPI4_CLK	270	output	SPI4clock output	
SPI4_MO	264	output	SPI4data output	
SPI4_MI	265	input	SPI4data entry	
I2S output interface				
I2S3_MCK	110	output	I2S master clock output	Reuse SPI1
I2S3_LRCK	109	output	I2S left and right clock output	
I2S3_BCK	107	output	I2S bit clock output	
I2S3_DO	108	output	I2S data output	
I2S input interface				
I2S0_MCK	102	output	I2S master clock output	Reuse SPI3
I2S0_LRCK	101	output	I2S left and right clock output	
I2S0_BCK	99	output	I2S bit clock output	
I2S0_DI	100	input	I2S data entry	
ADCinterface				
ADC_IN2	128	input	ADCanalog sampling input	Input range 0.05~1.45V
ADC_IN3	185	input	ADC analog sampling input	Input range 0.05~1.45V
Key interface				
PWRKEY	114	input	Power on and off button input	The level is equal tothe VBATvoltage
VOL+	95	input	Volume +key signal input	
VOL-	96	input	Volume-keysignal input	
USB_BOOT	46	input	Force upgrade key input	The input high enters upgrade mode
SYSRSTB	225	input	System reset signal input	
LEDstatus light				
LED_R	253	output	LEDlamp negative electrode	The positive terminal of motherboard LEDrequires a current limitingresistor
LED_G	252	output	LEDlamp negative electrode	
LED_B	249	output	LEDlamp negative electrode	
Motor interface				
VIBR_DRV	28	output	Vibrate the positive electrode of the motor	1.2V/1.3V/1.5V/1.8V/2.0V/2.8V/3.0V/3.3V@200mA, default2.8Voutput
Antenna port				

AN_WIFI/BT/GNSS	77	Input/output	WIFI/BT/GNSSthree-in-one day line	Default three-in-one dayline
ANT_GNSS	121	input	GNSSstandalone antenna	Default NC
ANT_MAIN	87	Input/output	RF main antenna	
ANT_DRX	131	input	RFdiversity antenna	
RF Tuner control interface				
BPI_BUS5	260	output	Antenna Tunerswitch control	Private, no other use
BPI_BUS6	262	output	Antenna Tunerswitch control	
BPI_BUS7	173	output	Antenna Tunerswitch control	
External GPS LNAenabled				
GPIO91	194	output	Motherboard GPS LNAenable control	Private, no other use
GPIOinterface				
GPIO166	182	Input/output		
GPIO165	177	Input/output		
GPIO176	178	Input/output		
GPIO167	179	Input/output		
GPIO89	90	Input/output		
GPIO3	115	Input/output		
GPIO88	123	Input/output		
GPIO160	124	Input/output		
GPIO87	127	Input/output		
GPIO7	153	Input/output		
GPIO8	154	Input/output		
GPIO172	186	Input/output		
GPIO168	201	Input/output		
GPIO164	232	Input/output		
GPIO169	239	Input/output		
GPIO152	267	Input/output		
GPIO107	163	Input/output		

GPIO109	164	Input/output		
GPIO108	165	Input/output		
Other features				
NFC_CLK	181	output	Clock output	
NC	32,150, 152,174,175 183,246,254 257,263			

2. 6 Electrical parameters

2.6.1 Power supply characteristics

Parameter	Description	Min	Type	Max	Unit
VBAT	Power Supply	3.5	3.8	4.4	V
I_{peak}	Peak current			3000	mA
I_{sleep}	Current in sleep mode			TBD	mA
$I_{leakage}$	Current in power off mode			TBD	uA

2.6.2 I/O electrical characteristics

Voltage Domain	Parameter	Min	Type	Max
VOH	High level output	1.35V	1.8V	1.98V
VOL	Low level output	0V	-	0.45V
VIH	High level input	1.26V	1.8V	1.98V
VIL	Low level input	0V	-	0.54V

2.6.3 Module scene power consumption(to be measured).

Parameter	Description	Conditions	Typ.	Unit
I_{BAT}	OFF state	Power down		uA
	Sleep state			

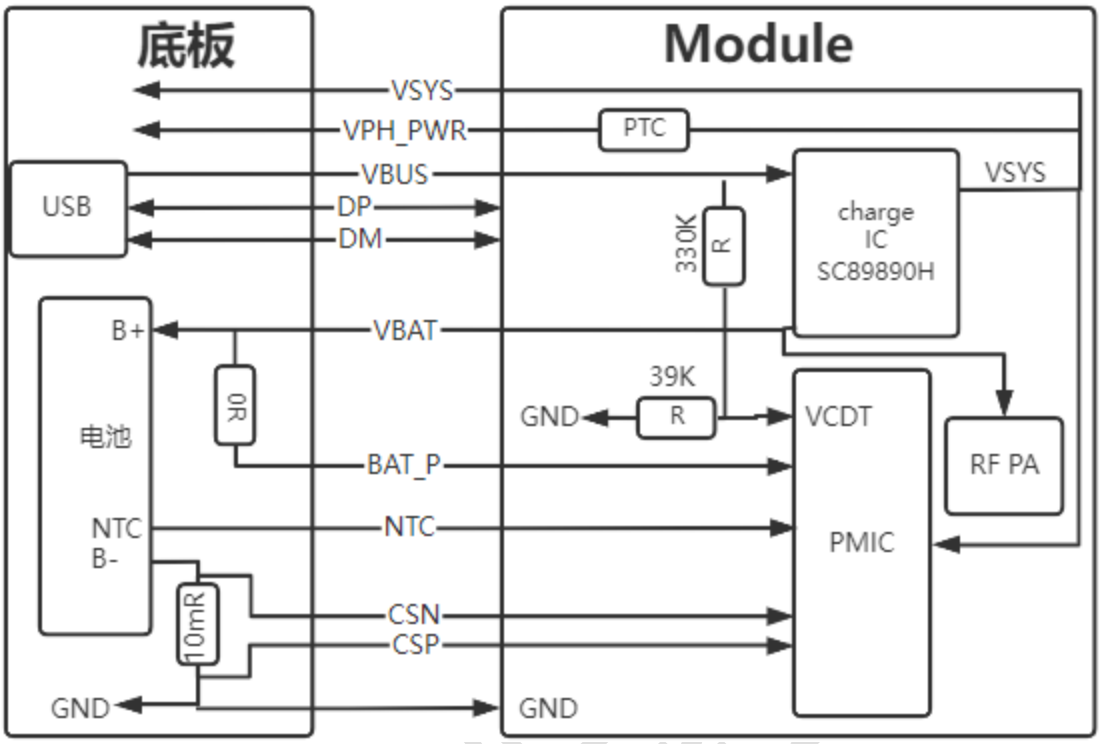
3. Environment and reliability

project		specification	remark
Working environment	temperature	TBD	
	humidity	TBD	
Storage environment	temperature	-50℃～90℃	
	humidity	Relative humidity 5%~93%,no condensation	
Degree of protection		/	
Environmental certification		National push RoHS	

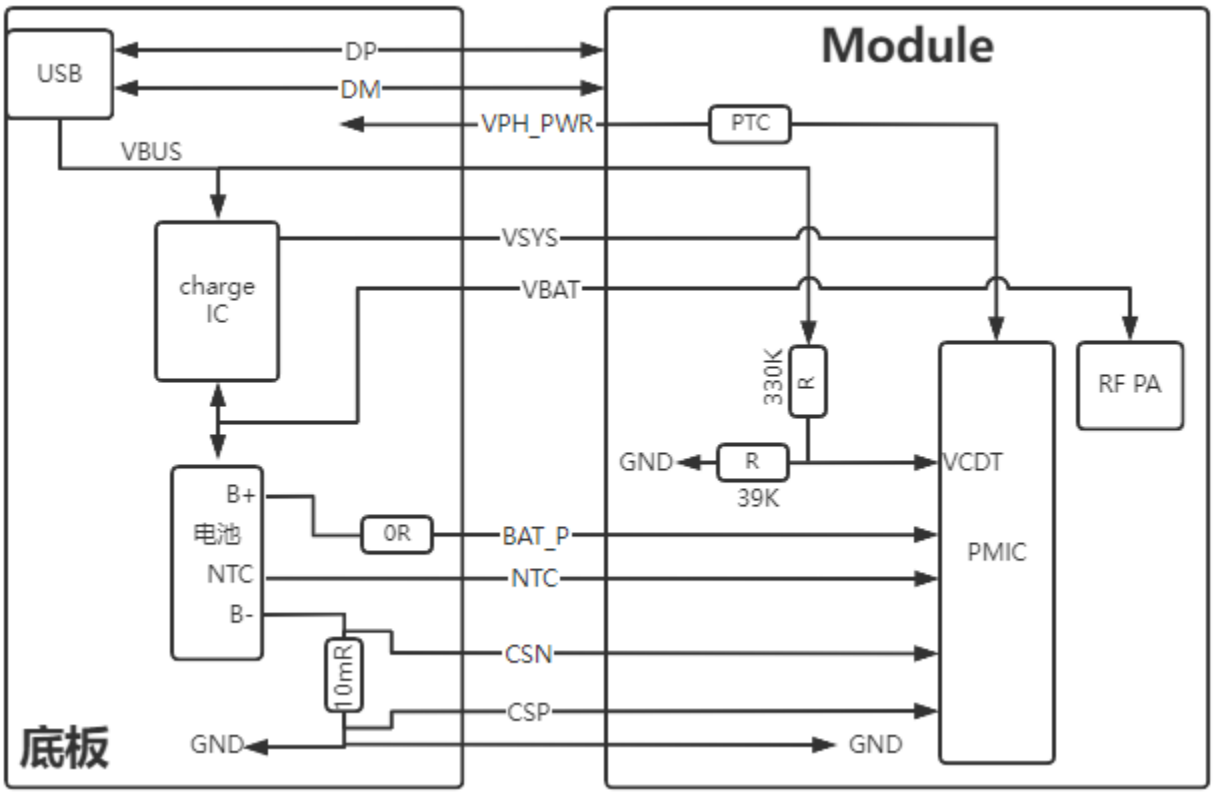
4. Hardware interface design (to be improved).

4.1.1 Power interface design

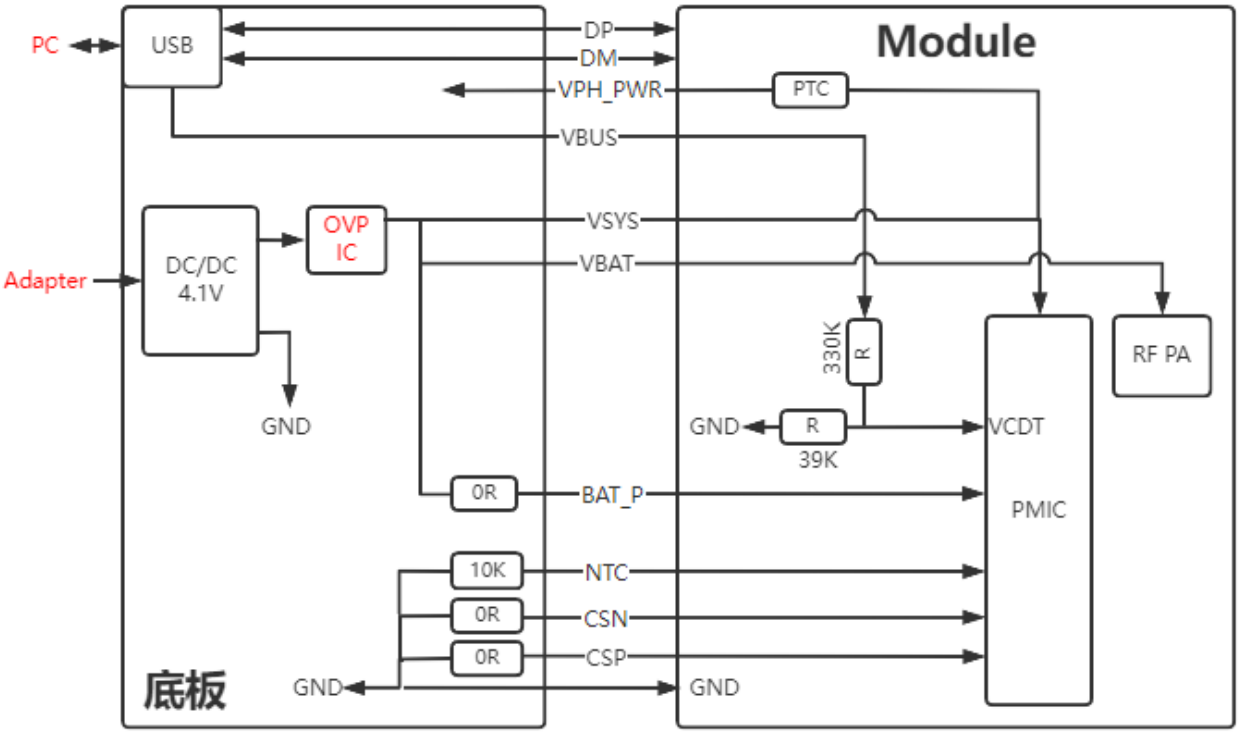
- The module supports internal charging function, module external charging function and no internal charging function, and the default module has internal charging function
- The internal VPH_PWR of the module outputs a load capacity of 1000mA
- The internal charging function of the module supports single-cell batteries, and the N TC resistance at the battery endis 10K by default
- The 10mR sampling resistor needs to be close to the battery interface, and the CSN/CSPcurrent sampling (coulombmeter) signal design is designed in a differential stereoscopic package design
- BAT_P voltage sampling needs to be connected close to the battery interface at a single point, and the input voltage range is 2.5~4.5V
- VBUS input voltage range 5~12V, when the V BUSinput is greater than 1 by defaultin the shutdown state 0.5V(VCDTdetects HW OVPvalue 10.5V), the V CDTdivider shunt resistor designneeds to be added
- No charging function design must beV.BAT&VSYSinputEnd increaseOVPProtection, protection voltage <4.45V
- When the design without charging function, the input voltage range of VBAT&VSYSis 3.5V~4.35V@3000mA , typical3.8V



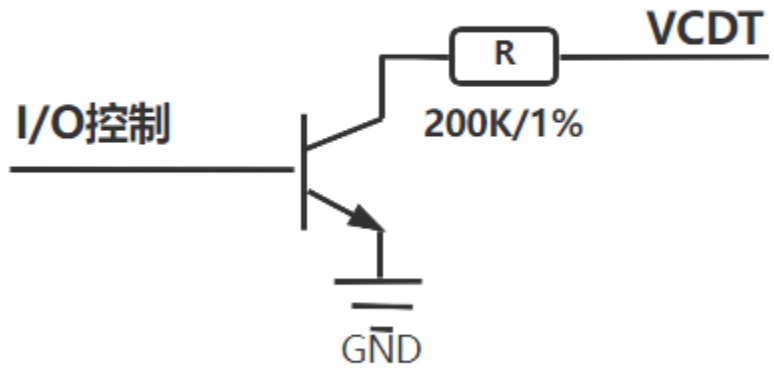
Module internal charging ICdesign



Module external charging ICdesign



No charging function design

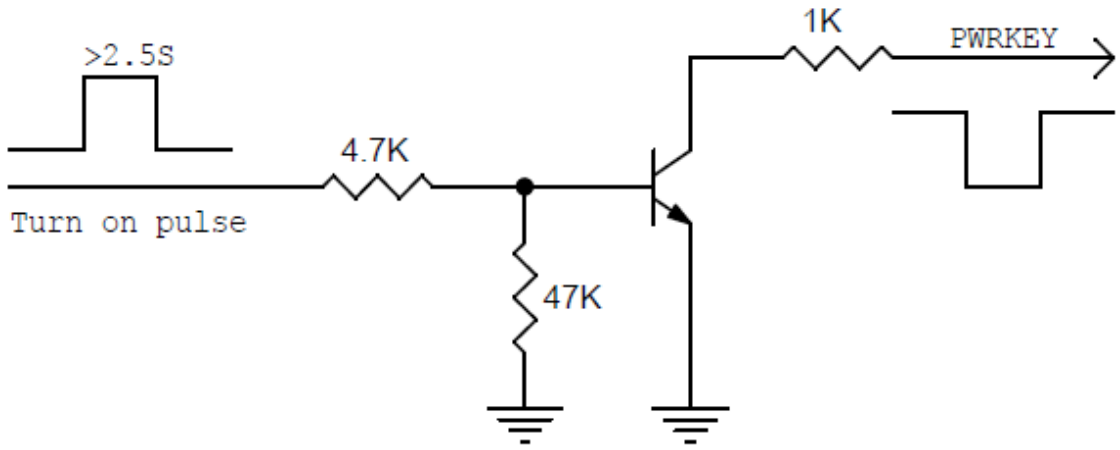


VCDT divider shunt resistor design

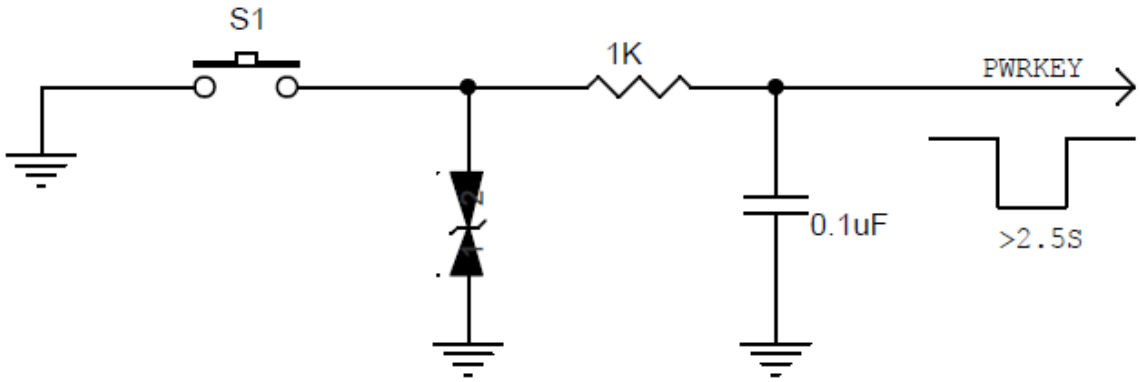
4.1.2 Module power on and off control

4.1.2.1.1 The module boots

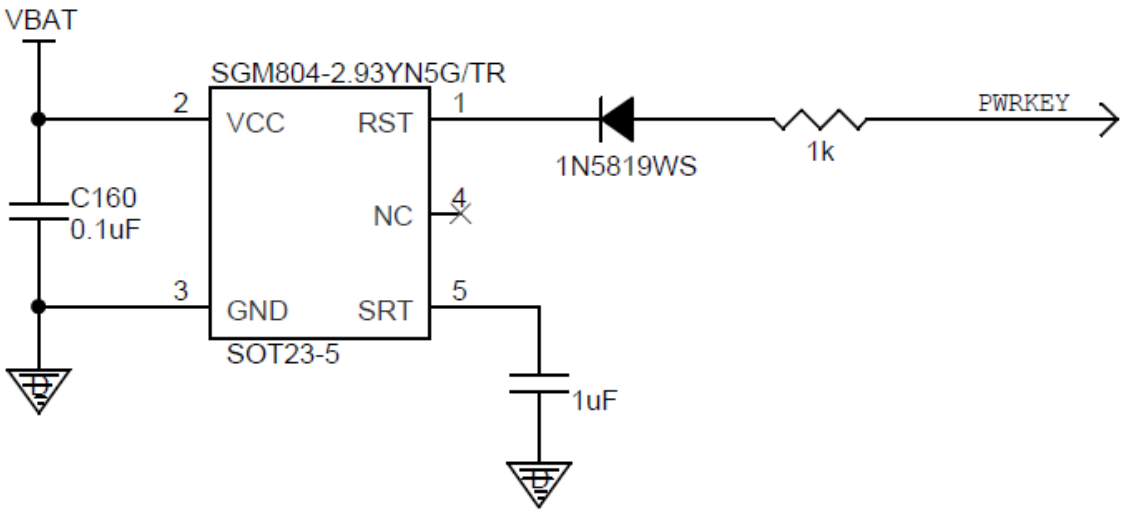
- After the VBAT is powered on,pull down the PWRKEY for at least2.5 seconds to power on the module
- PWRKEY signal PMIC is internally pulled up to the VBAT voltage, and the motherboard cannot be connected to a pull-up resistor
- After the PWRKEY signal is turned on, it needs to return to the high level and cannot be pulled low all the time (it will shut down or restart).



Power on mode1



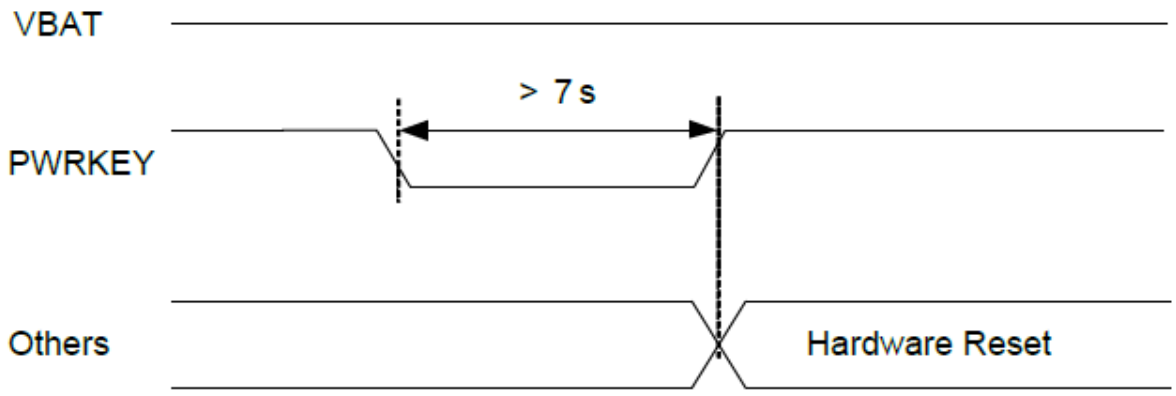
Power on mode 2



Boot mode 3(automatic power on).

4.1.2.1.2 The module shuts down

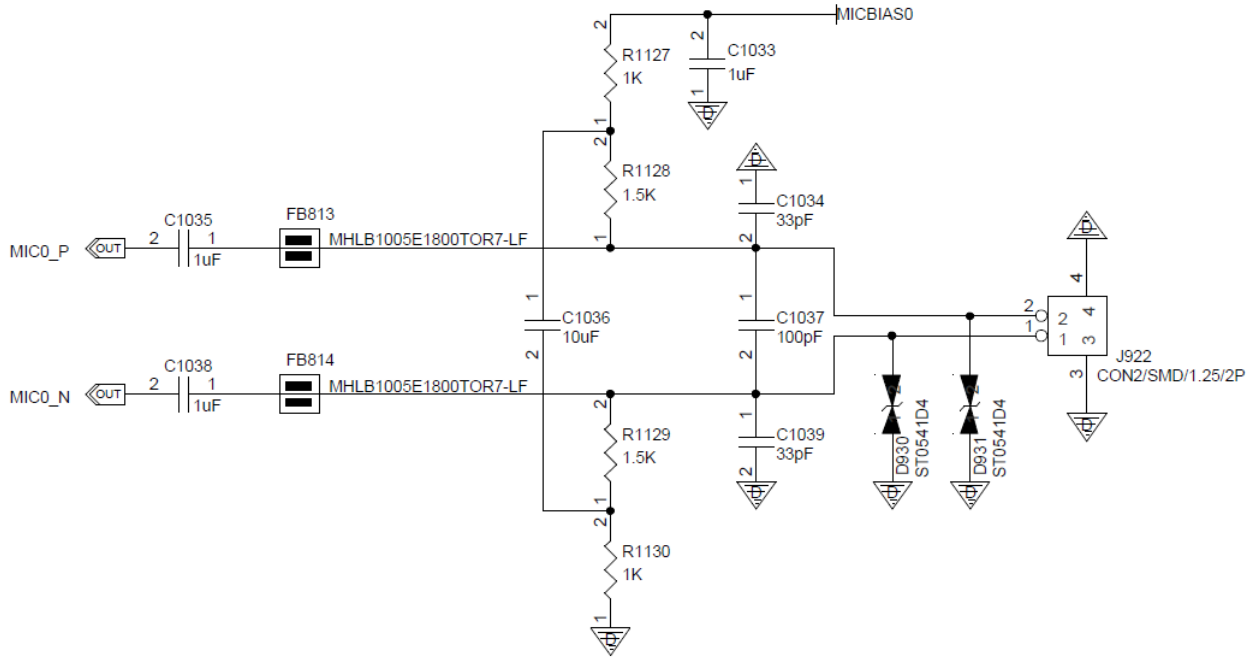
- In the boot state to detect PWRKEY pull-down greater than1 second, the Android system will have a prompt window pop up, the user confirms that click the shutdown menu to perform shutdown(IT IS ALSO POSSIBLETO ACHIEVE A FORCED RESTART BY PULLING DOWN THE P-WRKEY FOR 7 SECONDS).



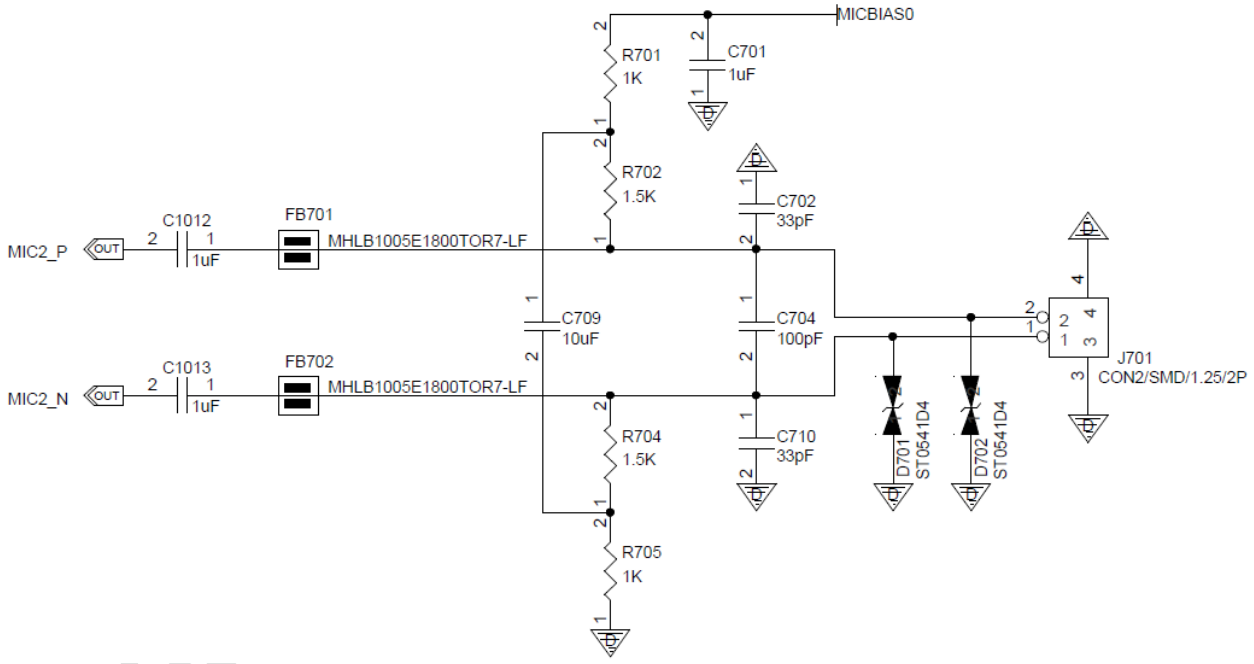
4.1.3 Analog audio interface

4.1.3.1.1 Analog MICinput

- The module supports 2sets of analog MICinputs
- Integrated Micbias voltage output
- MIC_P/N signal differential stereoscopic ground wrapping
- Micbias is paranoid power pack

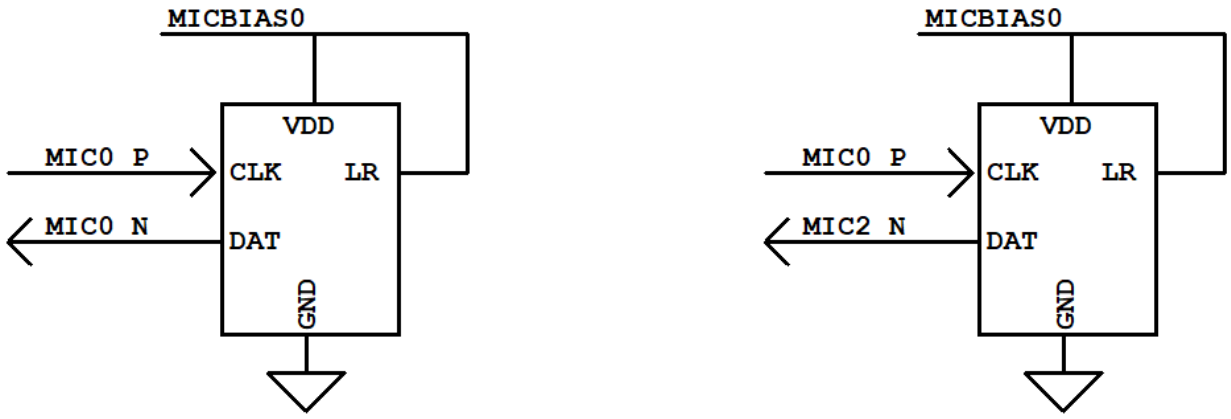


Analog MIC0input



Analog MIC2input

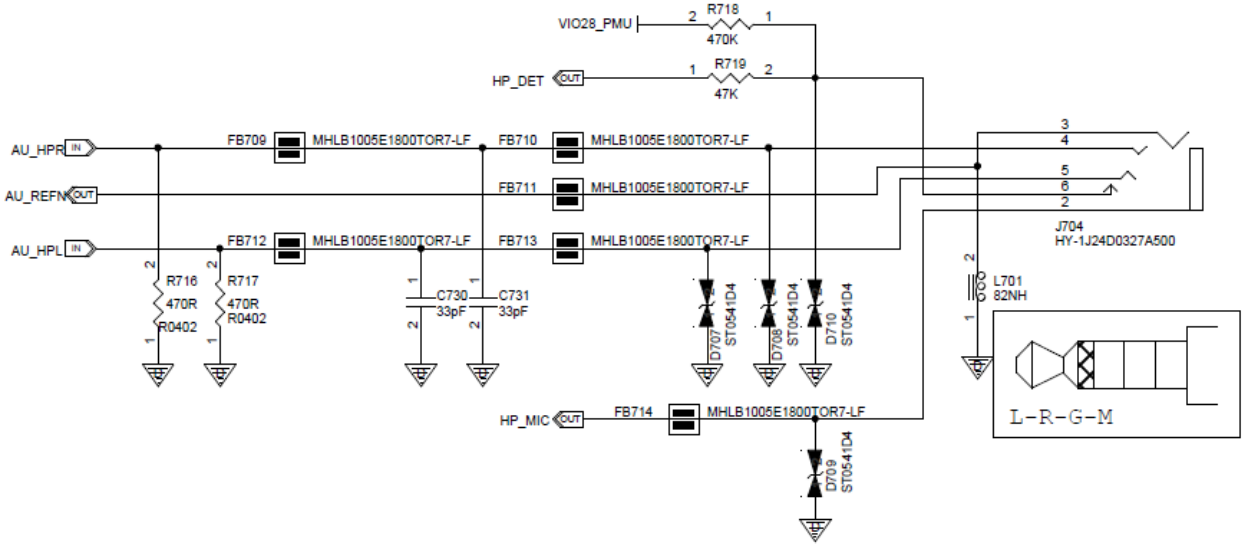
4.1.3.1.2 Digital DMICinput



Digital DMICinput

4.1.3.1.3 Analog headphone output

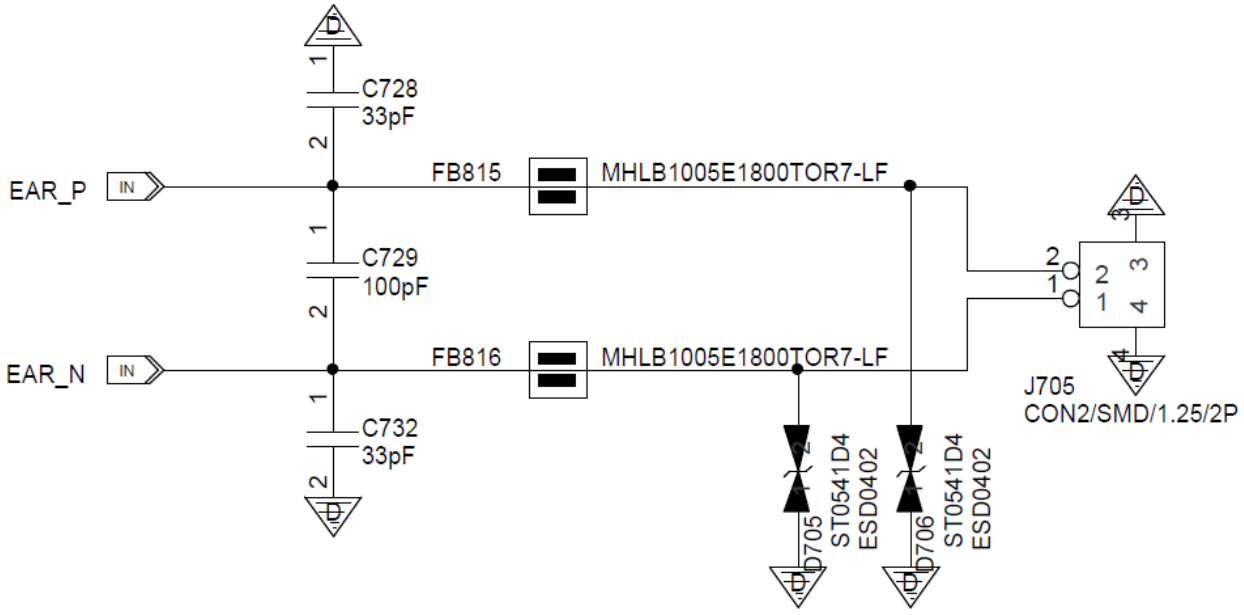
- Plug and unplug the headphones to pull up the detection signal to level VIO28_PMU
- AU_HPR/AU_REFN/AU_HPL signals are packaged in parallel stereoscopic land
- HP_MIC signal stereoscopic ground wrapping



Analog headphone output(withMIC).

4.1.3.1.4 Analog handset output

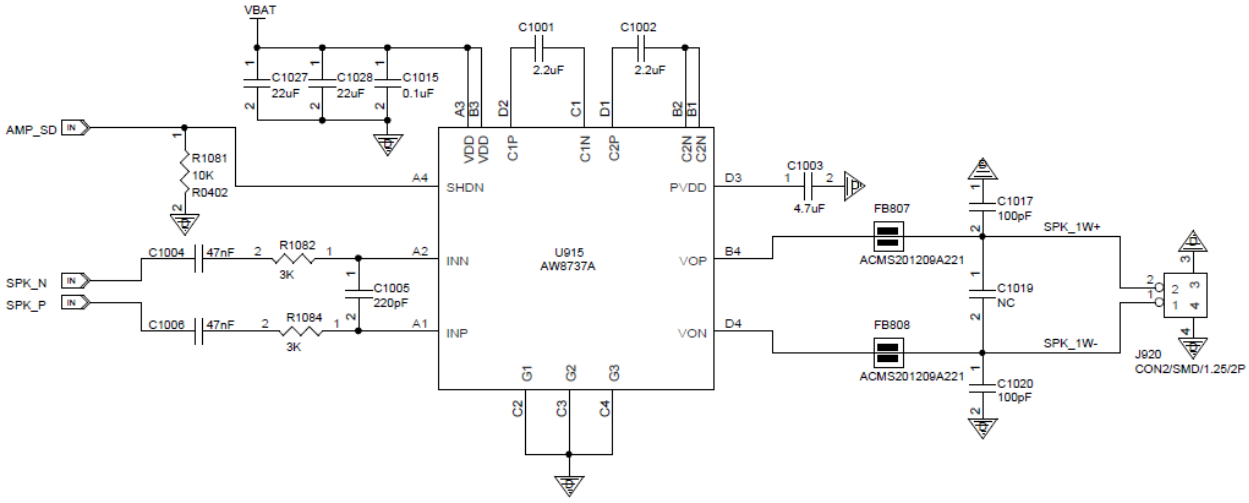
- EAR_P/EAR_Nsignaldifferential stereoscopic ground wrapping



Handset output

4.1.3.1.5 Line out speakeroutput

- EAR_P/EAR_N signal differential stereoscopic ground wrapping
- Stay away from interference sources such as RF antenna \ DC-DC



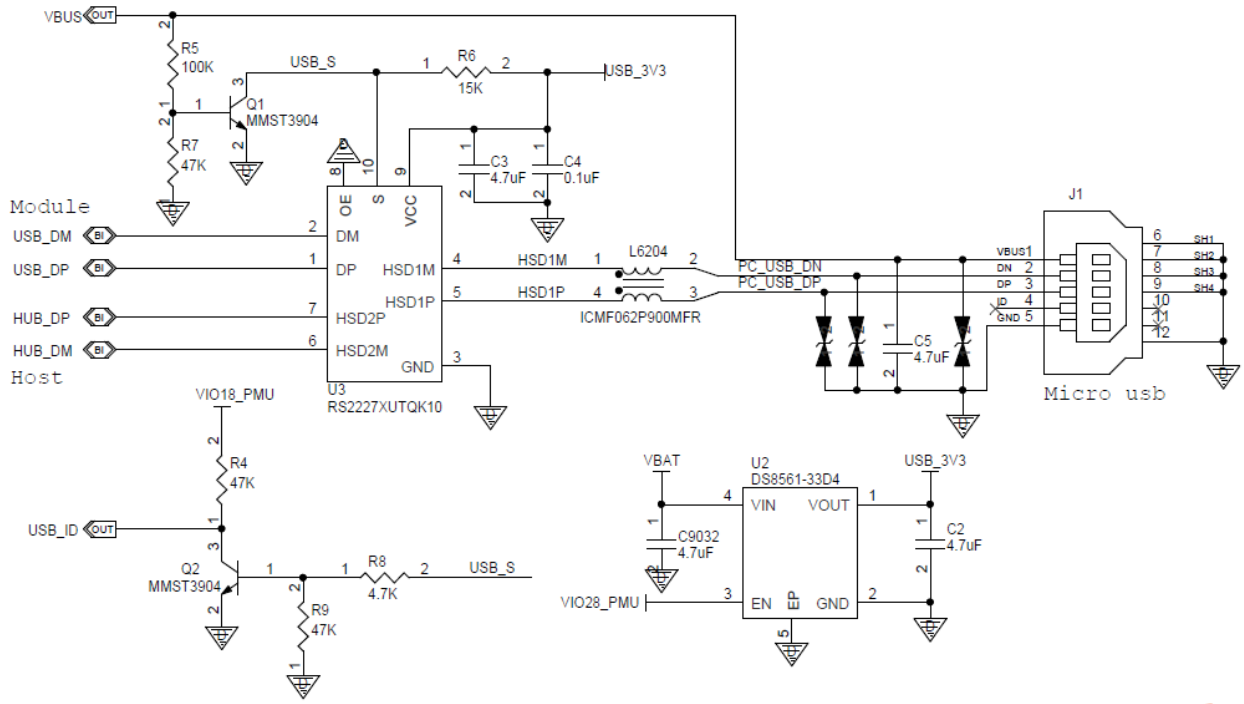
Line outspeaker output

4.1.4 USBinterface design

- The USBinterface conforms to the U SB2.0 specification and supportsUSB2.0high-speed 480Mbps
- The USBinterface is used for software upgrades and development and debugging
- Support USB OTG mode, U SB_ID switch D evice and Host mode, U SB_IDhighlevel

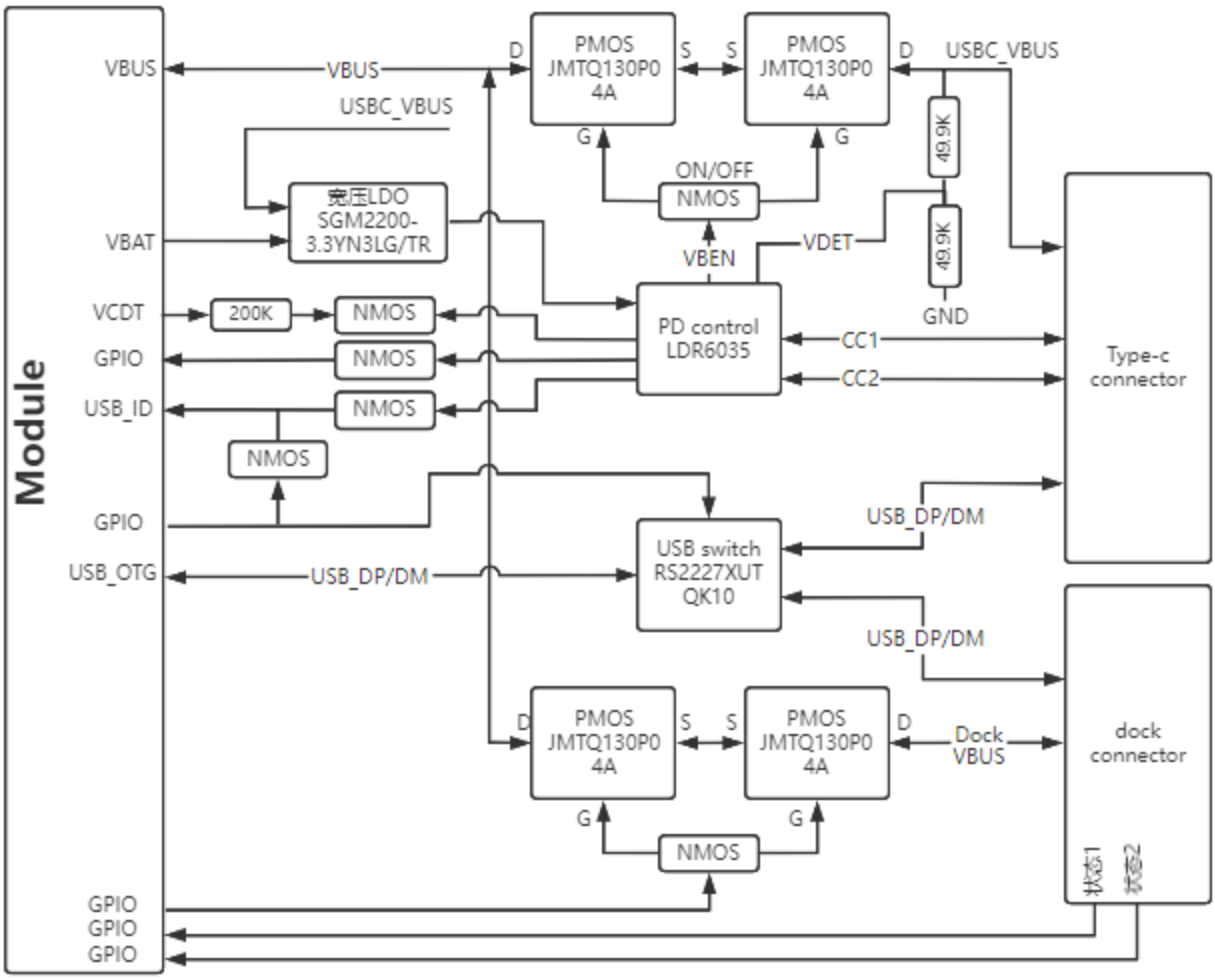
Device mode, USB_ID When the host mode is low,Device and host cannot be used at the same time

- VBUSsupports external output of 5Vpower supply (requires internal charging of the module).
- USB DP/DMsignal motherboard PCBneeds to differ the distribution line and stereoscopic package processing and differential impedance control 90Ω±5Ω



No charging function USBinterface design

Note:No charging function design, Vbuspower supply willautomatically switch between U **SBelectronic switch andUSB_IDDevicestatus**



Charging function Type-c withDock design

Note：

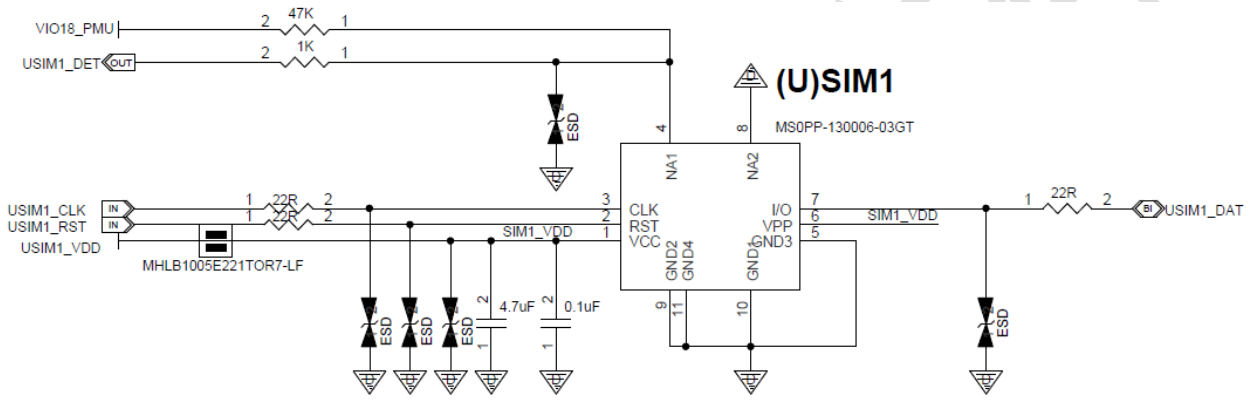
1.The TYPE-C interface is used with Dock for sharing

2. The DOCKis a fixed5Vcharging voltage

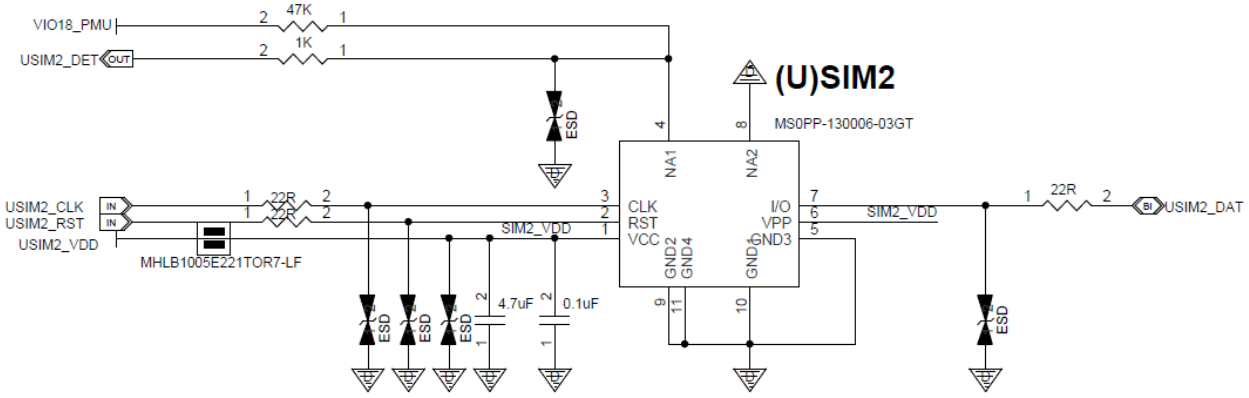
4.1.5 (U) SIMcard interface design

- The module supports dual SIM and dual standby, single pass
- (U)SIMThe card is powered internally by the module and automatically identifies the 1.8Vor2.95Vcard category
- Two sets of (U) SIMcard signals (including hotplug detection)cannot beused for otherfunctional purposes
- USIM_DET detects interrupts by default high level SIMcard insertion
- The SIM card holder is placed close to the module, try to ensure that the wiring length of the (U) SIM card signal line does not exceed200 mm, and the wiring in the S IMcard signal group isof equal length, and the error is ± 25mil

- The SIM card signal cable is routed away fromthe RF andVBAT power lines
- The layout of the SIM cardholder-related devices is placed close to the SIM card holder
- The CLK signal needs to be independentlywrapped to avoid crosstalk with the USIM_DATA signal, and the data groupwiring needs tobe protected by the land
- SIM卡SignalchooseTVSTube parasitic capacitance < 5 pF
- A 22 Ω resistor in series is required between the module and the SIM card to suppress spurious EMI and enhance ESD protection, and 2 2Ω resistors are placed close to the SIMcard holder end



(U) SIM1 design

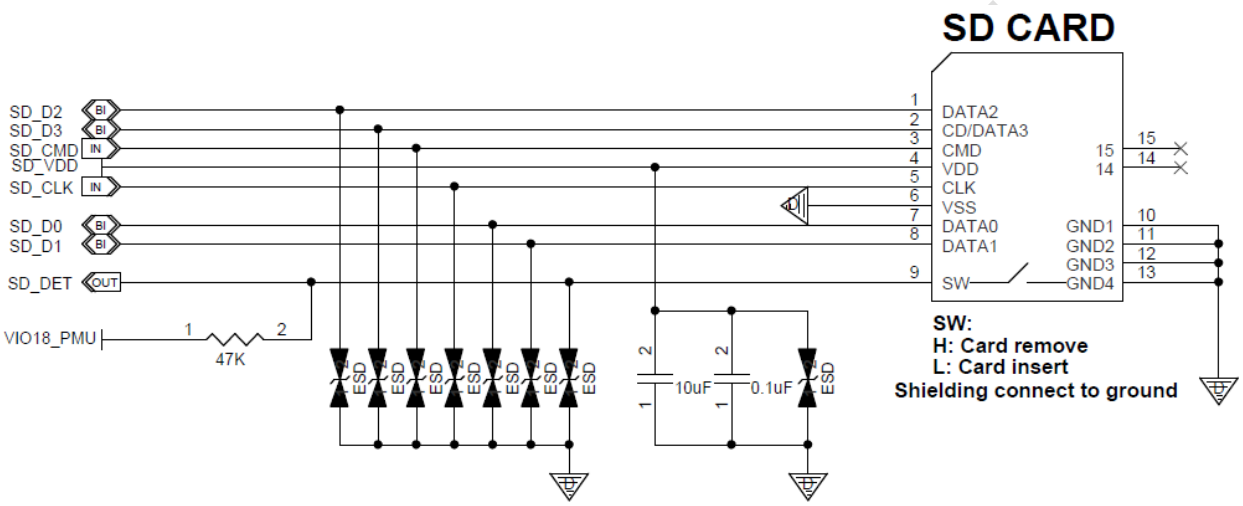


(U)SIM2Design

4.1.6 SD CADDINTERFACE DESIGN

- TheSDcard interface supports SDIO2.0/3.0protocol interface and supportsSD/SDHC/MS/MSPRO/MMC
- TheSDcard supports a maximumcapacity of 256GB
- The SD card is powered internally by the moduleat 3.0V

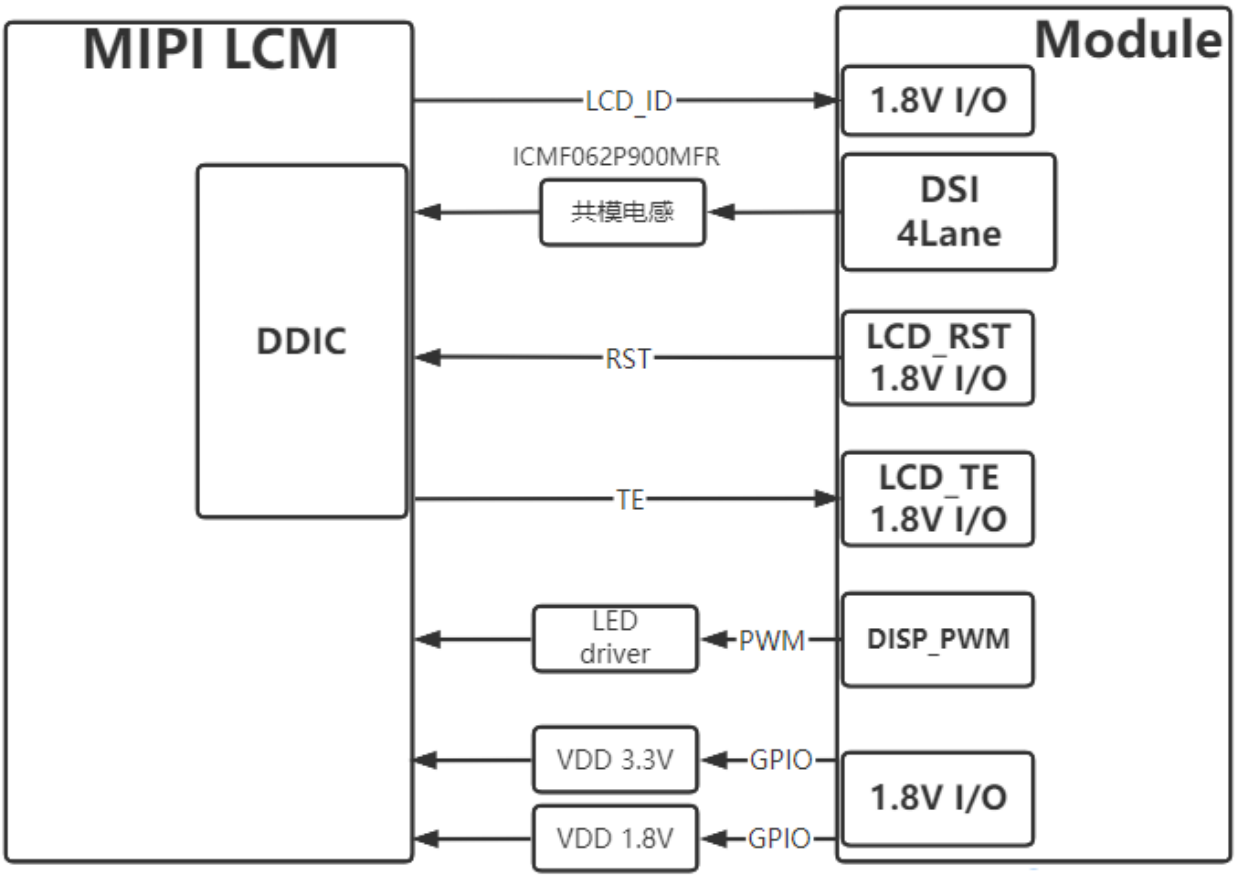
- The S D_DETsignal detection softwareis inserted into the SDcardat a low level by default
- SDThe card signal selects the TVS tube parasitic capacitance <5 pF
- The layout of the SIM card holder-related devices is placed close to the SIM card holder
- SD_CLK needs to be processed independently, and the SD card bus wiring refers to CLK to do the equal length in the group, and the error ± 25mil



SD card interface design

4.1.7 Main displayscreenDSIinterface design

- DSI 4lane MIPI high-speed signal
- 4lane MIPI high-speed signals add common-mode inductance
- The PCB layout of the motherboard requires a difference distribution line, a differential single group to do the package processing, 4 groups of differential need tohave a complete reference ground plane, and the differential impedance control is 100Ω±10%.
- The 4lane MIPI signal needs to be treated with an isometric error of < 6mil for a single group of P/N and a < of 25mil for the bus reference CLK isometric error
- When the MIPI signal is placed in the ESD device, the TVS parasitic capacitance < 1pF
- Total length of MIPI motherboard wiringDegree< 2000mil,

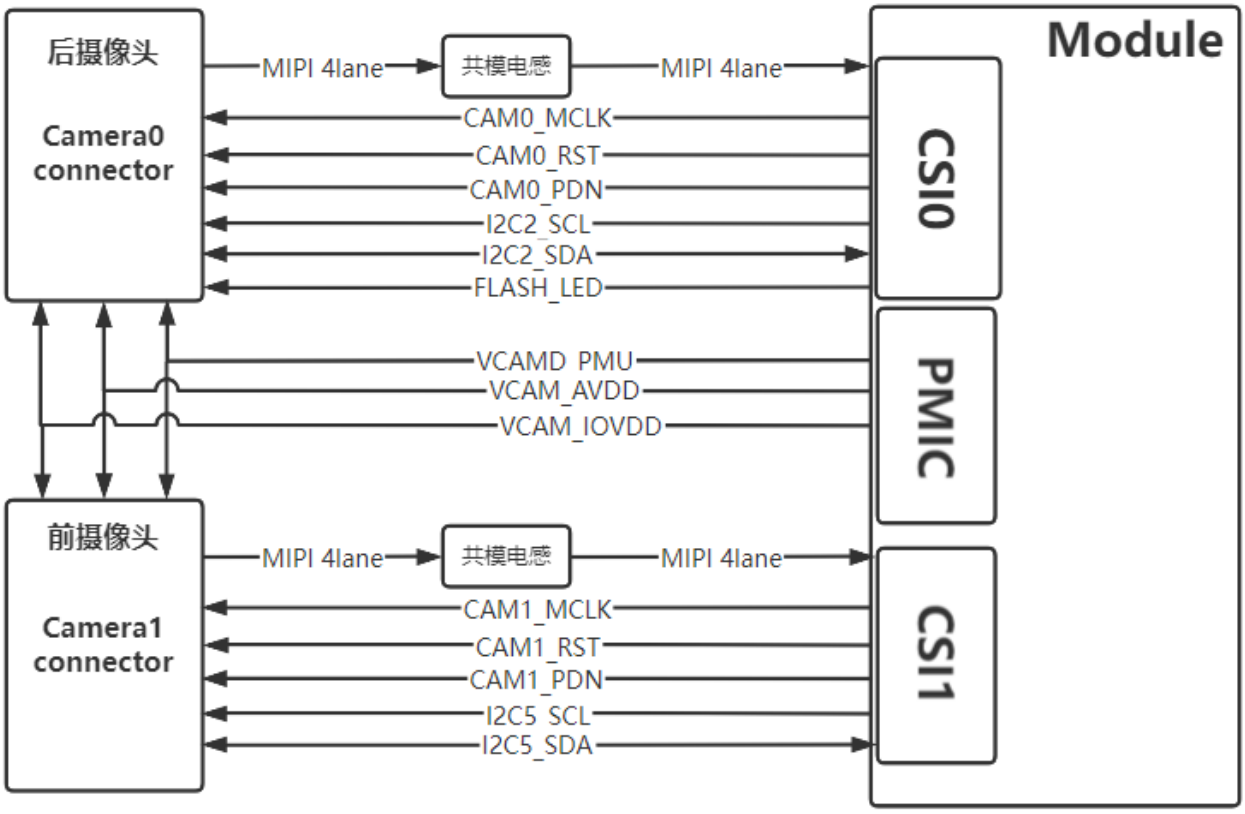


4.1.8 Camera interface design

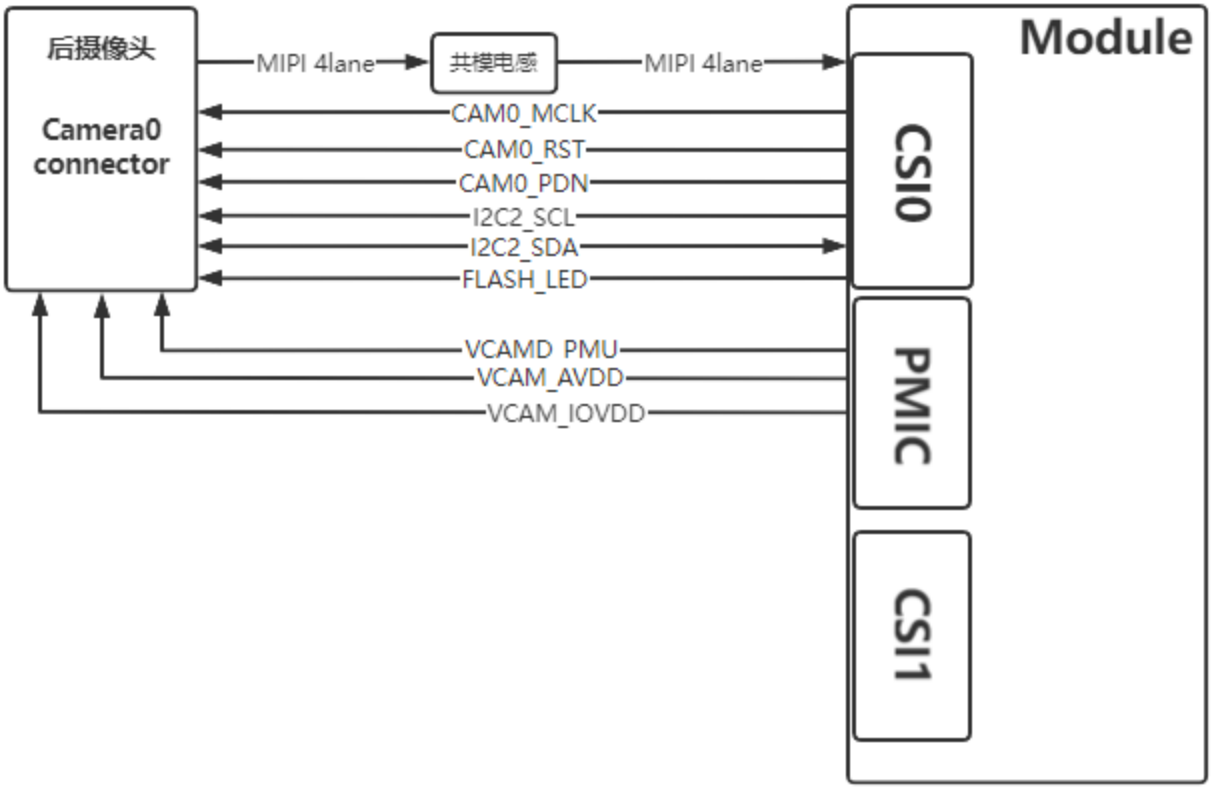
- Two sets of CSI-2protocol interfaces, 4lane MIPIhigh-speed signals
- 4lane MIPI high-speed signals add common-mode inductance
- The motherboard PCBwiringrequires a difference distribution line, a differential single group to do the ground package processing, 4 groupsof differential need tohave a complete referencegroundplane, and the differential impedance control is 100 Ω±10%
- 4lane MIPIThe signal needs to be processed at equal length,P/NSingle set of isometric errors < 6mil, bus reference CLKIsometric error < 25mil
- MIPISignal placement ESDWhen the device is used,TVSParasitic capacitance< 1pF
- MIPITotal length of motherboard cabling度 < 2000mil，
- The maximum driving current of the positive pole of FLASH_LEDflashis 700mA, and themotherboarddesigns a current-limiting resistoraccording to the requirements
- The VCAMD_PMU/ VCAM_AVDD/ VCAM_IOVDDpower supply is a special power supply for the camera and cannot be used for other purposes
- The camera power and control signals need to be increased by TVSelectrostatic tube,TVSParasitic capacitance< 5pF，VCAMD/VCAM_AVDD/VCAM_IOVDDThe power supply needs to add filter capacitors, and the related device layout is placed close to the

camera connector

- High-pixel cameras are connected to the CSI0channel by default
- In single-camera application scenarios, the C SI0 channel is preferred, and the CSI1channel is suspended



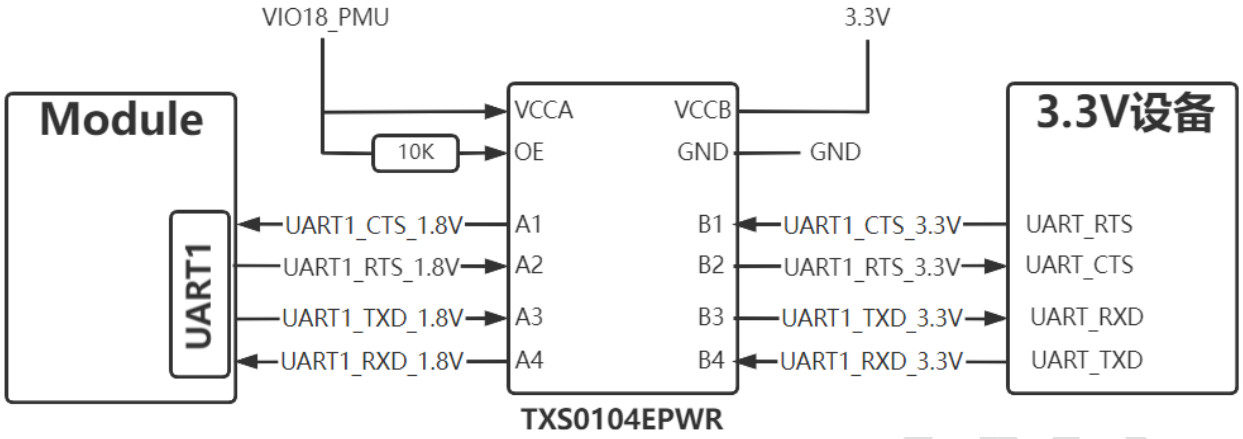
Front and rear **dual cameraswitching applications**



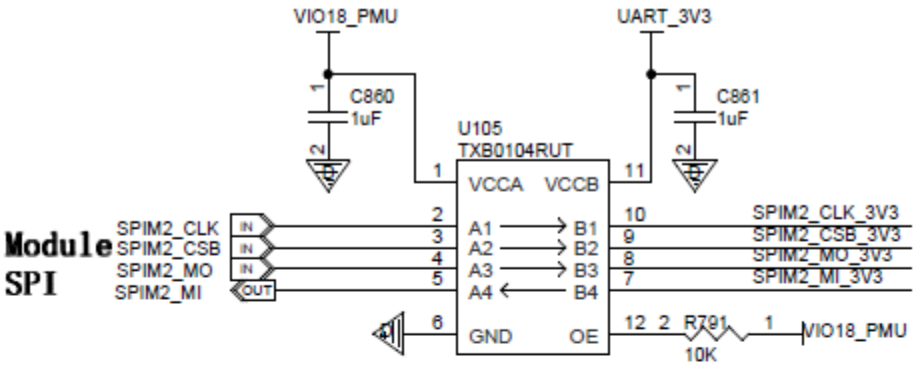
Single-camera app

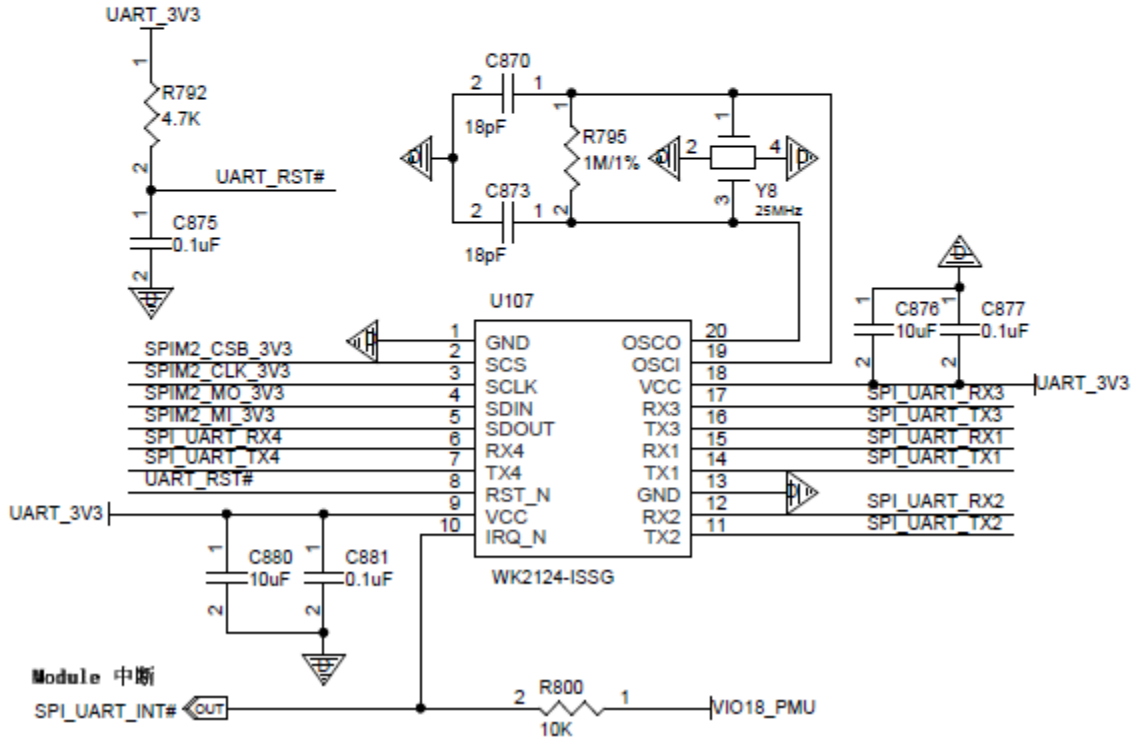
4.1.9 UARTserial port interface design

- The module supports 2 sets of UART(UART0/UART1),and the baud rate is 961200 by default
- UART0defaults to system debug use, modified software drivers can be used as functional serial ports, boot in the bootrom stage has debug log output, can not be used to encrypt I C and other important equipment, encryption ICand other important equipment use UART1 Communications
- The UART0signal cannot change the modulePin pin, fixing 93P in/94Pin
- The UART0/UART1interface level is 1.8V, and thelevel translation I C needs to be added for3.3Vdevice applications
- When the U ART serial port channel does not meet the requirements, please use the SPIinterface to convert and expand U ART, which can expand 4-way UART



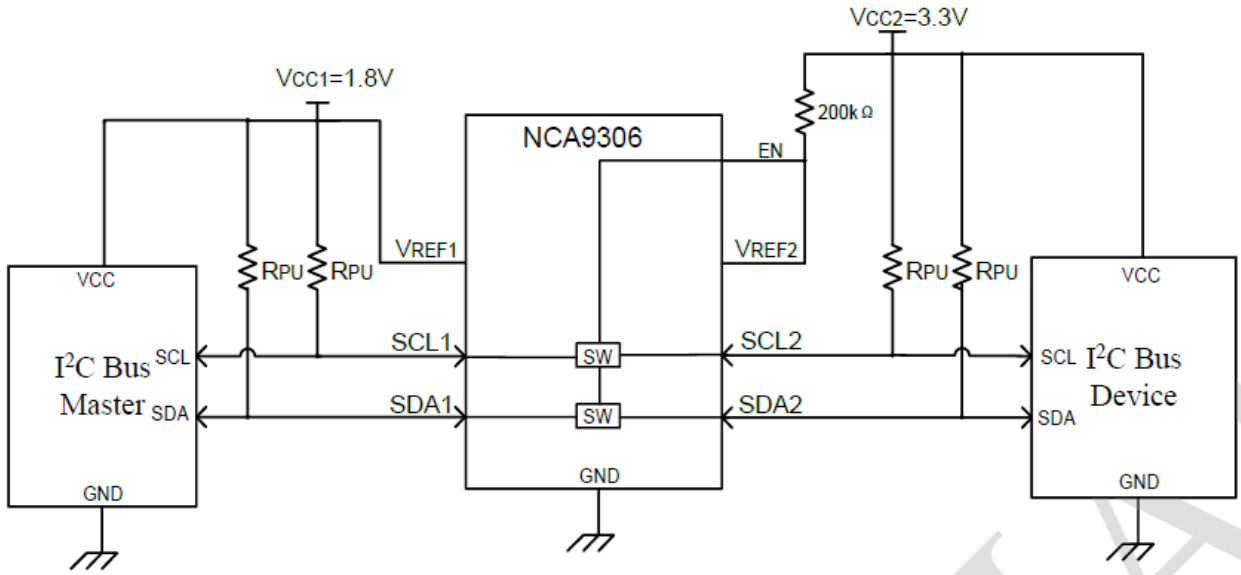
UARTlevel shifting applications

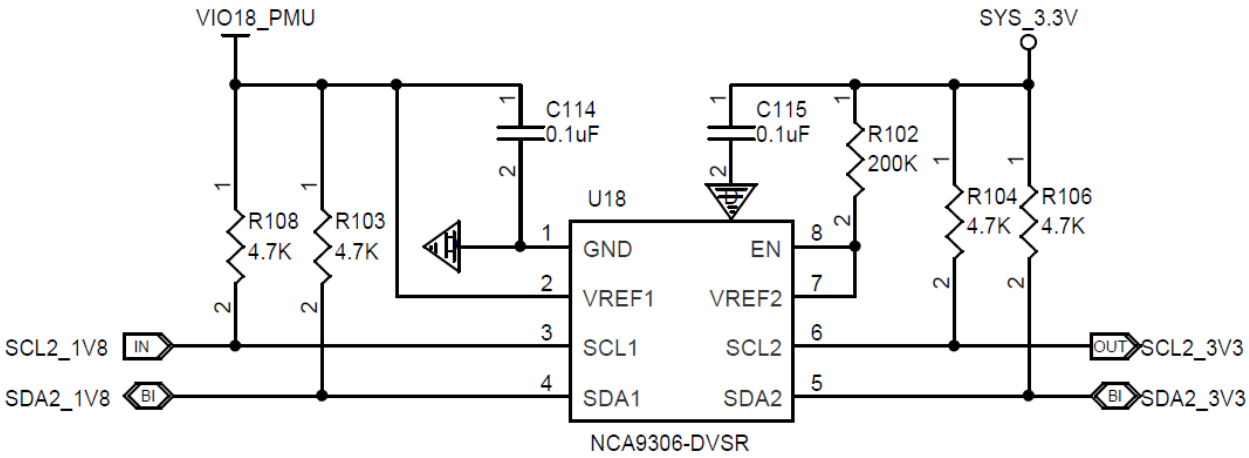




4.1.10 I2Cinterface design

- 5 groupsof I2C,support standard mode 100KHz and high speed mode400KHz
- I2C1/I2C2/I2C4/I2C5 channelSOCinternal hardware pulls up 5K Ω by default, andthe software can be changed to1K Ωpull-up
- There is no pull-up resistor inside the I2C6 channel SOC and the module, and the motherboard designmust haveanI2Cpull-up resistor
- TheI2Cinterface level is 1.8V, and the levelshifting I C needs to be added when3.3V devices are applied
- For level shifting I C and MOStube level shifting, you cannot use devices with internal pull-up resistors(such as SGM4553is similar to IC),please use N CA9306/PCA9306
- When designing the circuit, allI2Cchannels need to retain an external pull-up resistor design for flexible application in combination with software

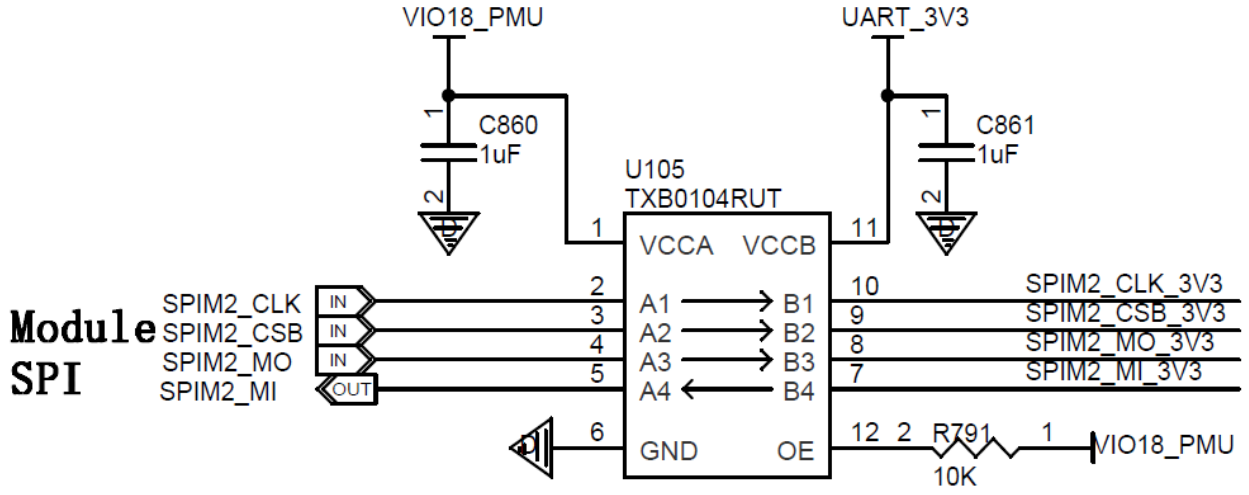




I2C level shifting applications

4.1.11 SPIinterface design

- Support 2 groups of independent working S PI interfaces and 3 groups of multiplexed(DPI/I2S)SPIinterfaces
- Operating frequency range 0.8K bit/s ~27M bit/s
- The SPI interface level is 1.8V, and the levelshift I C needs to be added for3.3V device applications
- When selecting level shifting IC, it is necessary to pay attention to the transmission rate required by Project SPI, and when the rate is lower than 15M, you can choose a chip with SGM4564category specifications with a rate higher than 1 5M (including 15M). For the above applications, please use theTXB0104RUTcategory specification chip SPIinterface level shifting cannot be used with SGM4553class specification chips

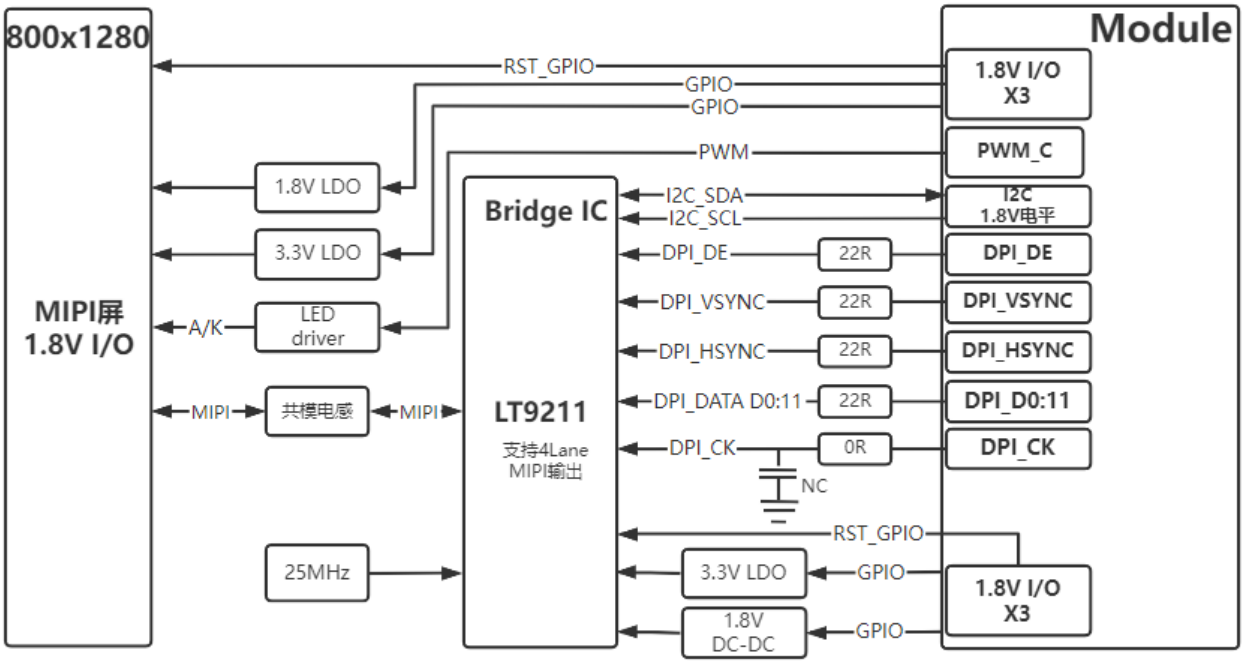


SPIlevel shifting applications

4.1.12 Sub-display DPIinterface design

4.1.12.1.1 Sub-MIPIdisplayoutput

- An 800x1280resolution displayis recommended for the DPI secondary screen
- DPI_CK signal motherboard PCB design independent stereoscopic package
- DPI_VSYNC/DPI_HSYNCsignal motherboard PCBdesign three-dimensional package
- DPI_DATA D0~11 data signal motherboard PCBdesign three-dimensional package
- DPI bus routing requiresa complete reference ground plane
- DPIbus motherboard PCBdesign reference DPI_CKsignal, do isometric processing, error ± 25mil
- DPIbusMotherboardPCBTotal routing length <

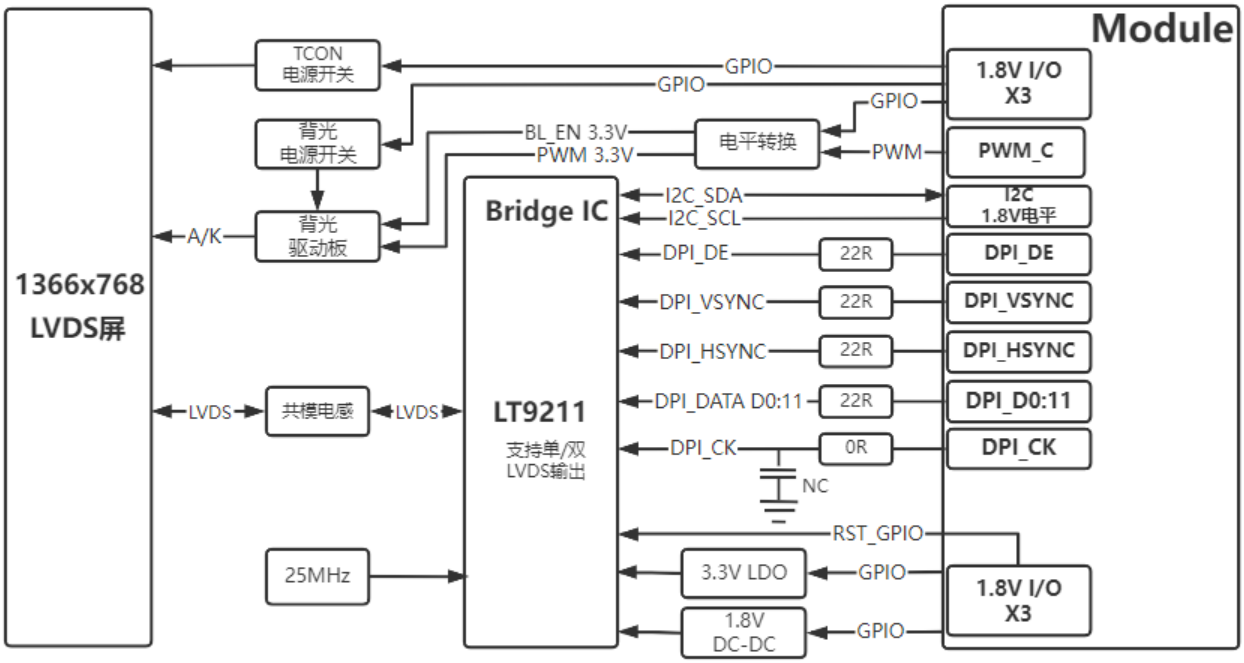


Sub-screen DPIto MIPIscreen application

4.1.12.1.2 Secondary LVDSdisplayoutput

- A 1366x768resolution display is recommended for the DPI secondary screen
- DPI_CK signal motherboard PCB design independent stereoscopic package
- DPI_VSYNC/DPI_HSYNC signal motherboard PCB design three-dimensional package
- DPI_DATA D0~11 data signal motherboard PCB design three-dimensional package
- DPI bus routing requiresa complete reference ground plane
-

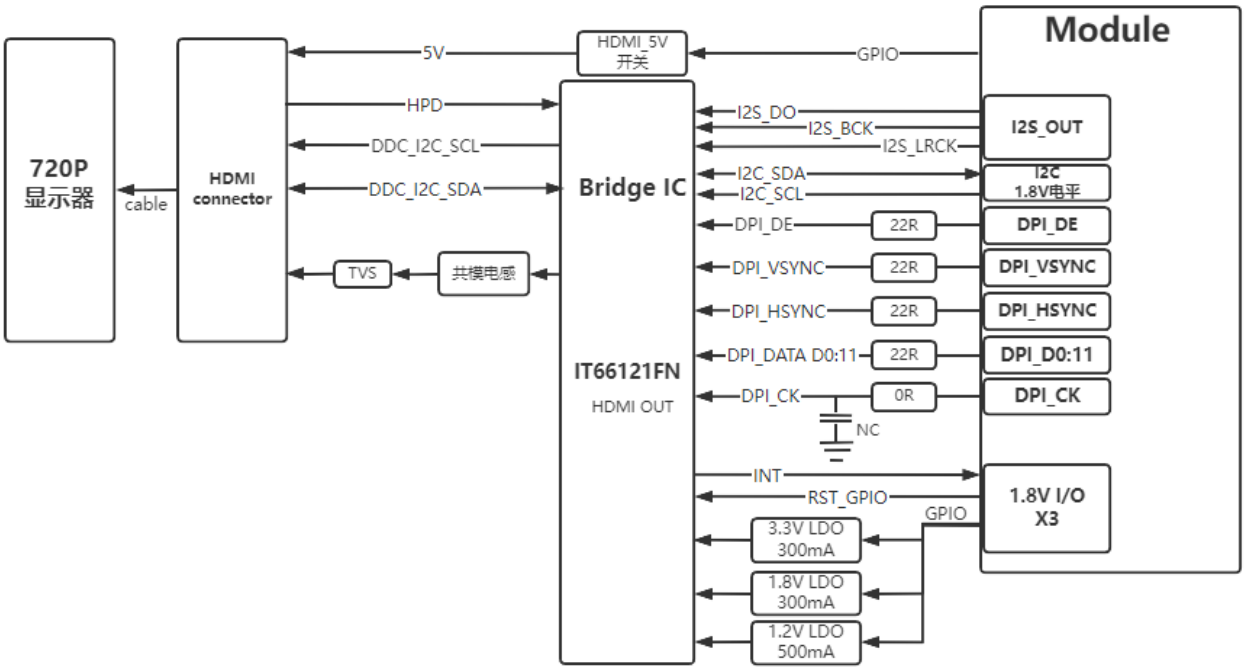
- DPI bus motherboard PCB design reference DPI_CK signal, do isometric processing, error ± 25mil
- DPI bus masterThe total length of the board PCB routing <



Sub-screen DPIto LVDSscreen application

4.1.12.1.3 Sub-HDMIdisplayoutput

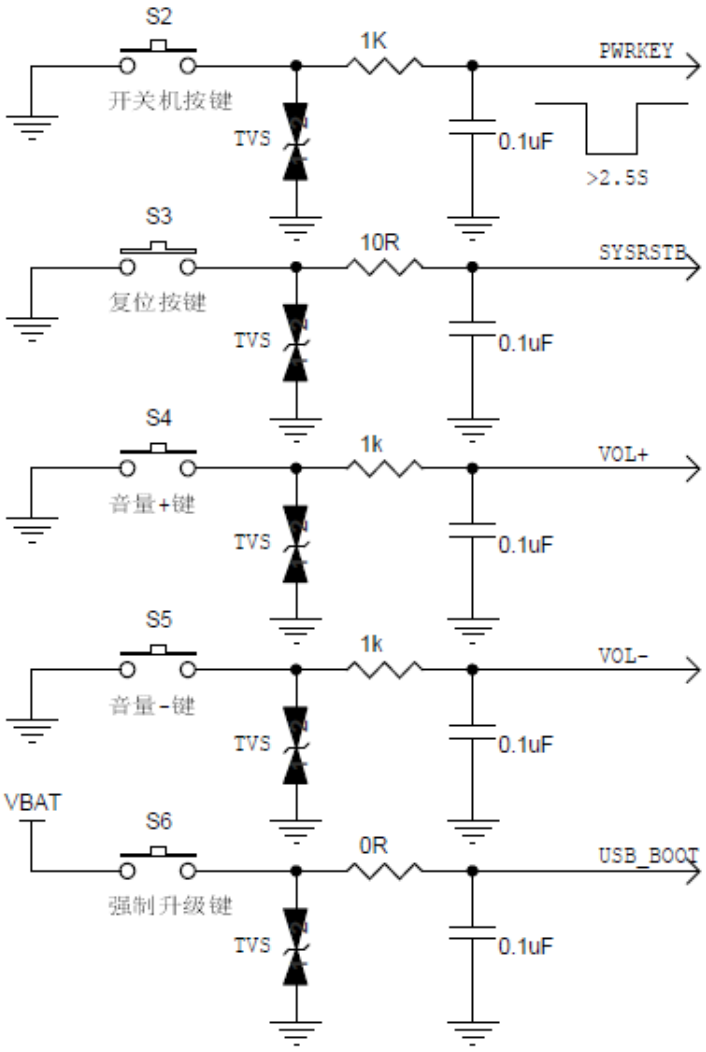
- The HDMI secondary screen is recommended to usea 720Presolution display
- DPI_CK signal motherboard PCB design independent stereoscopic package
- DPI_VSYNC/DPI_HSYNC signal motherboard PCB design three-dimensional package
- DPI_DATA D0~11 data signal motherboard PCB design three-dimensional package
- The DPIbuswiring requiresa complete reference ground plane
- DPI bus motherboard PCB design reference DPI_CK signal, do isometric processing, error ± 25mil
- DPI busThe total length of the motherboard PCB layout <



Sub-screen DPItoHDMIoutputapplication

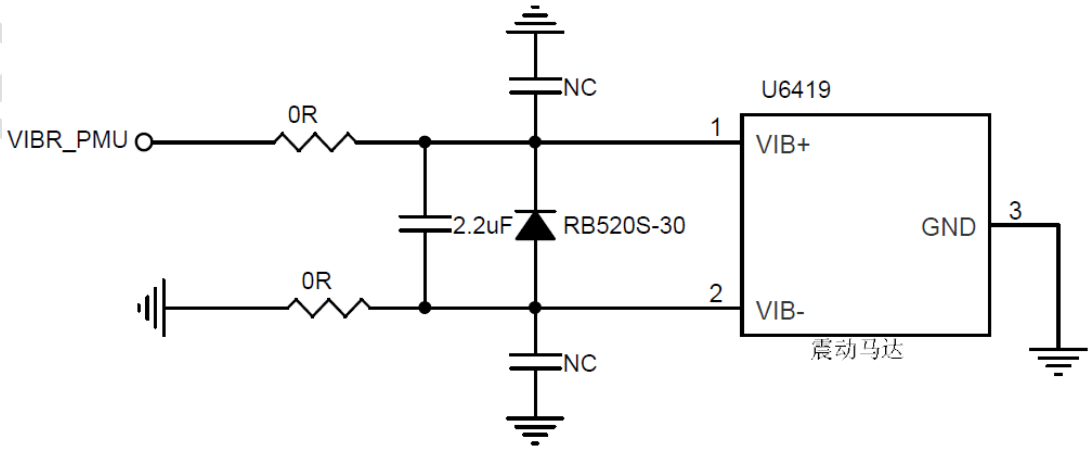
4.1.13 Key application design

- The button design needs to place TVSelectrostatic tube, PWRKEY/VOL+/VOL-/SYSRSTBsignal design RCto enhance EDSprotection
- USB_BOOT the control signal is the hardware forced upgrade state, press the forced upgrade button and then power on, SOCwill automatically enter the download burning mode
- The full-featured keyboard can be externally extended by using anI2Cor SPI interface



Module native function buttonapplication

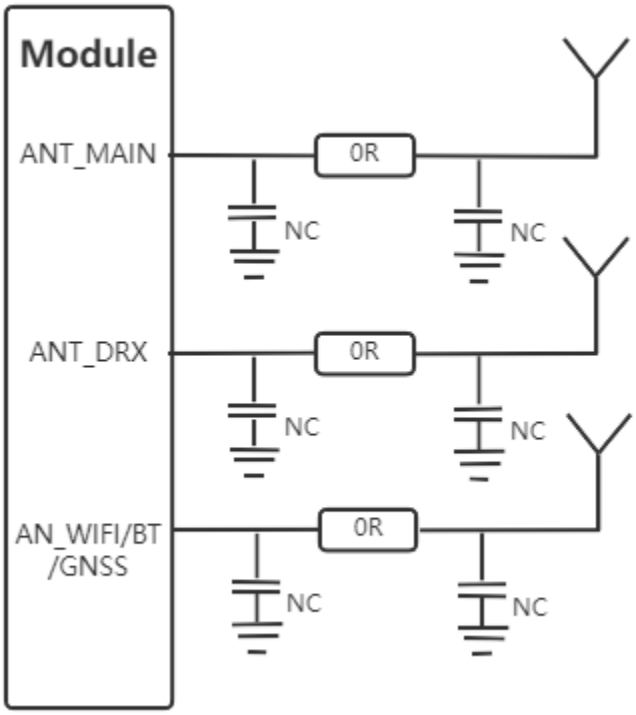
4.1.14 Vibrating motor design



Modulevibration motor application

4.1.15 Antenna port design

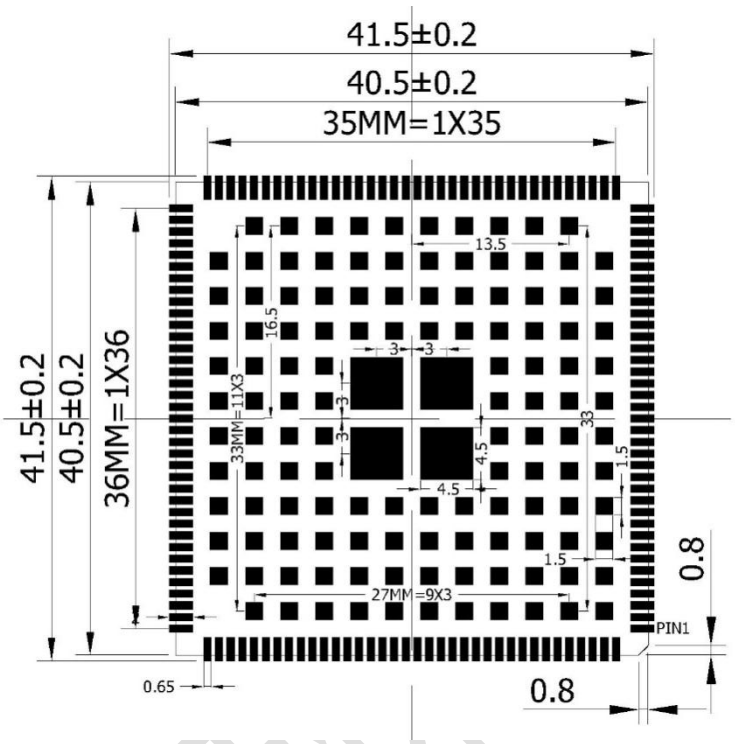
- ANT_MAIN Main Episode/ ANT_DRX Diversity andAN_WIFI/BT/GNSSThree-in-One Line The motherboard must do 50Ω impedance control
- The antenna wiring must have a complete reference G ND plane, and G ND vias must be added as much as possible around the signal line and reference ground to help improve RF performance, and the distance between the G NDvia and the signal line should be at least 2 times the linewidth (2W).
- The GND pad pin adjacent to the antenna pin does not make a thermal pad, and should be fully in contact with the ground toincrease the hole as much as possible
- The path loss from the antenna end to the Module antenna pad must be controlled within2dB, and theantennapathroutingPCBdesign cannot be punched through holes
- The motherboard must reserve a π-type matching circuit near the pin end of themodule antenna, and the default chip 0 ohm resistanceis straight-through
- Module only supports passive GPSantennas



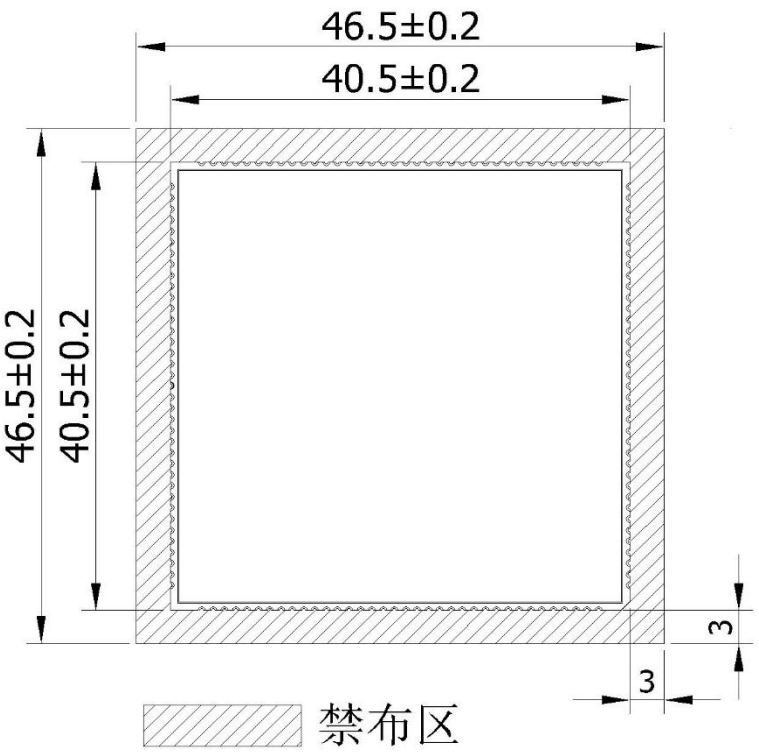
Moduleantennadesign

4.1.16 RF tuner switchwithSAR sensordesign

4.1.17 Recommended PCBpackage size



Recommended PCBpackage size (unit: mm).



Safe spacing (in mm).

5. Product packaging to be updated

The product adopts anti-static tray + desiccant + moisture sensitive card vacuum packaging

To be updated

6. producewith storage

6.1 Packaging and storage

For packaging and storage, please refer to the "Xinfa Core BoardZ600Z500Z400Intelligent ModuleSMTProcess Guide"

6.2 SMT patch

For SMT productionprocess parameters and related requirements, please refer to the "SMTProcess Guide for Core BoardZ400Intelligent Module"

7. List of mod AVLs (to be updated).

7.1 List of *camera* sensors

7.2 List of *camera* modules

7.3 Display a list of screen modules

7.4 List *of capacitive* touch sensors

8. Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

9. **Integration instructions for host product manufacturers according to KD B 996369 D03 OEM Manual v01**

8.1**List** of applicable FCC rules**.**

Part 15C,15E,22H,24E,27

8.2 Specific operational use conditions

Operating Frequency:part 2.3.1
Z400-H Is a universal GSM WCDMA LTE Wi-FiBTSmart module, with the industry's competitive package size and ultra-low energy consumption technology, designed for mobile devices and Internet of Things applications, Users can connect to the network through GSM, WCDMA, LTE WIFI, network communication, networking functions.
To maintain compliance with FCC RF exposure requirements, Please use the antenna provided with the product.

8.3 Limited Module Procedures. KDB 996369 D03, Section 2.4

not applicable .Please refer to the manual for usage scenarios Single Modular Approval Request

8.4Trace antenna designs. KDB 996369 D03, Section 2.5

not applicable .without trace antenna

8.5 RF exposure considerations.

RF exposure requirements are fulfilled for mobile configuration. This equipment should be installed and operated with minimum distance between 20cm the radiator your body
The installation of the module is restricted to mobile host devices
For portable applications OEM integrators need SAR evaluation and an own fCC ID.

8.6 Antennas.

The module comes with permanently attached External antennas. The spurious emission requirements are fulfilled (see attached test report).

8.7 Label and compliance information.

See Guidelines for Labeling and User Information for RF Devices –KDB Publication 784748.host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID 2A9FT-Z400-H3 ” with their finished product.

8.8 Information on test modes and additional testing requirements.

The test mode in the report is the module's maximum transmitting power emission for testing

Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

8.9 Additional testing, Part 15 Subpart B disclaimer

the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

FCC WARNING

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.

15.105 Information to the user.

(b) For a Class B digital device or peripheral, the instructions furnished the user shall include the following or similar statement, placed in a prominent location in the text of the manual:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

The availability of some specific channels and/or operational frequency bands are country dependent and are firmware programmed at the factory to match the intended destination.

The firmware setting is not accessible by the end user.

The final end product must be labelled in a visible area with the following:

“Contains Transmitter Module 2A9FT-Z400-H3”