Favalon

AN758-NA-H880 Module Hardware User Guide

Version: **1.0**

Date: **2024-07-19**

Favalon Auto Inc.

Applicability Model

No.	Product Model	Software Baseline	Applicable Customer	Description
1	AN758-NA-H880	-	-	Dual-core CPU, MCP: 8Gb+8Gb Supports European regional frequency bands, refer to Table 2-1 for frequency band information.

Change History

Version	Date	Author	Reviewed by	Approved by	Change Description
1.0	2024-07-19	Janwen QI	Billy Li, Jinlong Wang	Billy Li	Initial version.

Copyright Statement

Notice

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Contents

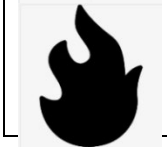
1 About This Document

1.1 Description

This document describes the electrical characteristics, RF performance, structural dimensions, and application environment information of the AN758-NA-H880 series modules. With the help of this document and other related documents, application developers can quickly understand the hardware functions of AN758-NA-H880 series modules and carry out hardware development of their products.

1.2 Safety Instruction

Please observe the following safety instructions to ensure personal safety and protect the product and work environment from potential damages. The product manufacturer should communicate the following safety instructions to end users and incorporate the safety instructions into the User Manuals of end products. Fibocom Auto Inc. will not take any responsibility for the consequences made by users who do not follow the safety rules or use the product improperly.

	Road safety first! When you are driving, do not use a handheld mobile terminal, even if it has a hands-free function. Stop the car before making a call.
	Please turn off the mobile terminal before boarding. It is prohibited to turn on the wireless function of the mobile terminal on the aircraft to prevent interference with the communication system of the aircraft. Failure to follow this prompt may affect flight safety or even violate the law.
	When you are in a hospital or health care facility, please be aware of restrictions on the use of mobile terminals. RF interference may cause abnormal operation of medical devices. Therefore, it may be required to turn off the mobile terminals.
	The mobile terminal does not guarantee a valid connection under any circumstances, for example, when the mobile terminal is in arrears or the (U)SIM is invalid. In case of emergency in above situations, remember to use the emergency call, and make sure your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal will receive and transmit RF signals when it is turned on. When it is close to TV, radio, computer or other electronic equipment, RF interference will be generated.
	Keep the mobile terminal away from flammable gases. Please turn off the mobile terminal when it is near gas stations, oil depots, chemical plants or explosive workplaces. There are potential safety hazards caused by the operation of electronic devices in any area with potential explosion hazards.

1.3 Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2A8RBAN758NA”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4)The max allowed antenna gain is 3.53dBi for external Dipole antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another

transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

2 Product Overview

2.1 Product Introduction

AN758-NA-H880 series module is a 5G automotive grade module designed based on MTK MT2735 platform, which can support 5G communication services under NSA and SA network architecture. AN758-NA-H880 integrates core devices such as Baseband, Memory, PMU, Transceiver, PA, etc., supporting 5G NR Sub6, FDD-LTE, TDD-LTE, WCDMA and GSM multi-standard long-distance communication modes, supports 3GPP release15, in addition to multi-frequency GNSS wireless positioning technology.

AN758-NA-H880 series modules are designed with LGA package and dual-core version of MTK MT2735M CPU, which is suitable for in-vehicle communication products.

2.2 Product Specifications

2.2.1 RF Characteristics

Table 2-1 shows the operating frequency bands of the AN758-NA-H880 series:

Table 2-1 Frequency bands supported by AN758-NA-H880 series modules

Model	AN758-NA-H880
5G NR	n1,n2,n3,n5,n7,n12,n14,n25,n28,n29,n38,n40,n41,n48,n66,n71,n77,n78
LTE FDD	B1,B2,B3,B4,B5,B7,B12,B13,B14,B17,B25,B26,B28,B29,B66,B71
LTE TDD	B38, B40, B41, B48
WCDMA	B1, B2, B4, B5
GSM	850,900,1800,1900MHz
GNSS	L1, L5

Table 2-2 and Table 2-3 for the transmission capabilities of the AN758-NA-H880 series:

Table 2-2 AN758-NA-H880 transmission capability

Model	AN758-NA-H880
NR Sub6 ENDC*	Maximum DL peak rate 2.75 Gbps Maximum UL peak rate 625 Mbps DL 4 x 4 MIMO LTE/NR
NR Sub6 SA*	Maximum DL peak rate 4.2 Gbps Maximum UL peak rate 525 Mbps DL 4 x 4 MIMO
LTE*	Maximum DL peak rate 1.6 Gbps Maximum UL peak rate 200 Mbps DL 4 x 4 MIMO
WCDMA	Maximum DL peak rate 42 Mbps (CAT24) Maximum UL peak rate 5.76 Mbps (CAT6)
GSM	GPRS: Maximum DL rate 107 Kbps, maximum UL rate 85.6 Kbps EDGE: Maximum DL rate 296 Kbps, maximum UL rate 236.8 Kbps

Note

1. The table shows the theoretical calculation results of the network standard data with "*".

Table 2-3 shows the modulation characteristics of the AN758-NA-H880 series:

Table 2-3 AN758-NA-H880 series modulation characteristics

Model	AN758-NA-H880
NR Sub6 ENDC	LTE modulation: Support DL 256 QAM, UL 256 QAM NR modulation: Support DL 256 QAM, UL 256 QAM
NR Sub6 SA	Support DL 256 QAM and UL 256 QAM Support RF bandwidth 5-100 MHz Support carrier interval: 15 KHz (FDD), 30 KHz (TDD)
LTE	Support 3GPP R15 Support 4DLCA maximally Support DL 256 QAM, UL 256 QAM Support bandwidth 1.4-20 MHz
WCDMA	Support 3GPP R9 DC-HSPA+ Support QPSK, 16-QAM and 64-QAM modulation
GSM	GPRS: Support GMSK EDGE: Support 8-PSK

2.2.2 Key Features

Table 2-4 Key features

Performance	Description
Power supply	DC: 3.4–4.2 V, typical voltage: 3.8 V
Processor	MediaTek MT2735, 7 nm, ARM Cortex-A55, up to 1.5 GHz
MCP	8 Gb LPDDR4X + 8 Gb Nand Flash
OS	Linux
Power class	Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2.7dB) for LTE-FDD bands Class 3 (23dBm±2.7dB) for LTE-TDD bands Class 3 (23dBm+2/-3dB) for NR Sub6 bands except N41/N77/N78 Class 2 (26dBm+2/-3dB) for N41/N77/78 bands
GNSS characteristics	Support GNSS L1 + L5 GPS/GLONASS/BeiDou/Galileo/QZSS
SMS	MO/MT SMS
Audio interface	2 sets of audio interfaces, 1 set of I²S interfaces, 1 set of PCM interfaces
USB interface	1 USB port, support USB2.0, data transfer rate of up to 480 Mbps; support USB3.0, data transfer rate of up to 5Gbps
PCIe interface	1 set of PCIe Gen 3 x2 Lanes
SIM interface	2 SIM card interfaces Support USIM/ESIM: 1.8 V and 3 V
SPI interface	3 SPI interfaces with up to 52 MHz clock frequency, one of which supports slave mode
I²C interface	2 I²C interfaces, high speed up to 3.4 Mbps (High speed)
UART interface	4 UART interfaces, including one debug UART

Performance	Description
RGMII interface	Support 10/100/1000 M
SGMII interface	Support 10/100/1000/2500 M
External flash interface	Support 4 bit SD card and 8 bit EMMC flash
ADC interface	5 sets of ADC interface
GPIOs	13 general-purpose GPIO ports, refer to "AN758-NA-H880_Pin Description_V1.0" for GPIO interface description.
Physical characteristics	Dimensions: 48 mm x 48 mm x 3.3mm Package: LGA
Temperature range	Operating temperature: -40°C to 85°C[1] Extended temperature: -40°C to 95°C[2] Storage temperature: -40°C to 105°C
Software update	Support FOTA update
RoHS	RoHS compliant, halogen free

Warning

1. Note 1: When the module operates in this temperature range, the functions of the module are normal.
2. Note 2: When the module operates in this temperature range, the relevant performance of the module may be reduced; when the temperature returns to the normal operating range, the module performance will return to normal again.

2.3 LTE CA Combinations

2.3.1 CA Combinations Supported by AN758-NA-H880

LTE DL 2CA					
CA_2C	CA_5B	CA_41C	CA_48C	CA_66C	CA_12A-66A
CA_25A-25A	CA_2A-2A	CA_2A-4A	CA_2A-5A	CA_2A-12A	CA_2A-13A
CA_2A-14A	CA_2A-48A	CA_2A-66A	CA_2A-71A	CA_4A-12A	CA_4A-29A
CA_4A-4A	CA_4A-5A	CA_4A-71A	CA_5A-66A	CA_7A-7A	CA_7A-12A
CA_66A-66A	CA_66A-71A	CA_48A-66A	--	--	--
LTE DL 3CA					
CA_41D	CA_48D	CA_2A-12A-66A	CA_2A-2A-12A	CA_2A-48C	CA_2A-66C
CA_2A-2A-4A	CA_2A-2A-5A	CA_2A-2A-14A	CA_2A-2A-66A	CA_2A-4A-12A	CA_2A-2A-13A
CA_2A-2A-71A	CA_2A-4A-71A	CA_2A-4A-4A	CA_2A-4A-5A	CA_2A-48A-66A	CA_2A-5A-66A
CA_2A-66A-66A	CA_2A-66A-71A	CA_5A-66A-66A	CA_12A-66A-66A	CA_4A-4A-71A	CA_66A-66A-71A
CA_48C-66A	CA_66A-66C	CA_4A-4A-12A	CA_4A-4A-5A	--	--
LTE DL 4CA					
CA_48E	CA_48D-66A	CA_2A-12A-66A-66A	CA_2A-2A-12A-66A	CA_2A-2A-5A-66A	CA_2A-2A-4A-12A

CA_2A-2A-4A-4A	CA_2A-2A-4A-5A	CA_2A-2A-4A-71A	CA_2A-2A-66A-66A	CA_2A-66A-66A-71A	CA_2A-5A-66A-66A
CA_2A-2A-66A-71A	--	--	--	--	--
LTE UL 2CA					
CA_48C	CA_66C	--	--	--	--
NR DL 2CA					
CA_n12A-n66A	CA_n12A-n77A	CA_n25A-n25A	CA_n25A-n66A	CA_n25A-n71A	CA_n25A-n77A
CA_n25A-n78A	CA_n2A-n12A	CA_n2A-n2A	CA_n2A-n5A	CA_n2A-n66A	CA_n2A-n77A
CA_n2A-n78A	CA_n41A-n41A	CA_n41A-n71A	CA_n41A-n77A	CA_n48A-n48A	CA_n48A-n66A
CA_n48C	CA_n5A-n66A	CA_n5A-n77A	CA_n5A-n78A	CA_n5B	CA_n66a-n66A
CA_n66A-n71A	CA_n66A-n77A	CA_n66A-n78A	CA_n71A-n77A	CA_n71B	CA_n77A-n77A

2.4 EN-DC Combinations

2.4.1 EN-DC Combinations Supported by AN758-NA-H880

5G-NR	组合类型	EN-DC 组合	4G 下行 4*4 MIMO	5G-NR 下行 4*4 MIMO	4G 上行	5G-NR 上行
TDD	1DL + FR1	DC_71A_n78A	--	n78A	71A	n78A
TDD	1DL + FR1	DC_4A_n78A	--	n78A	4A	n78A
TDD	1DL + FR1	DC_5A_n77A	--	n77A	5A	n77A
TDD	1DL + FR1	DC_5A_n78A	--	n78A	5A	n78A
TDD	1DL + FR1	DC_66A_n77A	--	n77A	66A	n77A
TDD	1DL + FR1	DC_7A_n77A	7A	n77A	7A	n77A
TDD	1DL + FR1	DC_7A_n78A	7A	n78A	7A	n78A
TDD	1DL + FR1	DC_14A_n77A	--	n77A	14A	n77A
TDD	1DL + FR1	DC_13A_n77A	--	n77A	13A	n77A
TDD	1DL + FR1	DC_2A_n78A	2A	n78A	2A	n78A
TDD	1DL + FR1	DC_12A_n78A	--	n78A	12A	n78A
TDD	1DL + FR1	DC_2A_n77A	2A	n77A	2A	n77A
TDD	1DL + FR1	DC_12A_n77A	--	n77A	12A	n77A
TDD	1DL + FR1	DC_25A_n77A	--	n77A	25A	n77A
TDD	1DL + FR1	DC_26A_n77A	--	n77A	26A	n77A

5G-NR	组合类型	EN-DC 组合	4G 下行 4*4 MIMO	5G-NR 下行 4*4 MIMO	4G 上行	5G-NR 上行
TDD	2DL + FR1	DC_2A-2A_n77A	2A	n77A	2A	n77A
TDD	2DL + FR1	DC_2A-12A_n77A	2A	n77A	2A,12A	n77A
TDD	2DL + FR1	DC_25A-25A_n77A	--	n77A	25A	n77A
TDD	2DL + FR1	DC_2A-2A_n78A	2A	n78A	2A	n78A
TDD	2DL + FR1	DC_2A-12A_n78	2A	n78A	2A,12A	n78A
TDD	2DL + FR1	DC_2A-13A_n77A	2A	n77A	2A,13A	n77A
TDD	2DL + FR1	DC_2A-14A_n77A	2A	n77A	2A,14A	n77A
TDD	2DL + FR1	DC_2A-71A_n78A	2A	n78A	2A,71A	n78A
TDD	2DL + FR1	DC_2A-5A_n77A	2A	n77A	2A,5A	n77A
TDD	2DL + FR1	DC_2A-5A_n78A	2A	n78A	2A,5A	n78A
TDD	2DL + FR1	DC_5A-66A_n77A	--	n77A	5A,66A	n77A
TDD	2DL + FR1	DC_66A-66A_n77A	--	n77A	66A	n77A
TDD	2DL + FR1	DC_7A-12A_n78A	7A	n78A	7A,12A	n78A
TDD	2DL + FR1	DC_7A-7A_n77A	7A	n77A	7A	n77A
TDD	3DL + FR1	DC_2A-2A-12A_n77A	2A	n77A	2A,12A	n77A
TDD	3DL + FR1	DC_2A-2A-12A_n78A	2A	n78A	2A,12A	n78A
TDD	3DL + FR1	DC_2A-2A-13A_n77A	2A	n77A	2A,13A	n77A
TDD	3DL + FR1	DC_2A-2A-14A_n77A	2A	n77A	2A,14A	n77A
TDD	3DL + FR1	DC_2A-2A-5A_n77A	2A	n77A	2A,5A	n77A
TDD	3DL + FR1	DC_2A-2A-71A_n78A	2A	n78A	2A,71A	n78A

Warning

1. The 4G bands not listed in the 4G DL 4 x 4 MIMO list do not support DL 4 x 4 MIMO, but DL 2 x 2 MIMO is supported by default.
2. "4G uplink": For example, in DC_2A-12A_n77A, the 4G uplink is 2A/12A, and 2A and 12A are or relationships, and only one band is the uplink.

2.5 Hardware Block Diagram

The following hardware block diagram shows the main hardware features of the AN758-NA-H880 series modules, including the following:

- Baseband
- RF transceiver section
- PMU
- MCP
- External interfaces

3 Application Interfaces

3.1 LGA Interface

The AN758-NA-H880 series modules use LGA interfaces with a total of 357 pins, which are distributed as shown below.

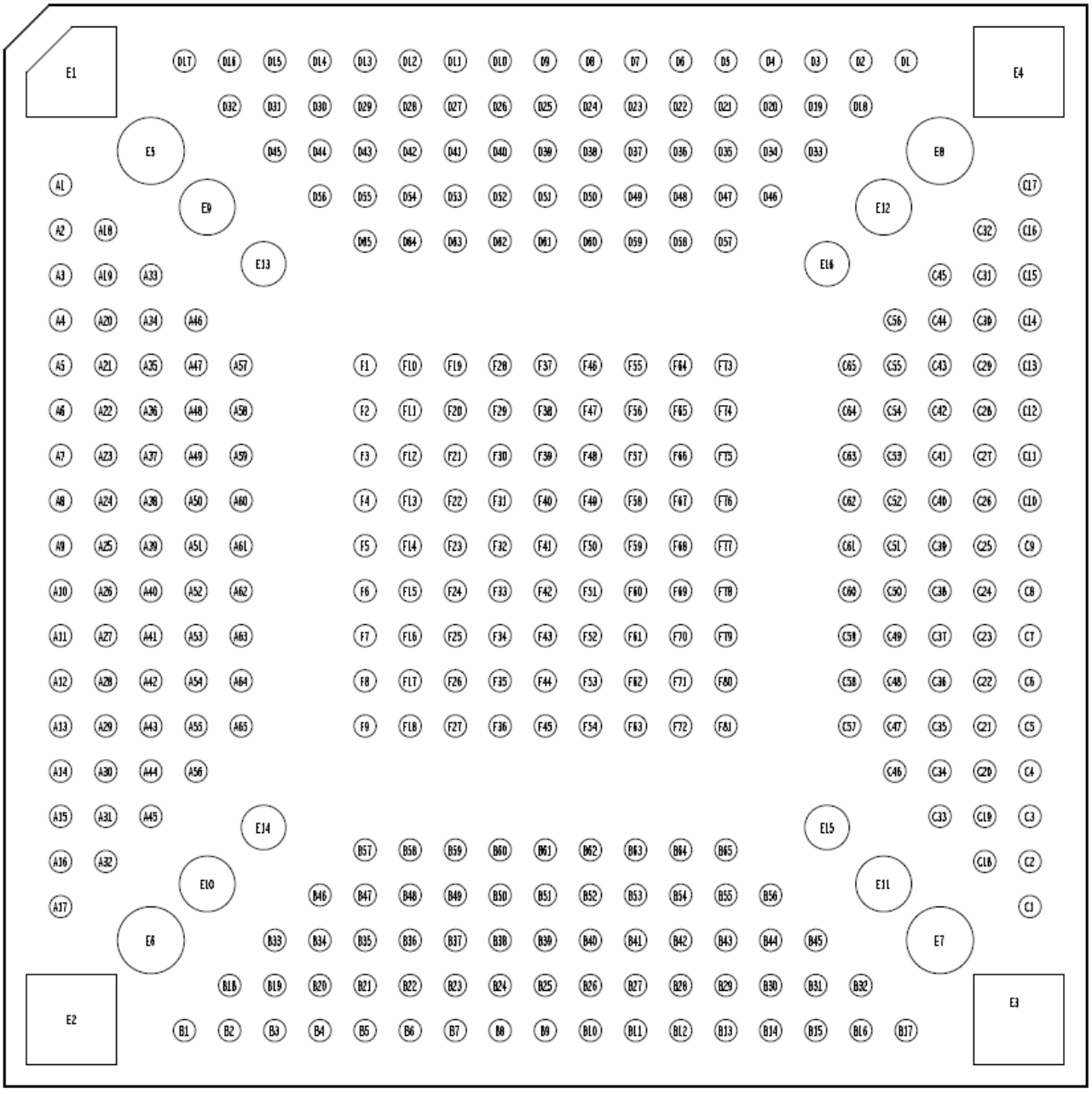


Figure 3-1 Pin Distribution Diagram

The pin definitions are shown in the following table:

Table 3-1 I/O parameter definitions

Type	Description
IO	Input/Output
DIO	Digital Input/Output

Type	Description
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AIO	Analog Input/Output
AI	Analog Input
AO	Analog Output
OD	Open Drain
PD	Pull Down
PU	Pull Up
Hi-Z	High Resistance

The pin functions and electrical characteristics of the AN758-NA-H880 series modules are described in the following table:

Table 3-2 Pin Descriptions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
ANT								
C14	ANT-GNSS	GNSS L1+L5 Antenna Interface	-	-	AIO	-	-	50Ω impedance requirement
C17	ANT1	GSM main set transmit and receive. WCDMA main set transmit and receive. 4G B1,B2,B3,B4,B5,B7,B12,B13,B14,B17,B25,B26,B28,B66,B71,B38,B40,B41main set transmit and receive. 4G B29 main set receive. 4G B48 main set transmit and receive. 5G N1,N2,N3,N5,N7,N12,N14,N25,N28,N38,N40,N41,N66,N71main set transmit and receive. 5G N29 main set receive. 5G N48,N77,N78 main set transmit and receive.	-	-	AIO	-	-	50Ω impedance requirement
D2	ANT2	GSM diversity reception. WCDMA diversity reception. 4G B1,B2,B3,B4,B5,B7,B12,B13,B14,B17,B25,B26,B28	-	-	AIO	-	-	50Ω impedance requirement

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
		,B66,B71,B38,B40,B41diversity reception. 4G B29 diversity reception 4G B48 main set reception MIMO. 5G N1,N2,N3,N5,N7,N12,N14,N25,N28,N38,N40,N41,N66,N71diversity reception. 5G N29 diversity reception 5G N48,N77,N78 main set receive MIMO.						
D14	ANT3	4G B1/3/7/38/40/41 main set reception MIMO. 4G B48 diversity receive. 5G N1/3/7/38/41/66 main set receive MIMO. 5G N48,N77/78 Diversity Reception.	-	-	AIO	-	-	50Ω impedance requirement
D17	ANT4	4G B1/2/3/7/38/40/41 diversity receive MIMO. 4G B48 diversity receive MIMO. 5G N1/2/3/7/38/41/66 diversity receive MIMO. 5G n48,N77/78 diversity receive MIMO.	-	-	AIO	-	-	50Ω impedance requirement
D8	Reserve_D8	Reserved	-	-	-	-	-	Suspension Handling
D11	Reserve_D11	Reserved	-	-	-	-	-	Suspension Handling
D5	Reserve_D5	Reserved	-	-	-	-	-	Suspension Handling
A1	Reserve_A1	Reserved	-	-	-	-	-	Suspension Handling
A4	Reserve_A4	Reserved	-	-	-	-	-	Suspension Handling
Power								
A7	VPH_IN_A7	Module power input	-	-	PI	3.8V	-	Peak current 3.8V/3A (25°C)
A8	VPH_IN_A8	Module power input	-	-	PI	3.8V	-	
A23	VPH_IN_A23	Module power input	-	-	PI	3.8V	-	
A24	VPH_IN_A24	Module power input	-	-	PI	3.8V	-	
A51	EMMC_VCC_OUT1	EMMC VCC power output	-	-	PO	3.0V	-	800mA
A50	EMMC_VCC_OUT2	EMMC VCC power output	-	-	PO	3.0V	-	

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
A25	EMMC_VCCQ_OUT	EMMC VCCQ power output	-	-	PO	1.8V	-	200mA
A9	VIO_1V8_OUT	1.8V interface power output	-	-	PO	1.8V	-	100mA
A37	Reserve_A37	Reserved	-	-	-	-	-	-
A38	Reserve_A38	Reserved	-	-	-	-	-	-
A39	Reserve_A39	Reserved	-	-	-	-	-	-
RGMII								
A43	RGMII_LDO1_EN	RGMII 1.8V power enable signal	Y	PD	DIO	1.8V	-	Configurable as GPIO
A42	RGMII_LDO2_EN	RGMII 3.3V power enable signal	Y	PD	DIO	1.8V	-	Configurable as GPIO
A17	RGMII_RESET_N	RGMII reset signal	Y	PD	DO	1.8V	-	-
A41	RGMII_INT_N	RGMII interrupt signal	Y	PD	DI	1.8V	-	-
A45	RGMII_MDIO	RGMII management data communication signal	Y	PD	DIO	1.8V	-	-
A44	RGMII_MDC	RGMII management data signal clock	Y	PD	DO	1.8V	-	-
A11	RGMII_CTL_TX	RGMII transmit control signal	Y	PD	DO	1.8V	-	-
A12	RGMII_CK_TX	RGMII transmit signal clock	Y	PD	DO	1.8V	-	-
A13	RGMII_TX_0	RGMII transmit data bit 0	Y	PD	DO	1.8V	-	-
A14	RGMII_TX_1	RGMII transmit data bit 1	Y	PD	DO	1.8V	-	-
A15	RGMII_TX_2	RGMII transmit data bit 2	Y	PD	DO	1.8V	-	-
A16	RGMII_TX_3	RGMII transmit data bit 3	Y	PD	DO	1.8V	-	-
A27	RGMII_CTL_RX	RGMII receive control signal	Y	PD	DI	1.8V	-	-
A28	RGMII_CK_RX	RGMII receive signal clock	Y	PD	DI	1.8V	-	-
A29	RGMII_RX_0	RGMII receive data bit 0	Y	PD	DI	1.8V	-	-
A30	RGMII_RX_1	RGMII receive data bit 1	Y	PD	DI	1.8V	-	-
A31	RGMII_RX_2	RGMII receive data bit 2	Y	PD	DI	1.8V	-	-
A32	RGMII_RX_3	RGMII receive data bit 3	Y	PD	DI	1.8V	-	-
SIM								
A6	VDD_UIM1	UIM1 card power supply	-	-	PO	1.8V/ 3.0V	-	-
A22	UIM1_RST	UIM1 card reset signal	-	PD	DO	1.8V/ 3.0V	-	-
A36	UIM1_DATA	UIM1 card data signal	-	PD	DIO	1.8V/ 3.0V	-	-
A48	UIM1_CLK	UIM1 card clock signal	-	PD	DO	1.8V/ 3.0V	-	-
A49	UIM1_DET	UIM1 card insertion detection signal	-	PD	DI	1.8V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
A35	VDD_UIM2	UIM2 card power supply	-	-	PO	1.8V/ 3.0V	-	-
A34	UIM2_RST	UIM2 card reset signal	-	PD	DO	1.8V/ 3.0V	-	-
A46	UIM2_DATA	UIM2 card data signal	-	PD	DIO	1.8V/ 3.0V	-	-
A47	UIM2_CLK	UIM2 card clock signal	-	PD	DO	1.8V/ 3.0V	-	-
A33	UIM2_DET	UIM2 card insertion detection signal	-	PD	DI	1.8V	-	-
PCIe								
B35	PCIE_CLKREQ	PCIe clock request signal	Y	PU	DI	1.8V	-	-
B7	PCIE_WAKE_N	PCIe wake-up signal	Y	PU	DI	1.8V	-	-
B6	PCIE_RESET	PCIe reset signal	Y	PU	DO	1.8V	-	-
B3	PCIE_CLK_P	PCIe differential clock signal +	-	-	AIO	1.2V	-	1. 100±10% impedance control. 2. 50Ω±1% (external pull-down resistor)
B20	PCIE_CLK_M	PCIe differential clock signal -	-	-	AIO	1.2V	-	
B4	PCIE_TX0_P	PCIe differential transmit signal 0 +	-	-	AO	1.2V	-	85±10% impedance control.
B21	PCIE_TX0_M	PCIe differential transmit signal 0 -	-	-	AO	1.2V	-	
B5	PCIE_TX1_P	PCIe differential transmit signal 1 +	-	-	AO	1.2V	-	
B22	PCIE_TX1_M	PCIe differential transmit signal 1 -	-	-	AO	1.2V	-	
B2	PCIE_RX0_P	PCIe differential receive signal 0 +	-	-	AI	1.2V	-	1. 85±10% impedance control. 2. If not used, grounding treatment.
B19	PCIE_RX0_M	PCIe differential receive signal 0 -	-	-	AI	1.2V	-	
B1	PCIE_RX1_P	PCIe differential receive signal 1 +	-	-	AI	1.2V	-	
B18	PCIE_RX1_M	PCIe differential receive signal 1 -	-	-	AI	1.2V	-	
WIFI6								
B49	WLAN_ACT	WLAN using request signal	-	PD	DIO	1.8V	-	Cannot be used as GPIO.
B47	BT_ACT_TXD	BT use request signal	-	PD	DO	1.8V	-	
B48	BT_PRI_RXD	BT priority use signal	-	PD	DO	1.8V	-	
B24	RF_COEX_UART_TX	PTA transmit signal	-	PD	DO	1.8V	-	
B23	RF_COEX_UART_RX	PTA receive signal	-	PD	DI	1.8V	-	
B46	BT_EN	Bluetooth enable signal	Y	PD	DIO	1.8V	-	-
B8	WLAN_EN	WIFI module enable signal	Y	PD	DIO	1.8V	-	-
B36	HOST_WAKE_BT	5G NAD wakeup BT	Y	PD	DIO	1.8V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
B37	BT_UART_RX	Bluetooth UART receive signal	-	PD	DI	1.8V	GPIO180	-
B38	BT_UART_TX	Bluetooth UART transmit signal	-	PD	DO	1.8V	GPIO179	-
B40	BT_UART_RTS_N	Bluetooth UART transmit request signal	-	PD	DO	1.8V	GPIO178	-
B39	BT_UART_CTS_N	Bluetooth UART receive ready signal	-	PD	DI	1.8V	GPIO177	-
SYSTEM								
B56	RESIN_N	Module reset signal	-	PU	DI	1.8V	-	-
B55	PWR_KEY	Module power on/off signal	-	PU	DI	1.8V	-	After the level changes from high to low and the hold time is greater than 37.4ms, it enters the power-on timing after the power-on timing.
C9	WAKEUP_IN	Wakeup input signal	Y	PD	DI	1.8V	-	-
C10	WAKEUP_OUT	Wakeup output signal	Y	PD	DO	1.8V	-	-
C28	DBG_UTXD0	Debug serial port transmit signal	-	PU	DO	1.8V	-	It is recommended to add TVS tube.
C12	DBG_URXD0	Debug serial port receive signal	-	PU	DI	1.8V	-	
C33	FORCE_BOOT	Forced download signal	-	PU	DI	1.8V	-	Low level enters boot.
D46	PHY_WAKE_HOST	PHY module wake-up signal	Y	PD	DIO	1.8V	GPIO82	-
D47	HOST_WAKE_PHY	Module wakeup PHY signal	Y	PD	DIO	1.8V	GPIO79	-
D34	SUSPEND_STATUS	Hibernate indication signal	Y	PD	DIO	1.8V	GPIO80	-
D49	STATUS_IND	BOOT_IND startup indication	Y	PD	DIO	1.8V	GPIO94	-
D48	SPI_INT_O	Six-wire SPI interrupt output	Y	PD	DIO	1.8V	GPIO197	-
D36	SPI_INT_IN	Six-wire SPI interrupt input	Y	PD	DIO	1.8V	GPIO93	-
D39	EINT0_Dump	Reserved only	Y	PD	DIO	1.8V	GPIO0	Configurable as GPIO
PPS								
C27	GPS_1PPS	GPS 1PPS synchronized output signal	-	PD	DO	1.8V	-	-
Reserve (function to be developed)								
B33	Reserve_B33	Reserved only Built-in HSM serial port to receive signals.	-	-	-	-	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
B34	Reserve_B34	Reserved only Built-in HSM serial port transmit signal.	-	-	-	-	-	-
A56	Reserve_A56	Reserved	-	-	-	-	-	-
USB								
B12	USB_VBUS	USB VBUS detection	-	-	DI	5V	-	Voltage divider circuit inside the module.
B27	HS_DM	HS USB differential signal -	-	-	AIO	3.3V	-	90Ω±10% impedance control.
B11	HS_DP	HS USB differential signal +	-	-	AIO	3.3V	-	
B28	USB_ID	USB ID detection pin	-	-	DI	1.8V	-	Default pull-up 1.8V.
B25	SS_RX_M	SS USB receive differential signal -	-	-	AI	1.2V	-	1. 90Ω±10% impedance control. 2. If not used, grounding treatment.
B9	SS_RX_P	SS USB receive differential signal +	-	-	AI	1.2V	-	
B10	SS_TX_P	SS USB transmit differential signal +	-	-	AO	1.2V	-	90Ω±10% impedance control.
B26	SS_TX_M	SS USB transmit differential signal -	-	-	AO	1.2V	-	
EMMC								
B42	SDC_RESET	EMMC reset signal	-	PU	DO	1.8V	-	-
B13	SDC0_DSL	EMMC data selector signal	-	PD	DI	1.8V	-	1. If not used, suspended processing. 2. HS400 mode to be connected.
B44	SDC_CMD	EMMC command signal	-	PU	DIO	1.8V	-	-
B45	SDC_CLK	EMMC clock signal	-	PD	DIO	1.8V	-	-
B14	SDC_DATA0	EMMC data bit 0	-	PD	DIO	1.8V	-	-
B15	SDC_DATA1	EMMC data bit 1	-	PD	DIO	1.8V	-	-
B16	SDC_DATA2	EMMC data bit 2	-	PD	DIO	1.8V	-	-
B17	SDC_DATA3	EMMC data bit 3	-	PD	DIO	1.8V	-	-
B30	SDC_DATA4	EMMC data bit 4	-	PD	DIO	1.8V	-	-
B31	SDC_DATA5	EMMC data bit 5	-	PD	DIO	1.8V	-	-
B32	SDC_DATA6	EMMC data bit 6	-	PD	DIO	1.8V	-	-
B43	SDC_DATA7	EMMC data bit 7	-	PD	DIO	1.8V	-	-
UART for GNSS								
C5	AP_UART_TX	UART transmit signal	-	PD	DO	1.8V	-	-
C6	AP_UART_RX	UART receive signal	-	PD	DI	1.8V	-	-
C21	AP_UART_CTS	UART receive ready signal	-	PD	DI	1.8V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
C22	AP_UART_RTS	UART transmit request signal	-	PD	DO	1.8V	-	-
V2X								
A54	V2X_UTXD	V2X serial communication transmit signal	-	PD	DO	1.8V	-	-
A55	V2X_URXD	V2X serial communication receive signal	-	PD	DI	1.8V	-	-
A60	V2X_SYNC	V2X eNB system pulse signal	-	PD	DIO	1.8V	-	Configurable as GPIO
A61	V2X_Boot12	V2X Boot GPIO	-	PD	DIO	1.8V	-	Configurable as GPIO
B50	V2X_Slave_Ready	V2X SPI slave ready signal	-	PD	DIO	1.8V	-	-
B29	V2X_BOOT9	V2X Boot GPIO	Y	PD	DIO	1.8V	-	Configurable as GPIO
SPI for MCU								
C23	MCU_SPI_MISO	SPI data signal NAD input/slave output	-	PD	DI	1.8V	-	Only the master mode is supported.
C24	MCU_SPI_MOSI	SPI data signal NAD output	-	PD	DO	1.8V	-	
C7	MCU_SPI_CLK	SPI clock signal	-	PD	DO	1.8V	-	
C8	MCU_SPI_CSB	SPI chip select signal	-	PD	DO	1.8V	-	
SPI for v2x								
C49	V2X_SPI_MISO	SPI data signal NAD input/slave output	-	PD	DI	1.8V	-	Master-slave mode is supported.
C50	V2X_SPI_MOSI	SPI data signal NAD output	-	PD	DO	1.8V	-	
C37	V2X_SPI_CLK	SPI clock signal	-	PD	DIO	1.8V	-	
C38	V2X_SPI_CSB	SPI chip select signal	-	PD	DIO	1.8V	-	
I²S for CODEC								
C18	CDC_I²S_MCLK	I²S master clock signal	-	PD	DO	1.8V	-	-
C19	CDC_I²S_DIN	I²S data input signal	-	PD	DI	1.8V	-	-
C1	CDC_I²S_SCK	I²S bit clock signal	-	PD	DIO	1.8V	-	-
C3	CDC_I²S_DOUT	I²S data output signal	-	PD	DO	1.8V	-	-
C2	CDC_I²S_WS	I²S chip select signal	-	PD	DIO	1.8V	-	-
PCM for WIFI6								
C4	BT_PCM_CLK	PCM clock signal	-	PD	DIO	1.8V	-	-
C34	BT_PCM_DOUT	PCM data output signal	-	PD	DO	1.8V	-	-
C46	BT_PCM_DIN	PCM data input signal	-	PD	DI	1.8V	-	-
C20	BT_PCM_SYNC	PCM synchronization signal	-	PD	DIO	1.8V	-	-
I²C_0 for Sensor								
C35	IMU_I²C0_SDA	I²C0 data signal	-	PU	DIO	1.8V	-	-
C36	IMU_I²C0_SCL	I²C0 clock signal	-	PU	DIO	1.8V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
C40	SENSOR_INT1	Sensor interrupt 1	Y	PD	DIO	1.8V	GPIO30	-
C41	SENSOR_INT2	Sensor interrupt 2	Y	PD	DIO	1.8V	GPIO29	-
I²C_1 for Codec								
C47	CDC_I²C1_SDA	I²C1 data signal	-	PU	DIO	1.8V	-	-
C48	CDC_I²C1_SCL	I²C1 clock signal	-	PU	DIO	1.8V	-	-
C39	CDC_RESET_N	Codec reset signal	Y	PD	DIO	1.8V	GPIO26	-
C11	EINT	Interrupt signal	Y	PD	DIO	1.8V	GPIO28	Configurable as GPIO
External HSM								
C25	HSM_INT1	External HSM interrupt signal	Y	PU	DIO	1.8V	GPIO170	-
C26	HSM_INT0	External HSM interrupt signal	Y	PU	DIO	1.8V	GPIO169	-
C44	HSM_RST	External HSM reset signal	Y	PD	DIO	1.8V	GPIO181	-
C42	HSM_SPI_CLK	SPI clock signal	-	PD	DO	1.8V	-	Only the master mode is supported.
C43	HSM_SPI_MI	SPI master device input signal	-	PD	DI	1.8V	-	
C54	HSM_SPI_MO	SPI master device output signal	-	PD	DO	1.8V	-	
C55	HSM_SPI_CSB	SPI chip select signal	-	PD	DO	1.8V	-	
SGMII								
B52	SGMII_1_RXN	SGMII_1 receives differential signals -	-	-	AIO	1.2V	-	If not used, the RX needs to be grounded.
B53	SGMII_1_RXP	SGMII_1 receive differential signal +	-	-	AIO	1.2V	-	If not used, the RX needs to be grounded.
B62	SGMII_1_TXN	SGMII_1 transmits differential signals -	-	-	AIO	1.2V	-	-
B63	SGMII_1_TXP	SGMII_1 transmits differential signal +	-	-	AIO	1.2V	-	-
B60	GBE1_RST	GBE1 reset signal	-	PD	DO	1.8V	-	-
B61	GBE1_INT	GBE1 interrupt signal	-	PD	DI	1.8V	-	-
C59	SGMII_MDIO	Management data communication signal	-	PD	DIO	1.8V	-	-
C60	SGMII_MDC	Management data signal clock	-	PD	DO	1.8V	-	-
C61	GBE0_RST	GBE0 reset signal	-	PD	DO	1.8V	-	-
B59	GBE0_INT	GBE0 interrupt signal	-	PD	DI	1.8V	-	-
C62	SGMII_0_TXP	SGMII_0 transmit differential signal +	-	-	AO	1.2V	-	-
C63	SGMII_0_TXN	SGMII_0 transmits differential signal -	-	-	AO	1.2V	-	-
C52	SGMII_0_RXP	SGMII_0 receive differential signal +	-	-	AI	1.2V	-	If not used, the RX needs to be grounded.

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
C53	SGMII_0_RXN	SGMII_0 receives differential signal -	-	-	AI	1.2V	-	If not used, the RX needs to be grounded.
GPIO								
D33	GPIO_01	General GPIO	Y	PD	DIO	1.8V	GPIO81	-
D35	GPIO_02	General GPIO	Y	PD	DIO	1.8V	GPIO198	-
D38	GPIO_03	General GPIO	Y	PD	DIO	1.8V	GPIO91	-
D37	GPIO_04	General GPIO	Y	PD	DIO	1.8V	GPIO95	-
D50	GPIO_05	General GPIO	Y	PD	DIO	1.8V	GPIO92	-
D54	GPIO_06	General GPIO	Y	PD	DIO	1.8V	GPIO141	-
D42	GPIO_07	General GPIO	Y	PD	DIO	1.8V	GPIO140	-
D53	GPIO_08	General GPIO	Y	PD	DIO	1.8V	GPIO139	-
D41	GPIO_09	General GPIO	Y	PD	DIO	1.8V	GPIO138	-
D52	GPIO_10	General GPIO	Y	PD	DIO	1.8V	GPIO165	-
D40	GPIO_11	General GPIO	Y	PD	DIO	1.8V	GPIO164	-
C56	GPIO_12	General GPIO	Y	PD	DIO	1.8V	GPIO116	-
C45	GPIO_13	General GPIO	Y	PD	DIO	1.8V	GPIO112	-
GNSS_LNA_Enable								
D45	GNSS_ELNA_EN0	GNSS L1 external LAN enable signal 0	-	PD	DO	1.8V	-	Specific for GNSS LNA
D56	GNSS_ELNA_EN1	GNSS L5 external LAN enable signal 1	-	PD	DO	1.8V	-	Specific for GNSS LNA
ADC								
A53	ADC0_AP	ADC0	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D55	ADC1_AP	ADC1	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D44	ADC2_AP	ADC2	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D43	ADC3_AP	ADC3	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
PM_ADC								
B51	ADC_PM	PM ADC	-	-	AI	0.04V to 1.78V	-	Without internal pull-up. If not used, grounding is required.
SDIO								
D51	MSDC1_CMD	SD card command signal	-	PD	DIO	1.86V/3V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
D59	MSDC1_CLK	SD card clock signal	-	PD	DIO	1.86V/3V	-	-
D60	MSDC1_DAT3	SD card data bit 3	-	PD	DIO	1.86V/3V	-	-
D61	MSDC1_DAT2	SD card data bit 2	-	PD	DIO	1.86V/3V	-	-
D62	MSDC1_DAT1	SD card data bit 1	-	PD	DIO	1.86V/3V	-	-
D63	MSDC1_DAT0	SD card data bit 0	-	PD	DIO	1.86V/3V	-	-
GND								
A2,A3,A5,A10,A18,A19,A20,A21,A26,A40,A52,A57,A58,A59,A62,A63,A64,A65, B41,B54,B57,B58,B64,B65, C13,C15,C16,C29,C30,C31,C32,C51,C57,C58,C64,C65, D1,D3,D4,D6,D7,D9,D10,D12,D13,D15,D16,D18-D32,D57,D58,D64,D65, E1-E16,F1-F81						GND		

Note

1. The AN758-NA-H880 does not support the V2X function, but can be used with the V2X module (AX166) from FIBOCOM.

3.2 Power Supply

The AN758-NA-H880 series modules use the standard power supply pin in the LGA interface to provide power for the module. The power supply input range is 3.4V~4.2V, and the recommended value is 3.8V, and the power supply continuous power supply capability shall not be lower than the performance of 3A power supply, such as the load capability, the magnitude of the ripple, etc., which directly affects the performance and stability of the module.

3.2.1 Power Supply

The AN758-NA-H880 series modules provide power supply power through the VPH_PWR pin.

Table 3-3 module power supply interfaces

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
Power								
A7	VPH_IN_A7	Module power input	-	-	PI	3.8V	-	Peak current 3.8V/3A (25°C)
A8	VPH_IN_A8	Module power input	-	-	PI	3.8V	-	
A23	VPH_IN_A23	Module power input	-	-	PI	3.8V	-	
A24	VPH_IN_A24	Module power input	-	-	PI	3.8V	-	
A51	EMMC_VCC_OUT1	EMMC VCC power output	-	-	PO	3.0V	-	800mA
A50	EMMC_VCC_OUT2	EMMC VCC power output	-	-	PO	3.0V	-	
A25	EMMC_VCCQ_OUT	EMMC VCCQ power output	-	-	PO	1.8V	-	200mA
A9	VIO_1V8_OUT	1.8V interface power supply output	-	-	PO	1.8V	-	100mA

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
A37	Reserve_A37	Reserved	-	-	-	-	-	-
A38	Reserve_A38	Reserved	-	-	-	-	-	-
A39	Reserve_A39	Reserved	-	-	-	-	-	-

Table 3-4 module power supply parameters

Parameter	Minimum value	Recommended value	Maximum value	Unit
VPH_IN_A7,A8,A23,A24	3.4	3.8	4.2	V

The power supply design is shown in figure:

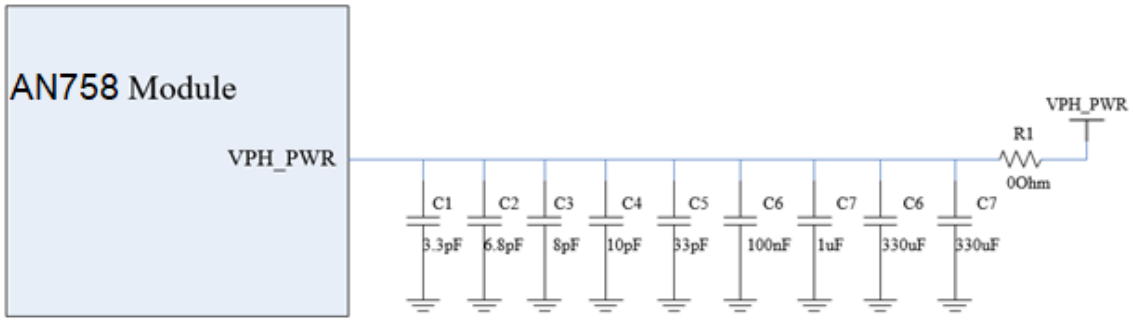


Figure 3-2 power supply design diagram

The filter capacitors for the power supply are designed as shown in the table below:

Table 3-5 filter capacitor design for power supply

Recommended Capacitance	Application	Description
330uF x 2	Voltage regulator capacitors	Reducing power fluctuations during module operation requires low ESR capacitors. LDO or DC-DC power supply requires no less than 680uF capacitance. Battery power supply can be appropriately reduced to 100 - 330uF capacitance.
1uF,100nF	Digital signal noise	Filtering of clock and digital signal interference.
39pF,33pF	700/850/900 MHz band	Filter out RF interference (low frequency band).
3.3pF,6.8pF,8pF, 10pF	1500/1700/1800/1900/2100/2300/2500/ 2600/3500/3700 MHz, 5GHz band	Filtering of RF interference (middle and high frequency bands).

An example of a power supply voltage drop is shown below:

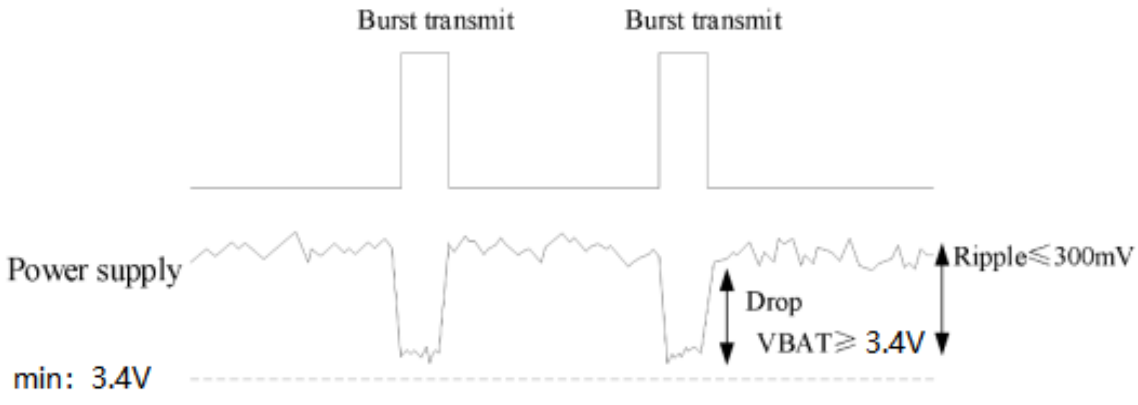


Figure 3-3 example diagram of supply voltage dips

In order to ensure that the power supply voltage is not less than 3.4V, near the module power input, it is recommended to connect in parallel two low ESR 330uF tantalum capacitors, as well as 1uF, 100nF, 39pF, 33pF, and other filter capacitors, and it is recommended that the power supply PCB alignments are as short as possible and wide enough, to reduce the power supply alignments of the equivalent impedance, to ensure that in the maximum power of the transmitter under the high current will not produce too large a voltage drop.

3.2.2 Power Output

The AN758-NA-H880 has 5 power outputs for external EMMC, SIM card and 1.8V peripheral interfaces such as codec/sensor/RGMII.

Table 3-6 power supply description

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
Power								
A51	EMMC_VCC_OUT1	EMMC VCC power supply output	-	-	PO	3.0V	-	800mA
A50	EMMC_VCC_OUT2		-	-	PO	3.0V	-	
A25	EMMC_VCCQ_OUT	EMMC VCCQ power supply output	-	-	PO	1.8V	-	200mA
A9	VIO_1V8_OUT	1.8V interface power supply output	-	-	PO	1.8V	-	100mA
A6	VDD_UIM1	UIM1 card power supply	-	-	PO	1.8V/ 3.0V	-	200mA
A35	VDD_UIM2	UIM1 card power supply 2	-	-	PO	1.8V/ 3.0V	-	200mA

3.2.3 Power Consumption

Table 3-7 AN758-NA-H880 power consumption description

Parameter	Description	Adjustment	TYP	Unit	Remarks
I_{off}	Power off	--	50	uA	--
I_{sleep}	GSM	DRX=5	4.5	mA	--
	WCDMA	DRX=8	4.2	mA	--
	TDD LTE	DPC(Default Paging Cycle)=#128	4.6	mA	--
	FDD LTE	DPC(Default Paging Cycle)=#128	4.6	mA	--
	SA	DRX=128	7.2	mA	--
	Radio Off	AT+CFUN=4 Flight Mode	3.9	mA	--
$I_{GSM-RMS}$	GSM	GSM850 PCL5	TBD	mA	--
		GSM900 PCL5	458	mA	--
		DCS1800 PCL0	368	mA	--
		PCS1900 PCL0	TBD	mA	--
$I_{GPRS-RMS}$ CS4	GPRS	GPRS Data transfer GSM850; PCL=5; 1Rx/4Tx	TBD	mA	--

Parameter	Description	Adjustment	TYP	Unit	Remarks
		GPRS Data transfer GSM900; PCL=5; 1Rx/4Tx	828	mA	--
		GPRS Data transfer DCS1800; PCL=0; 1Rx/4Tx	568	mA	--
		GPRS Data transfer PCS1900; PCL=0; 1Rx/4Tx	TBD	mA	--
$I_{EGPRS-RMS}$ MCS9	EDGE	EDGE Data transfer GSM850; PCL=8; 1Rx/4Tx	TBD	mA	--
		EDGE Data transfer GSM900; PCL=8; 1Rx/4Tx	512	mA	--
		EDGE Data transfer DCS1800; PCL=2; 1Rx/4Tx	575	mA	--
		EDGE Data transfer PCS1900; PCL=2; 1Rx/4Tx	TBD	mA	--
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power	983	mA	--
		Band2@ max power	TBD	mA	--
		Band4@ max power	TBD	mA	--
		Band5@ max power	TBD	mA	--
$I_{LTE-RMS}$	FDD data RMS Current	Band1@max power (10MHz,1RB)	986	mA	--
		Band2@max power (10MHz,1RB)	TBD	mA	--
		Band3@max power (10MHz,1RB)	855	mA	--
		Band4@max power (10MHz,1RB)	TBD	mA	--
		Band5@max power (10MHz,1RB)	797	mA	--
		Band7@max power (10MHz,1RB)	1050	mA	--
		Band12@max power (10MHz,1RB)	TBD	mA	--
		Band13@max power (10MHz,1RB)	TBD	mA	--
		Band14@max power (10MHz,1RB)	TBD	mA	--
		Band17@max power (10MHz,1RB)	TBD	mA	--
		Band25@max power (10MHz,1RB)	TBD	mA	--
		Band26@max power (10MHz,1RB)	TBD	mA	--
		Band28@max power (10MHz,1RB)	789	mA	--
		Band66@max power (10MHz,1RB)	TBD	mA	--
		Band71@max power (10MHz,1RB)	TBD	mA	--
	TDD data RMS Current	Band38@max power (10MHz,1RB)	490	mA	--
		Band40@max power (10MHz,1RB)	506	mA	--
		Band41@max power (10MHz,1RB)	549	mA	--
		Band48@max power (10MHz,1RB)	TBD	mA	--

Parameter	Description	Adjustment	TYP	Unit	Remarks
I_{NR-RMS}	FDD data RMS Current	N1@max power (50MHz, RB135@67)	1017	mA	--
		N2@max power (20MHz, RB50@25)	TBD	mA	--
		N3@max power (40MHz, RB108@54)	1053	mA	--
		N5@max power (20MHz, RB50@25)	851	mA	--
		N7@max power (20MHz, RB50@25)	1325	mA	--
		N12@max power (15MHz, RB36@18)	TBD	mA	--
		N14@max power (10MHz, RB25@12)	TBD	mA	--
		N25@max power (20MHz, RB50@25)	TBD	mA	--
		N28@max power (30MHz, RB80@40)	855	mA	--
		N66@max power (40MHz, RB108@54)	TBD	mA	--
		N71@max power (20MHz, RB50@25)	TBD	mA	--
	TDD data RMS Current	n38@max power (20MHz, RB25@12)	408	mA	--
		n40@max power (80MHz, RB108@54)	399	mA	--
		n41@max power (100MHz, RB135@67)	502	mA	--
		n48@max power (100MHz, RB135@67)	TBD	mA	--
		n77@max power (100MHz, RB135@67)	482	mA	--
		n78@max power (100MHz, RB135@67)	453	mA	--

Warning

1. Test conditions TEMP: 25℃, VPH_IN: 3.8V.
2. The power consumption is NA-H880 data, which is for reference only..

4 Antenna Interface

The AN758-NA-H880 series module adopts a 5-antenna scheme with 4 cellular antennas and 1 GNSS antenna with different bands and frequency ranges, and the following are the descriptions and illustrations of each antenna.

4.1 RF Antenna Interface Configuration

The AN758-NA-H880 provides four cellular antenna interfaces, and the antenna interface definitions are shown in the following table.

Table 4-1 AN758-EAU-H880 series antenna interface definitions

Antenna Interface	Pin	Description	Frequency Range (MHz)
MAIN	C17	ANT1	617–960 MHz
			1452–2690 MHz
			3300–4200 MHz
DRX/AUX	D2	ANT2	617–960 MHz
			1452–2690 MHz
			3300–4200 MHz
MIMO3	D14	ANT3	1710–2690 MHz
			3300–4200 MHz
MIMO4	D17	ANT4	1710–2690 MHz
			3300–4200 MHz

Table 4-2 AN758-NA-H880 band antenna assignments

BAND	TX	PRX	DRX	PRX_MIMO	DRX_MIMO
GSM850/GSM900/DCS1800/PCS1900	1	1	2	--	--
WCDMA B1/2/4/5	1	1	2	--	--
LTE B29 NR N29	--	1	1	--	--
LTE B4/5/12/13/14/17/25/26/28/66/71 NR N5/12/14/25/28/40/71	1	1	2	--	--
LTE B1/2/3/7/38/40/41 NR N1/2/3/7/38/41/66	1	1	2	3	4
LTE B48 NR N48 NR N77/78	1	1	3	2	4
备注：1=ANT1 MAIN；2=ANT2 DRX/AUX；3=ANT3 5G MIMO3；4=ANT4 5G MIMO4					

4.1.1 Operating Bands

Table 4-3 AN758-NA-H880 operating band and frequency range

Band	Tx	Rx	Unit
EGSM850	824~849	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B12	699~716	729~746	MHz
LTE-FDD B13	777~786.9	746~755.9	MHz
LTE-FDD B14	788~798	758~768	MHz
LTE-FDD B17	704~716	734~746	MHz
LTE-FDD B25	1850~1915	1930~1995	MHz
LTE-FDD B26	814~849	859~894	MHz
LTE-FDD B28	703~748	758~803	MHz
LTE-FDD B29	--	717~728	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2496~2690	2496~2690	MHz
LTE-FDD B66	1710~1780	2110~2200	MHz
LTE-FDD B71	663~698	617~652	MHz
LTE-TDD B48	3550~3700	3550~3700	MHz
5G NR n1	1920~1980	2110~2170	MHz
5G NR n2	1850~1910	1930~1990	MHz
5G NR n3	1710~1785	1805~1880	MHz
5G NR n5	824~849	869~894	MHz
5G NR n7	2500~2570	2620~2690	MHz
5G NR n12	699~716	729~746	MHz
5G NR n14	788~798	758~768	MHz
5G NR n25	1850~1915	1930~1995	MHz

Band	Tx	Rx	Unit
5G NR n28	703~748	758~803	MHz
5G NR n29	--	717~728	MHz
5G NR n38	2570~2620	2570~2620	MHz
5G NR n40	2300~2400	2300~2400	MHz
5G NR n41	2496~2690	2496~2690	MHz
5G NR n48	3550~3700	3550~3700	MHz
5G NR n66	1710~1780	2110~2200	MHz
5G NR n71	663~698	617~652	MHz
5G NR n77	3300~4200	3300~4200	MHz
5G NR n78	3300~3800	3300~3800	MHz

The circuit design is shown below:

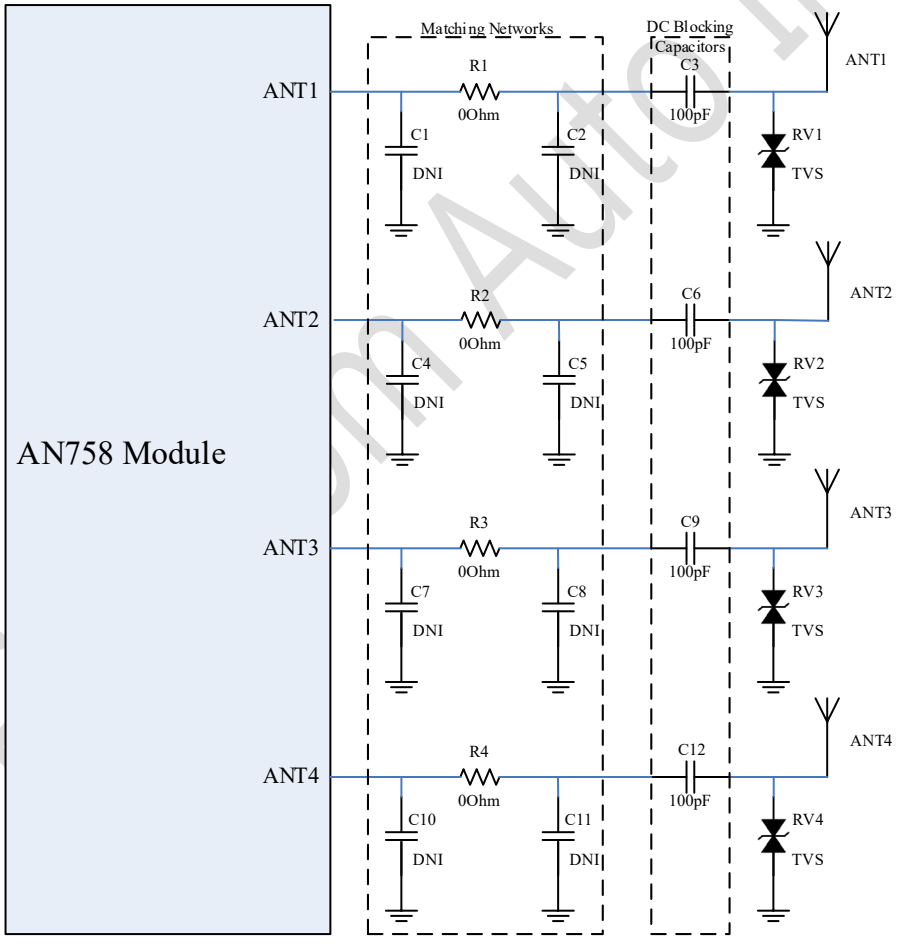


Figure 4-1 RF antenna circuit design

4.2 GNSS Antenna Interface

The module does not have a built-in GPS LNA, and an active antenna is recommended.The GNSS-related information is shown in the following table.

Table 4-4 GNSS antenna interface definitions

Pin Name	Pin	Description	Frequency Range (MHz)	Remarks
ANT-GNSS	C14	GPS L1+L5	L1(1559-1609MHz)+L5(1166-1187MHz)	-

4.2.1 Operating Bands

Table 4-5 GNSS operating frequency bands

Mode	Frequency	Frequency Range	Remarks
GPS L1	Center frequency(FC) = 1575.42 MHz	1574.4MHz~1576.4MHz	-
GLONASS G1	Center frequency(FC) = 1601.7 MHz	1597.5MHz~1605.9MHz	-
BeiDou B1	Center frequency(FC) = 1561 MHz	1559.1MHz~1563.1MHz	-
Galileo E1	Center frequency(FC) = 1575.42 MHz	1573.4MHz~1577.5MHz	-
GPS L5, Galileo E5a,BeiDou B2a	Center frequency(FC) = 1176.45 MHz	1166.22MHz~1186.68MHz	-

The circuit design is shown below:

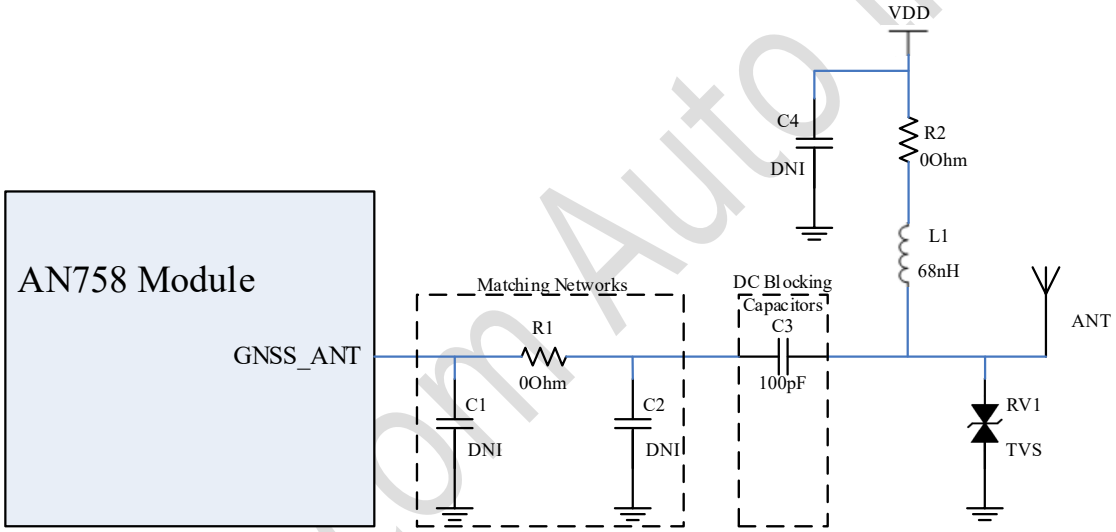


Figure 4-2 RF antenna circuit design

4.3 Antenna Requirements

The AN758-NA-H880 series modules provide four cellular RF transceiver antennas, one GNSS antenna interface, and the antenna requirements are shown in the following table:

Table 4-6 module antenna requirements

Type	Antenna Requirements
GSM/WCDMA/LTE/NR	VSWR: ≤ 2:1 Gain (dBi): 1 Maximum input power (W): 2 Input impedance (Ω): 50 Isolation band for each antenna (dB): > 25
GNSS (Recommended active antenna)	Frequency range: L1: 1559 MHz – 1609 MHz L5: 1166 MHz - 1187 MHz VSWR: < 2:1

Type	Antenna Requirements
	Antenna gain > -1dBi

4.4 Reference RF Signal Cable LAYOUT

In the circuit design of the RF antenna interface, in order to ensure good performance and reliability of the RF signal, it is recommended to follow the following design principles in the circuit design:

1）The distance between the RF signal pin and the RF connector should be as short as possible, and the insertion loss should be controlled within 1.5dB.

2）RF wiring should pay attention to the corners to avoid right-angle alignment, the use of arc processing, the antenna from the RF module needs to be made into a microstrip line.

3）RF ground should be reasonably designed, RF signal line reference ground plane should be complete; in the signal line and the reference ground around the increase of a certain amount of ground holes can help improve RF performance. The distance between the ground hole and the signal line should be at least 2 times the line width (2 x W).

4）PCB boards require precise 50Ω impedance control for RF signal lines.

5）It is recommended that the customer LAYOUT preliminary version and FIBOCOM pull-through review.

5 Other Interfaces

5.1 Control Interface

The control signals are used for on/off and reset control of the module.

Table 5-1 control signal pin definitions

Pin Name	I/O	Pin No.	Description
RESIN_N	DI	B56	When the module is working, pull down the RESET_N pin more than 0.25ms (edge triggered), the module reset.
PWR_KEY	DI	B55	1） In power off state, pull down PWR_KEY pin >37.4ms, then release, module power on. 2） In power-on state, pull down PWR_KEY pin for 3s - 8s, then release, module turns off.

5.1.1 Power-On/Off

5.1.1.1 Power-On

When the module is in power-off mode, pulling down PWR_KEY for more than 37.4ms and then releasing it can turn on the module. It is recommended to use the OC/OD driver circuit to control the PWR_KEY pin.

The reference circuit is shown below:

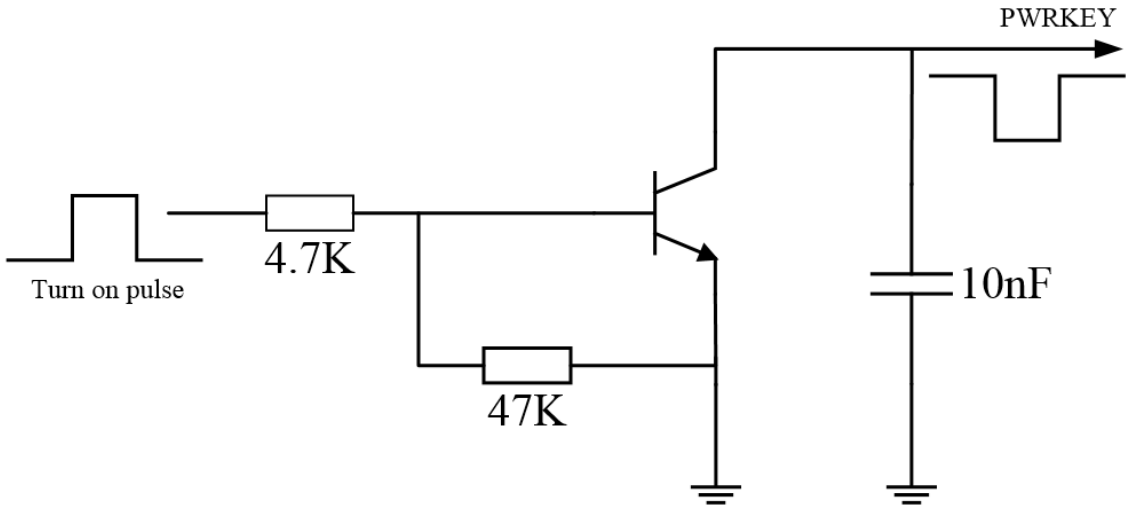


Figure 5-1 OC driver power-on reference circuit

Another way to control the PWR_KEY pin is directly through a pushbutton switch, a TVS (recommended ESD9X5VL-2/TR) needs to be placed near the button for ESD protection.

The reference circuit is shown below:

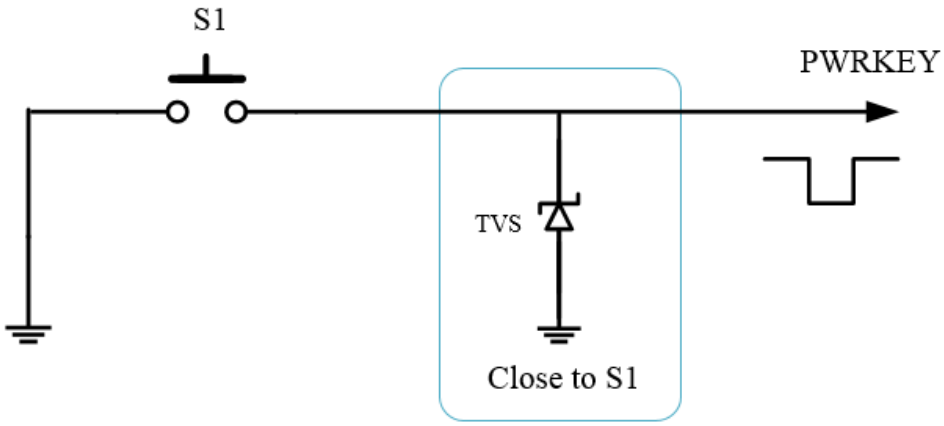


Figure 5-2 button power-on reference circuit

Note

1. If space permits, it is recommended to connect a 1K resistor in series with the back end of the TVS tube on the PWR_KEY line.

The power-on timing is shown below:

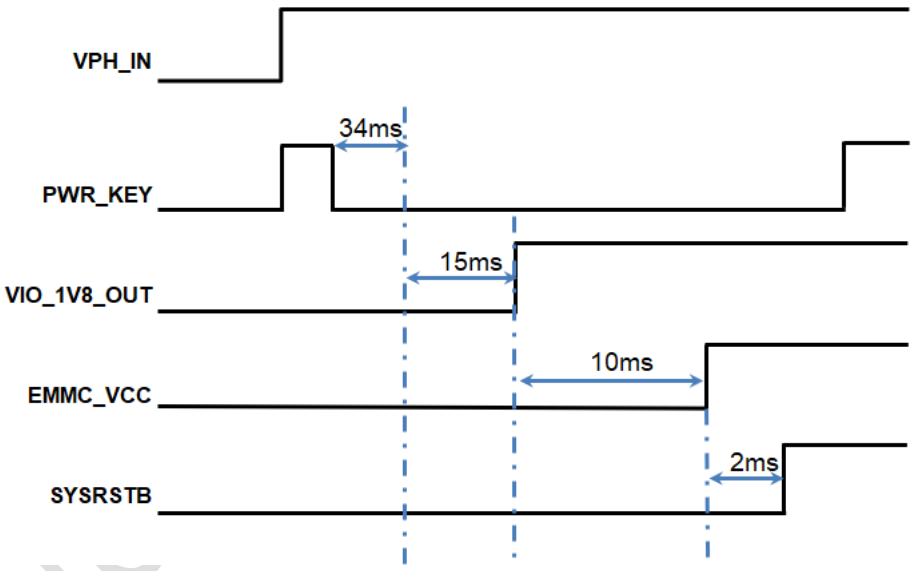


Figure 5-3 power-on timing

Note

1. Before pulling down the PWR_KEY pin, it is necessary to ensure that the VPH_PWR voltage is stable. It is recommended that the time interval between powering up VPH_PWR and pulling down the PWR_KEY pin is not less than 30ms.
2. Timing deviation ±10%.

5.1.1.2 Power-Off

The module supports two power-off methods.

Table 5-2 module power-off methods

Power-off method	Power-off operation	Applicable scenarios
Low voltage power-off	The module will power-off when VPH_PWR voltage is too low or power down.	At this point the module does not perform the normal shutdown process of logging off from the base station.
Hardware power-off	Pull down the PWR_KEY pin for 3s~8s, then release it.	Power off normally.

Note

1. When the module is working normally, do not cut off the module power immediately to avoid damaging the internal Flash of the module. it is strongly recommended to turn off the module by long pressing the PWR_KEY pin first, and then disconnect the power.
2. Timing deviation ±10%.

The power-off timing is shown below:

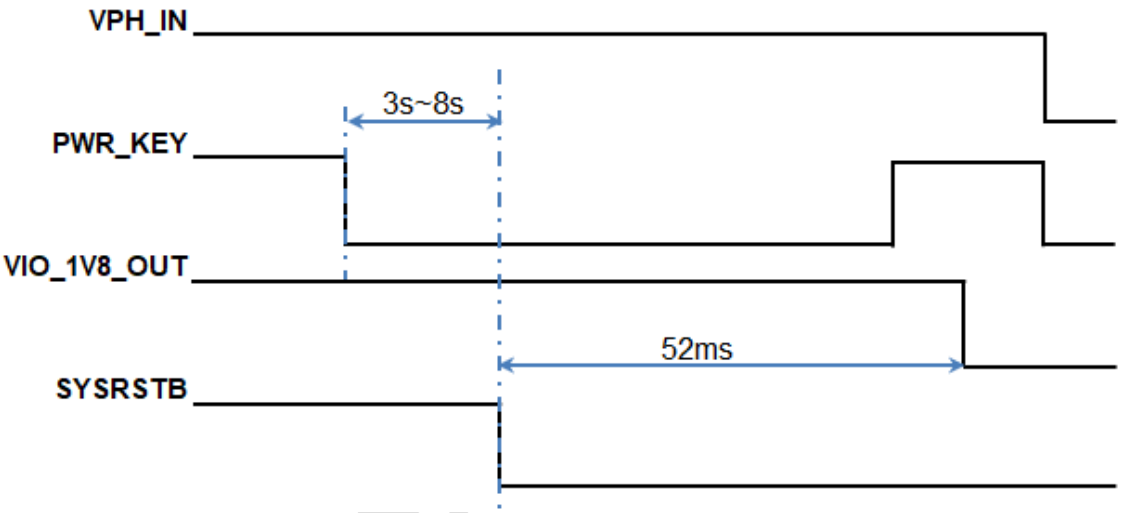


Figure 5-4 power-off timing

5.1.2 Reset

The module can be reset in two ways: hardware reset and software reset.

Table 5-3 reset methods

Reset Method	Reset Operation
Hardware reset	Pull the RESET_N pin low for more than 0.25ms, then pull it high.
Software reset	Send adb command *reboot*.

Customers can use both the OC/OD driver circuit and the pushbutton switch to control the RESET_N pin.

The reference circuits are shown in Figure 5-5 and Figure 5-6, respectively:

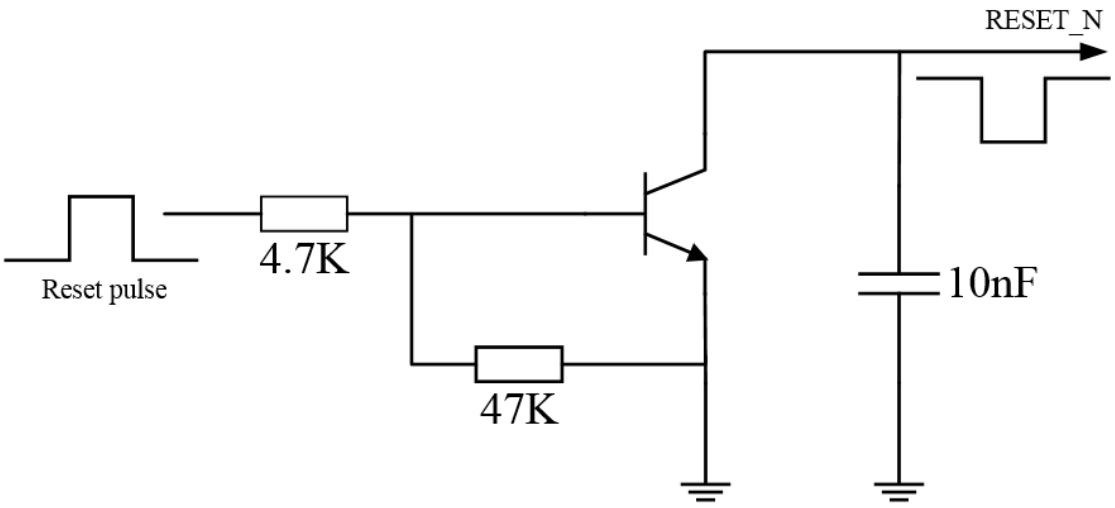


Figure 5-5 OC driver reset reference circuit

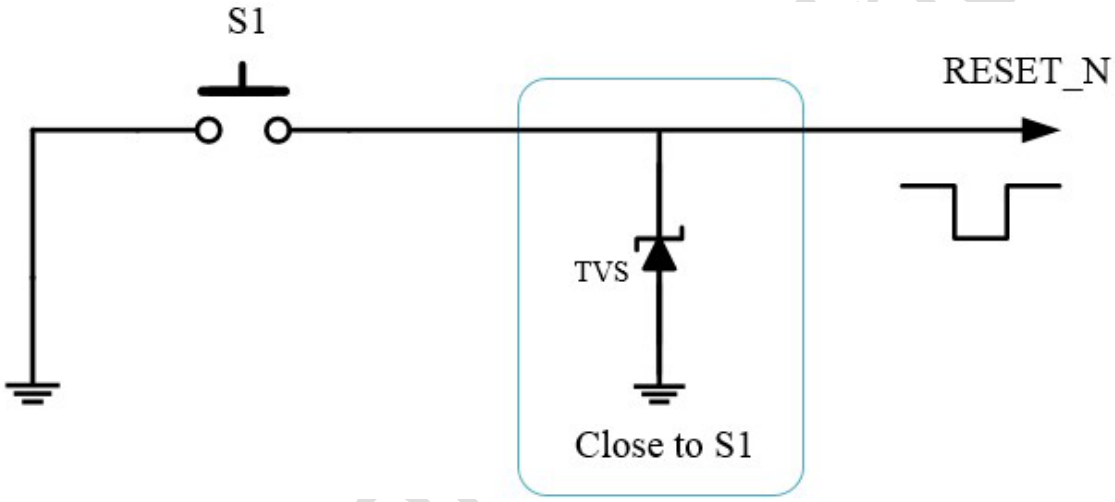


Figure 5-6 button reset reference circuit

The RESET_N reset timing is shown below:

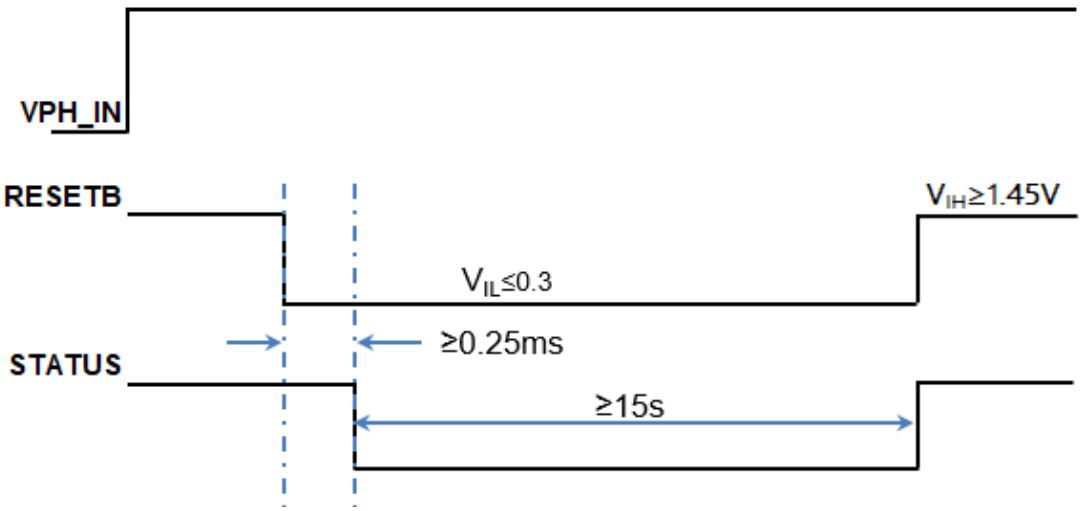


Figure 5-7 RESET_N reset timing

5.2 (U)SIM Card Interface

The module has built-in 2 sets of SIM card interfaces, supporting 1.8V and 3.0V (U)SIM cards.

5.2.1 (U)SIM Pin Definition

Table 5-4 (U)SIM pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
SIM								
A6	VDD_UIM1	UIM1 card power supply	-	-	PO	1.8V/ 3.0V	-	-
A22	UIM1_RST	UIM1 card reset signal	-	PD	DO	1.8V/ 3.0V	-	-
A36	UIM1_DATA	UIM1 card data signal	-	PD	DIO	1.8V/ 3.0V	-	-
A48	UIM1_CLK	UIM1 card clock signal	-	PD	DO	1.8V/ 3.0V	-	-
A49	UIM1_DET	UIM1 card insertion detection signal	-	PD	DI	1.8V	-	-
A35	VDD_UIM2	UIM2 card power supply	-	-	PO	1.8V/ 3.0V	-	-
A34	UIM2_RST	UIM2 card reset signal	-	PD	DO	1.8V/ 3.0V	-	-
A46	UIM2_DATA	UIM2 card data signal	-	PD	DIO	1.8V/ 3.0V	-	-
A47	UIM2_CLK	UIM2 card clock signal	-	PD	DO	1.8V/ 3.0V	-	-
A33	UIM2_DET	UIM2 card insertion detection signal	-	PD	DI	1.8V	-	-

5.2.2 (U)SIM Interface Circuit

5.2.2.1 (U)SIM Card Holder with Card Detect Signal

The module determines the (U)SIM card insertion and removal support by detecting the USIM_DET pin status: (U)SIM card insertion, SIM_DET pin is high; (U)SIM card removal, SIM_DET pin is low.

With card detection signal (U) SIM card holder circuit reference design is shown below:

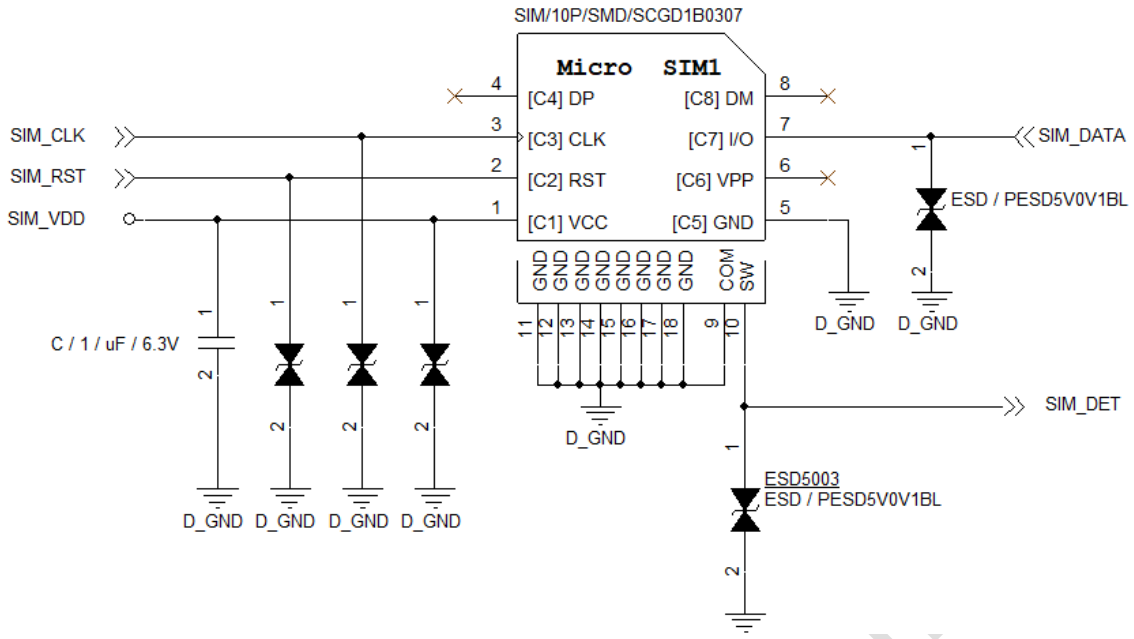


Figure 5-8 reference circuit design for card holders with card detection

5.2.2.2 eSIM Reference Circuitry

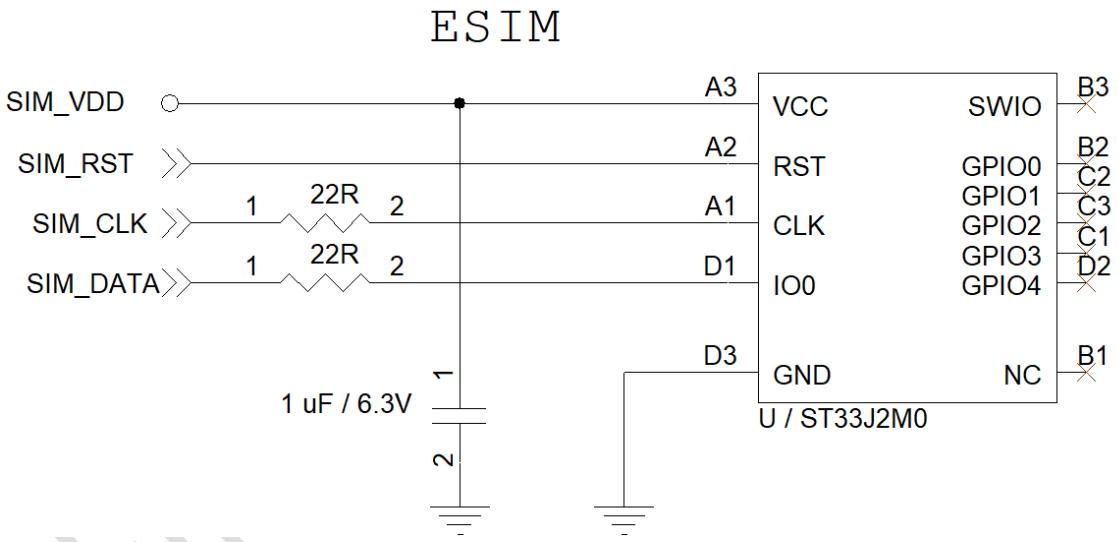


Figure 5-9 eSIM reference circuit design

5.2.3 (U)SIM Design Requirements

The (U)SIM card circuit design needs to meet the EMC standards and ESD requirements, and at the same time, it needs to improve the anti-interference ability to ensure that the (U) SIM card can work stably.

The following points need to be strictly observed in the design:

- Layout of the (U)SIM card holder as close as possible to the module and away from strong sources of interference such as RF antennas, DC-DC power supplies, clock signal lines, etc..
- Use the (U)SIM card holder with metal shielded enclosure so as to improve the anti-interference capability.
- The length of the alignment from the module to the (U)SIM card holder should not exceed 100mm; excessively long alignment will reduce signal quality.

- The USIM_CLK and USIM_DATA signal packets are ground isolated to avoid mutual interference. If conditions are restricted, at least the (U)SIM signals need to be protected as a set of packet grounds.
- Filter capacitors and ESD devices for the (U)SIM signal line are placed close to the (U)SIM card holder, ESD devices are recommended to choose low capacitance, please choose 22 pF – 33 pF capacitors for the filter capacitors, and the total loading capacitance on the signal line should not exceed 45 pF.

5.3 USB Interface

The module supports USB2.0/USB3.0, refer to "Universal Serial Bus Specification 2.0/ Universal Serial Bus Specification 3.0" for USB bus timing and electrical characteristics.

5.3.1 USB Interface Definition

Table 5-5 USB interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
USB								
B12	USB_VBUS	USB VBUS detection	-	-	DI	5V	-	Voltage divider circuit inside the module.
B27	HS_DM	HS USB differential signal -	-	-	AIO	3.3V	-	90Ω±10% impedance control.
B11	HS_DP	HS USB differential signal +	-	-	AIO	3.3V	-	
B28	USB_ID	USB ID detection pin	-	-	DI	1.8V	-	Default pull-up 1.8V.
B25	SS_RX_M	SS USB receive differential signal -	-	-	AI	1.2V	-	1. 90Ω±10% impedance control. 2. If not used, grounding treatment.
B9	SS_RX_P	SS USB receive differential signal +	-	-	AI	1.2V	-	
B10	SS_TX_P	SS USB transmit differential signal +	-	-	AO	1.2V	-	90Ω±10% impedance control.
B26	SS_TX_M	SS USB transmit differential signal -	-	-	AO	1.2V	-	

For more information on the USB 2.0/USB3.0 specification, visit http://www.usb.org/home.

Warning

1. Since the module supports USB 2.0/USB3.0:
   - The equivalent capacitance of the TVS tube on the HS_DM/DP signal line is required to be lower than 3 pF, and the equivalent capacitance of the TVS tube on the SS_TX_P/M, SS_RX_P/M signal lines is required to be lower than 0.5pF.
   - Recommend to string 0 ohm resistors on each of the HS_DM/DP, SS_TX_P/M, and SS_RX_P/M differential lines.
   - There are no series/parallel devices on HS_DM/DP, SS_TX_P/M, SS_RX_P/M differential lines inside the module. It is recommended to reserve common mode inductors on HS_DM/DP; AC coupling capacitors on SS_TX_P/M with a recommended capacitance value of 100nF, and AC coupling capacitors on SS_RX_P/M with a recommended capacitance value of 330 nF.

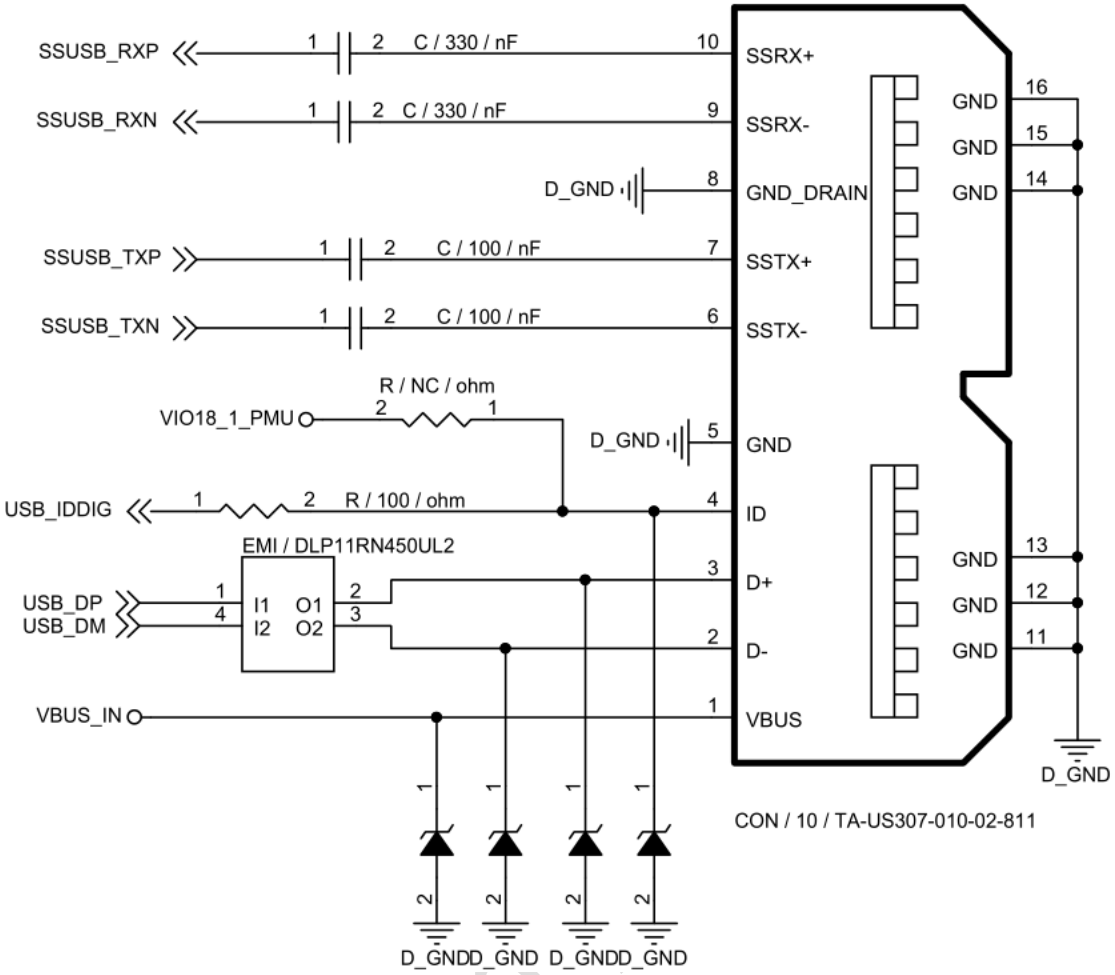


Figure 5-10 USB3.0 reference circuitry

HS_DM/DP, SS_TX_P/M, and SS_RX_P/M are high-speed differential signal lines, and the following rules must be strictly adhered to in PCB Layout:

- HS_DM and HS_DP, SS_TX_P and SS_TX_M, SS_RX_P and SS_RX_M signal lines control differential impedance 90 Ω.
- HS_DM and HS_DP, SS_TX_P and SS_TX_M, SS_RX_P and SS_RX_M signal lines are required to be of equal length and parallel, avoiding right-angle alignment.
- HS_DM and HS_DP, SS_TX_P and SS_TX_M, SS_RX_P and SS_RX_M signal lines are routed at the signal layer closest to the ground layer, and the alignment is protected by wrapping the top, bottom, left and right sides of the line with ground.

5.4 UART Interface

5.4.1 UART Interface Definition

The module has 4 sets of serial ports: 2 sets of main serial ports, 1 set of debug serial ports, and 1 set of V2X dedicated serial ports.

The main serial port and V2X dedicated serial port support:

4800bps/9600bps/19200bps/38400bps/57600bps/115200bps/230400bps/380400bps/460800bps/921600bps, and the

default baud rate is 921600bps for data transmission and AT command transmission.

The debugging serial port supports 921600 bps, which is only used for internal debugging by FIBOCOM.

Table 5-6 UART pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
UART for BT								
B37	BT_UART_RX	Bluetooth UART receive signal	-	PD	DI	1.8V	GPIO180	-
B38	BT_UART_TX	Bluetooth UART transmit signal	-	PD	DO	1.8V	GPIO179	-
B40	BT_UART_RTS_N	Bluetooth UART transmit request signal	-	PD	DO	1.8V	GPIO178	-
B39	BT_UART_CTS_N	Bluetooth UART receive ready signal	-	PD	DI	1.8V	GPIO177	-
UART for Debug								
C28	DBG_UTXD0	Debug serial port transmit signal	-	PU	DO	1.8V	-	It is recommended to add TVS tube.
C12	DBG_URXD0	Debug serial port receive signal	-	PU	DI	1.8V	-	
UART for GNSS								
C5	AP_UART_TX	UART transmit signal	-	PD	DO	1.8V	-	-
C6	AP_UART_RX	UART receive signal	-	PD	DI	1.8V	-	-
C21	AP_UART_CTS	UART receive ready signal	-	PD	DI	1.8V	-	-
C22	AP_UART_RTS	UART transmit request signal	-	PD	DO	1.8V	-	-
UART for V2X								
A54	V2X_UTXD	V2X serial communication transmit signal	-	PD	DO	1.8V	-	-
A55	V2X_URXD	V2X serial communication receive signal	-	PD	DI	1.8V	-	-

5.4.2 UART Interface Application

The serial port level of the module is 1.8V, if the customer's host system level is 3.3V or other, it is necessary to add a level converter in the serial port connection between the module and the host.

The following figure shows the reference circuit design of the serial port level converter chip:

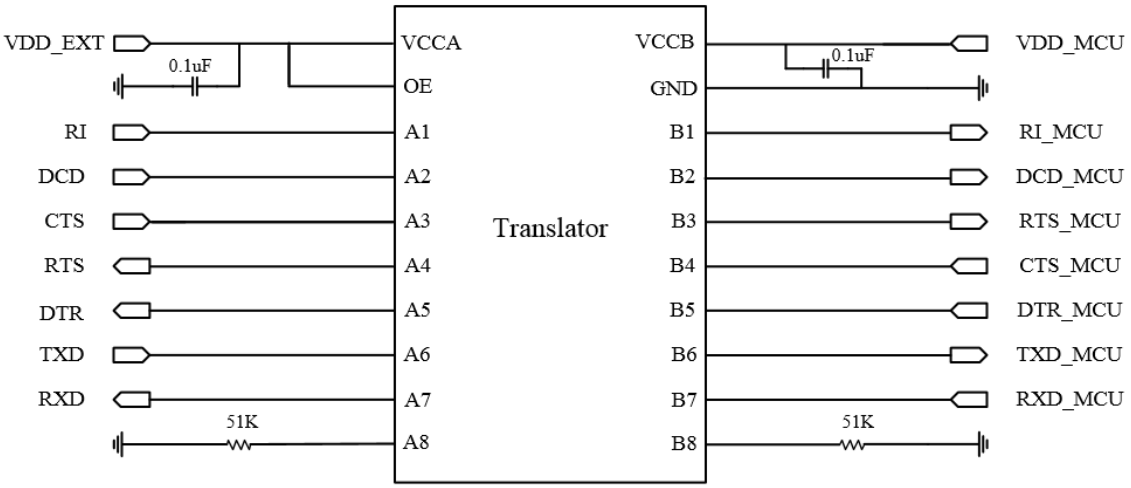


Figure 5-11 level shifter reference circuit

5.5 ADC Interface

The module provides a five-channel analog-to-digital converter interfaces.

Table 5-7 ADC pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
ADC								
A53	ADC0_AP	ADC0	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D55	ADC1_AP	ADC1	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D44	ADC2_AP	ADC2	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
D43	ADC3_AP	ADC3	-	-	AIO	0.05V to 1.45V	-	If not used, grounding is required.
PM_ADC								
B51	ADC_PM	PM ADC	-	-	AI	0.04V to 1.78V	-	Without internal pull-up. If not used, grounding is required.

Warning

1. Recommended for ADC to do ground wrap when wiring.
2. ADC_PM is a 10-bit ADC, controlled by PMIC, no internal pull-up, input voltage range: 0.04V to 1.78V, reading error ±17mV.
3. ADC0-3 are 12-bit ADCs, controlled by AP, input voltage range: 0.05V to 1.45V, reading error ±10mV.

5.6 Digital Audio

The module provides two sets of digital audio interfaces, I²S and PCM, which enable communication with digital audio devices such as external Codecs.

- Both support master and slave modes.
- PCM supports 24bits, 48KHz.
- I²S supports 32bits, 192KHz (master).

5.6.1 Audio Interface Definition

Table 5-8 I²S interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
I²S for CODEC								
C18	CDC_I²S_MCLK	I²S master clock signal	-	PD	DO	1.8V	-	-
C19	CDC_I²S_DIN	I²S data input signal	-	PD	DI	1.8V	-	-
C1	CDC_I²S_SCK	I²S bit clock signal	-	PD	DIO	1.8V	-	-
C3	CDC_I²S_DOUT	I²S data output signal	-	PD	DO	1.8V	-	-
C2	CDC_I²S_WS	I²S chip select signal	-	PD	DIO	1.8V	-	-
PCM for BT Audio								
C4	BT_PCM_CLK	PCM clock signal	-	PD	DIO	1.8V	-	-
C34	BT_PCM_DOUT	PCM data output signal	-	PD	DO	1.8V	-	-
C46	BT_PCM_DIN	PCM data input signal	-	PD	DI	1.8V	-	-
C20	BT_PCM_SYNC	PCM synchronization signal	-	PD	DIO	1.8V	-	-

5.7 External Flash Interface

The module provides 2 sets of interfaces, one set of SDIO interface supporting SD 3.0 and one set of EMMC interface supporting EMMC5.1.

5.7.1 EMMC Interface Definition

Table 5-9 EMMC interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
EMMC								
B42	SDC_RESET	EMMC reset signal	-	PU	DO	1.8V	-	-
B13	SDC0_DSL	EMMC data selector signal	-	PD	DI	1.8V	-	1. If not used, suspended processing.

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
EMMC								
								2. HS400 mode to be connected.
B44	SDC_CMD	EMMC command signal	-	PU	DIO	1.8V	-	-
B45	SDC_CLK	EMMC clock signal	-	PD	DIO	1.8V	-	-
B14	SDC_DATA0	EMMC data bit 0	-	PD	DIO	1.8V	-	-
B15	SDC_DATA1	EMMC data bit 1	-	PD	DIO	1.8V	-	-
B16	SDC_DATA2	EMMC data bit 2	-	PD	DIO	1.8V	-	-
B17	SDC_DATA3	EMMC data bit 3	-	PD	DIO	1.8V	-	-
B30	SDC_DATA4	EMMC data bit 4	-	PD	DIO	1.8V	-	-
B31	SDC_DATA5	EMMC data bit 5	-	PD	DIO	1.8V	-	-
B32	SDC_DATA6	EMMC data bit 6	-	PD	DIO	1.8V	-	-
B43	SDC_DATA7	EMMC data bit 7	-	PD	DIO	1.8V	-	-

EMMC interface features:

- Supports EMMC 5.1 protocols
- Supports high speed SDR/DDR mode
- Supports HS200/HS400
- Supports 1/4/8-bit bus bandwidth

EMMC design requirements:

- EMMC signals need to be stereo wrapped to ground with impedance controlled at 50Ω ±10%.
- EMMC signals inner layer alignment, alignment spacing to maintain 1 times line width.
- EMMC other alignment to be maintained with the DATA line 1.5 times line width.
- EMMC alignment length is to be less than 50.8mm and alignment width is to be more than 0.2mm.
- CLK/DSL and DATA/CMD alignment length difference should be less than 7.62mm.
- Capacitance on the power supply should be more than 0.1UF.
- It is recommended to reserve series resistors on the clock signal line.
- Chip select signal: if configure HS400 mode, it needs to be connected; if not, it needs to be overhang design and cannot be configured for other functions.

EMMC interface module internal alignment:

Table 5-10 EMMC internal alignment

Pin	DSL	CMD	CLK	D0	D1	D2	D3	D4	D5	D6	D7
Alignment Length (mm)	16.27	14.66	17.04	13.618	13.946	13.57	13.614	14.187	14.164	13.824	14.213

5.7.2 SDIO Interface Definition

Table 5-11 SDIO interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
SDIO								
D51	MSDC1_CMD	SD card command signal	-	PD	IO	1.86V/3V	-	-
D59	MSDC1_CLK	SD card clock signal	-	PD	IO	1.86V/3V	-	-
D60	MSDC1_DAT3	SD card data bit 3	-	PD	IO	1.86V/3V	-	-
D61	MSDC1_DAT2	SD card data bit 2	-	PD	IO	1.86V/3V	-	-
D62	MSDC1_DAT1	SD card data bit 1	-	PD	IO	1.86V/3V	-	-
D63	MSDC1_DAT0	SD card data bit 0	-	PD	IO	1.86V/3V	-	-

The module and SDIO reference design is shown below:

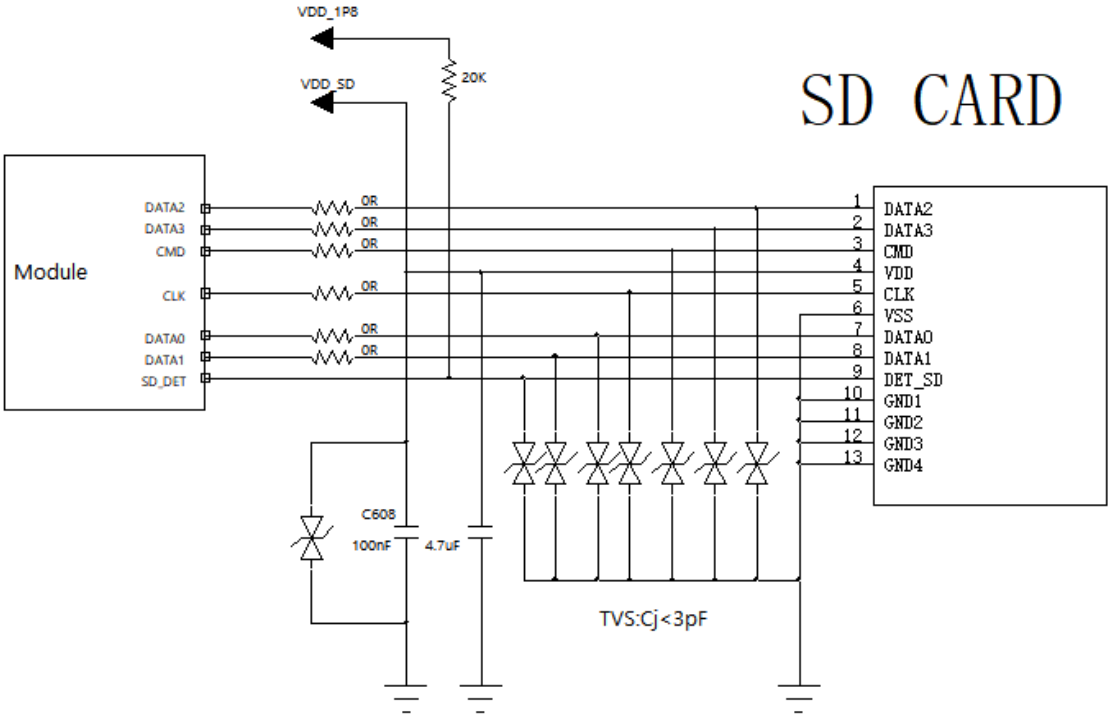


Figure 5-12 SD card reference circuit design

Please follow the following principles for SD card circuit design:

- SD card power supply VDD_3V voltage range is 2.7V~3.6V, and need to provide at least 800mA current.
- SD card power supply needs to be provided from outside the module; 4.7UF filter capacitance on the power supply is recommended.
- In order to avoid bus jitter, pull-up resistor can be reserved for the SDIO signal; the resistance value ranges from 10~100kΩ, and the recommended value is 100kΩ.
- In order to adjust the signal quality, you can reserve 0Ω resistor in series for the SDIO signal, and you can reserve the capacitor bit if the space is allowed, and the default is not posted. Resistors and capacitors need to be placed close to the module side when arranging.
- In order to ensure good ESD performance, it is recommended to add TVS tubes to the SD card pins.

- SDIO bus load capacitance needs to be less than 40pF; TVS tube equivalent capacitance on signal line should be less than 3pF.
- SDIO signals need stereo packet ground with impedance controlled at 50Ω ±10%.
- Other sensitive signals such as RF and analog signals need to be kept away from the SDIO signal, while the SDIO signal also needs to be kept away from noise signals such as clock and DCDC.
- SDC_CLK and SDC_DATA[0:3]/SDC_CMD need to be processed with equal length (the difference is less than 7.62mm), and the total length needs to be less than 101.6mm; the internal alignment of the module needs to be taken into consideration, so the length of the external alignment needs to be less than 17.272mm.
- Spacing between SDIO signals and other signals should be more than 2 times the line width.
- SD card detect pin needs to use GPIO port with interrupt function.
- Module internal alignment:

Pin	CMD	CLK	D0	D1	D2	D3
Alignment Length (mm)	79.263	75.252	84.257	83.617	81.677	77.045

5.8 SPI Interface

The module provides 3 sets of SPI interfaces with a maximum clock frequency of 52MHz.

Table 5-12 SPI interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
SPI for MCU								
C23	MCU_SPI_MISO	SPI data signal NAD input/slave output	-	PD	DI	1.8V	-	Only the master mode is supported.
C24	MCU_SPI_MOSI	SPI data signal NAD output/slave input	-	PD	DO	1.8V	-	
C7	MCU_SPI_CLK	SPI clock signal	-	PD	DO	1.8V	-	
C8	MCU_SPI_CSB	SPI chip select signal	-	PD	DO	1.8V	-	
SPI for V2X								
C49	V2X_SPI_MISO	SPI data signal NAD input/slave output	-	PD	DI	1.8V	-	Master-slave mode is supported.
C50	V2X_SPI_MOSI	SPI data signal NAD output/slave input	-	PD	DO	1.8V	-	
C37	V2X_SPI_CLK	SPI clock signal	-	PD	DIO	1.8V	-	
C38	V2X_SPI_CSB	SPI chip select signal	-	PD	DIO	1.8V	-	
SPI for Ext.HSM								
C42	HSM_SPI_CLK	SPI clock signal	-	PD	DO	1.8V	-	Only the master mode is supported.
C43	HSM_SPI_MI	SPI master device input signal	-	PD	DI	1.8V	-	
C54	HSM_SPI_MO	SPI master device output signal	-	PD	DO	1.8V	-	

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
C55	HSM_SPI_CSB	SPI chip select signal	-	PD	DO	1.8V	-	

Warning

1. The SPI interface level of the module is 1.8V. If the system level of the customer host is 3.3V or other, it is necessary to add a level shifter that supports 52MHz in the SPI connection between the module and the host.

5.9 RGMII Interface

The module provides 1 set of RGMII interface with embedded Ethernet MAC and two-wire management interface, which only supports 1.8V interface PHY chip, and VIO18_1_PMU is recommended for PHY chip interface power control.

Table 5-13 RGMII interface pin definition

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
RGMII								
A43	RGMII_LDO1_EN	RGMII 1.8V power enable signal	Y	PD	DIO	1.8V	-	Configurable as GPIO
A42	RGMII_LDO2_EN	RGMII 3.3V power enable signal	Y	PD	DIO	1.8V	-	Configurable as GPIO
A17	RGMII_RESET_N	RGMII reset signal	Y	PD	DO	1.8V	-	-
A41	RGMII_INT_N	RGMII interrupt signal	Y	PD	DI	1.8V	-	-
A45	RGMII_MDIO	RGMII management data communication signal	Y	PD	DIO	1.8V	-	-
A44	RGMII_MDC	RGMII management data signal clock	Y	PD	DO	1.8V	-	-
A11	RGMII_CTL_TX	RGMII transmit control signal	Y	PD	DO	1.8V	-	-
A12	RGMII_CK_TX	RGMII transmit signal clock	Y	PD	DO	1.8V	-	-
A13	RGMII_TX_0	RGMII transmit data bit 0	Y	PD	DO	1.8V	-	-
A14	RGMII_TX_1	RGMII transmit data bit 1	Y	PD	DO	1.8V	-	-
A15	RGMII_TX_2	RGMII transmit data bit 2	Y	PD	DO	1.8V	-	-
A16	RGMII_TX_3	RGMII transmit data bit 3	Y	PD	DO	1.8V	-	-
A27	RGMII_CTL_RX	RGMII receive control signal	Y	PD	DI	1.8V	-	-
A28	RGMII_CK_RX	RGMII receive signal clock	Y	PD	DI	1.8V	-	-
A29	RGMII_RX_0	RGMII receive data bit 0	Y	PD	DI	1.8V	-	-
A30	RGMII_RX_1	RGMII receive data bit 1	Y	PD	DI	1.8V	-	-
A31	RGMII_RX_2	RGMII receive data bit 2	Y	PD	DI	1.8V	-	-

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
A32	RGMII_RX_3	RGMII receive data bit 3	Y	PD	DI	1.8V	-	-

The module RGMII interface complies with the following standards:

- Conforms to IEEE802.3 standards.
- Supports 10M/100M/1000M operating modes.
- The management interface supports 1.8V only.
- Supports VLAN tagging.
- Supports IEEE 1588 and PTP protocols.
- Can be connected to an external Ethernet PHY chip.

Please refer to the following description for RGMII signal design principles:

- RGMII data and control signals need to be kept away from sensitive signals such as RF and analog signals, as well as noise signals such as clocks and DC-DC.
- RGMII data signal impedance is controlled at 50Ω ±10% and the complete reference ground plane is guaranteed.
- RGMII signal line load capacitance should be less than 15pF.
- The power supply alignment width should be greater than 0.21mm, and the alignment length from the power supply pin to the decoupling capacitor should be less than 5.08mm.
- RGMII interface has two groups of high-speed signals, TX and RX. 6 signal lines in each group, TX_CLK/RX_CLK signal alignment needs to be wrapped separately to the ground; the difference in length of the alignment within the group is controlled at ≤ 2.5mm, and the signal spacing is wired according to the 1W/1W principle, refer to the following:

- RGMII signal alignment total length control within 4400mil.
- RGMII signal alignment over the number of holes is best not more than 1.

5.10 SGMII Interface

The module provides 2 sets of SGMII interfaces with embedded Ethernet MAC and two-wire management interfaces, and only supports 1.8V interface PHY chip, and VIO18_1_PMU is recommended for PHY chip interface power control.

Table 5-14 SGMII interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
SGMII								
B52	SGMII_1_RXN	SGMII_1 receives differential signal -	-	-	AI	1.2V	-	If not used, the RX needs

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
								to be grounded.
B53	SGMII_1_RXP	SGMII_1 receive differential signal +	-	-	AI	1.2V	-	If not used, the RX needs to be grounded.
B62	SGMII_1_TXN	SGMII_1 transmits differential signal -	-	-	AO	1.2V	-	-
B63	SGMII_1_TXP	SGMII_1 transmits differential signal +	-	-	AO	1.2V	-	-
B60	GBE1_RST	GBE1 reset signal	-	PD	DO	1.8V	-	-
B61	GBE1_INT	GBE1 interrupt signal	-	PD	DI	1.8V	-	-
C59	SGMII_MDIO	Management data communication signal	-	PD	DIO	1.8V	-	-
C60	SGMII_MDC	Management data signal clock	-	PD	DO	1.8V	-	-
C61	GBE0_RST	GBE0 reset signal	-	PD	DO	1.8V	-	-
B59	GBE0_INT	GBE0 interrupt signal	-	PD	DI	1.8V	-	-
C62	SGMII_0_TXP	SGMII_0 transmit differential signal +	-	-	AO	1.2V	-	-
C63	SGMII_0_TXN	SGMII_0 transmits differential signal -	-	-	AO	1.2V	-	-
C52	SGMII_0_RXP	SGMII_0 receive differential signal +	-	-	AI	1.2V	-	If not used, the RX needs to be grounded.
C53	SGMII_0_RXN	SGMII_0 receives differential signal -	-	-	AI	1.2V	-	If not used, the RX needs to be grounded.

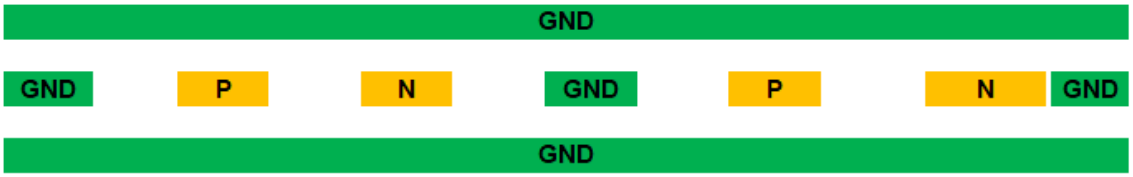
The module SGMII interface complies with the following standards:

- Conforms to IEEE802.3 standards.
- Supports 10 Mbps /100 Mbps /1000 Mbps /2500 Mbps transmission rates in full-duplex mode.
- Supports 10 Mbps /100 Mbps transmission rates in half-duplex mode.
- The management interface supports 1.8V only.
- Can be connected to an external Ethernet PHY.

Please refer to the following description for SGMII signal design principles:

- It is recommended that RGMII and SGMII_0 be used together; when SGMII_1 is not used, the RX signal needs to be grounded, and the other signals can be left hanging.
- SGMII data and control signals need to be kept away from sensitive signals such as RF and analog signals, as well as noisy signals such as clock and DCDC.
- SGMII data signal impedance is controlled at 100Ω±10% and complete reference ground plane is guaranteed.
- It is recommended to add a ground line isolation in the middle of the MDIO and MDC alignments to prevent crosstalk.

- SGMII signals are differential signals, the length difference of the alignment within the differential pair should be controlled at ≤0.127mm; the differential pair alignment should be wrapped with a good ground to shield other signals from interfering, as shown below:



- SGMII_0 signal line alignment length to be controlled within 4050mil; SGMII_1 signal alignment total length to be controlled within 5700mil.
- SGMII signal alignment over the number of holes is best not more than 1.

5.11 PCIe Interface

The module provides a set of 2Lane PCIe interfaces.

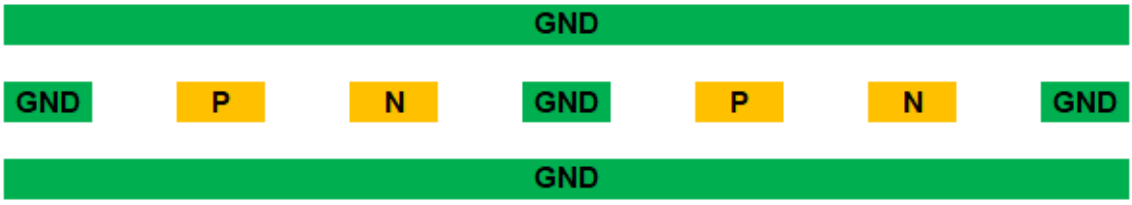
Table 5-15 PCIe interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
PCIe								
B35	PCIE_CLKREQ	PCIe clock request signal	Y	PU	DI	1.8V	-	-
B7	PCIE_WAKE_N	PCIe wake-up signal	Y	PU	DO	1.8V	-	-
B6	PCIE_RESET	PCIe reset signal	Y	PU	DO	1.8V	-	-
B3	PCIE_CLK_P	PCIe differential clock signal +	-	-	AIO	1.2V	-	1. 100±10% impedance control. 2. 50Ω±1% (external pull-down resistor)
B20	PCIE_CLK_M	PCIe differential clock signal -	-	-	AIO	1.2V	-	
B4	PCIE_TX0_P	PCIe differential transmit signal 0+	-	-	AO	1.2V	-	85±10% impedance control.
B21	PCIE_TX0_M	PCIe differential transmit signal 0-	-	-	AO	1.2V	-	
B5	PCIE_TX1_P	PCIe differential transmit signal 1+	-	-	AO	1.2V	-	
B22	PCIE_TX1_M	PCIe differential transmit signal 1-	-	-	AO	1.2V	-	
B2	PCIE_RX0_P	PCIe differential receive signal 0+	-	-	AI	1.2V	-	1. 85±10% impedance control. 2. If not used, grounding treatment.
B19	PCIE_RX0_M	PCIe differential receive signal 0-	-	-	AI	1.2V	-	
B1	PCIE_RX1_P	PCIe differential receive signal 1+	-	-	AI	1.2V	-	

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
PCIe								
B18	PCIE_RX1_M	PCIe differential receive signal 1-	-	-	AI	1.2V	-	

The module supports PCIe GEN 3.0x2 lanes, PCIe signals are differential, design requirements:

- The Gen3 rate, TX differential signal on the coupling capacitor recommended capacitance value of 220nF, placed close to the transmitter.
- The CLK differential impedance is controlled at 100Ω±10%; TX, RX differential impedance is controlled at 85Ω±10%.
- The difference in the length of the differential pair alignment should be controlled at ≤ 0.127mm, and the total length of the signal alignment should be controlled at ≤ 8800mil.
- The alignment should be wrapped with a good ground, as shown below:



5.12 I²C Interface

The module provides 2 sets of I²C interfaces.

Table 5-16 I²C interface pin definitions

Pin	Pin Name	Function	Wakeup	Status	Type	Power Domain	Multiplexing	NOTE
I²C_0 for Sensor								
C35	IMU_I²C0_SDA	I²C0 data signal	-	PU	DIO	1.8V	-	-
C36	IMU_I²C0_SCL	I²C0 clock signal	-	PU	DIO	1.8V	-	-
I²C_1 for Codec								
C47	CDC_I²C1_SDA	I²C1 data signal	-	PU	DIO	1.8V	-	-
C48	CDC_I²C1_SCL	I²C1 clock signal	-	PU	DIO	1.8V	-	-

The features are as follows:

- Supports master device mode operation.
- Supports standard/fast/high speed mode.
- Software default configuration 1K pull-up resistor.

6 Electrical Characteristics and Reliability

6.1 Recommended Parameters

Table 6-1 recommended parameters

Parameter	Minimum	Nominal	Maximum	Unit	Remarks
VPH_IN	3.4	3.8	4.2	V	-
VIL	-0.3	0	0.63	V	-
VIH	1.17	1.8	2.1	V	-
VOL	0	-	0.45	V	-
VOH	1.35	-	1.8	V	-
Operating Temperature	-40	25	85	℃	-
Extended Temperature	-40	25	95	℃	-
Storage Temperature	-40	25	105	℃	-

6.2 RF Transmit Power

The transmit power of AN758-NA-H880 series modules in each frequency band is shown in the following table:

Table 6-2 AN758-NA-H880 module RF transmit power

Model	Band	3GPP Requirements	Max Power Typ.	Unit	Remarks
GSM	GSM850	33+2/-2	33	dBm	--
	GSM900	33+2/-2	33	dBm	--
	DCS1800	30+2/-2	30	dBm	--
	PCS1900	30+1/-2	30	dBm	--
WCDMA	Band 1	24+1.7/-3.7	24	dBm	--
	Band 2	24+1.7/-3.7	24	dBm	--
	Band 4	24+1.7/-3.7	24	dBm	--
	Band 5	24+1.7/-3.7	24	dBm	--
LTE FDD	Band 1	23±2.7	24	dBm	--
	Band 2	23±2.7	24	dBm	--
	Band 3	23±2.7	24	dBm	--
	Band 4	23±2.7	24	dBm	--
	Band 5	23±2.7	24	dBm	--
	Band 7	23±2.7	24	dBm	--
	Band 12	23±2.7	24	dBm	--
	Band 13	23±2.7	24	dBm	--
	Band 14	23±2.7	24	dBm	--
	Band 17	23±2.7	24	dBm	--

Model	Band	3GPP Requirements	Max Power Typ.	Unit	Remarks
	Band 25	23±2.7	24	dBm	--
	Band 26	23±2.7	24	dBm	--
	Band 28	23±2.7	24	dBm	--
	Band 66	23±2.7	24	dBm	--
	Band 71	23±2.7	24	dBm	--
LTE TDD	Band 38	23±2.7	24	dBm	--
	Band 40	23±2.7	24	dBm	--
	Band 41	23±2.7	24	dBm	--
	Band 48	18+1/-3	18	dBm	--
5G NR	n1	23±2	24	dBm	--
	n2	23±2	24	dBm	--
	n3	23±2	24	dBm	--
	n5	23±2	24	dBm	--
	n7	23±2	24	dBm	--
	n12	23±2	24	dBm	--
	n14	23±2	24	dBm	--
	n25	23±2	24	dBm	--
	n28	23±2	24	dBm	--
	n38	23±2	24	dBm	--
	n40	23±2	24	dBm	--
	n41	26+2 /-3	26	dBm	--
	n48	19.5+1/-3	19.5	dBm	--
	n66	23±2	24	dBm	--
	n71	23±2	24	dBm	--
	n77	25.5+1 /-3	25.5	dBm	--
	n78	25.5+1 /-3	25.5	dBm	--

6.3 Dual-Antenna RX Sensitivity

The sensitivity of each frequency band under dual-antenna of AN758-NA-H880 series module is shown in the following table:

Table 6-3 AN758-NA-H880 module RF reception sensitivity

Model	Band	3GPP Requirements	Rx Sensitivity	Unit	Remarks
			Typ.		
GSM	GSM850	-102	TBD	dBm	--
	GSM900	-102	-111.4	dBm	--

Model	Band	3GPP Requirements	Rx Sensitivity	Unit	Remarks
			Typ.		
	DCS1800	-102	-109.8	dBm	--
	PCS1900	-102	TBD	dBm	--
WCDMA	Band 1	-106.7	-112.8	dBm	--
	Band 2	-104.7	TBD	dBm	--
	Band 4	-106.7	TBD	dBm	--
	Band 5	-104.7	-113.7	dBm	--
LTE FDD(10M)	Band 1	-96.3	-101.6	dBm	10MHz BW
	Band 2	-94.3	TBD	dBm	10MHz BW
	Band 3	-93.3	-101.8	dBm	10MHz BW
	Band 4	-96.3	TBD	dBm	10MHz BW
	Band 5	-94.3	-103.2	dBm	10MHz BW
	Band 7	-94.3	-100.4	dBm	10MHz BW
	Band 12	-93.3	TBD	dBm	10MHz BW
	Band 13	-93.3	TBD	dBm	10MHz BW
	Band 14	-93.3	TBD	dBm	10MHz BW
	Band 17	-93.3	TBD	dBm	10MHz BW
	Band 25	-92.8	TBD	dBm	10MHz BW
	Band 26	-93.8	TBD	dBm	10MHz BW
	Band 28	-94.8	-102.3	dBm	10MHz BW
	Band 29	-93.3	TBD	dBm	10MHz BW
	Band 66	-95.8	TBD	dBm	10MHz BW
	Band 71	-96.5	TBD	dBm	10MHz BW
LTE TDD(10M)	Band 38	-96.3	-101.5	dBm	10MHz BW
	Band 40	-96.3	-101.4	dBm	10MHz BW
	Band 41	-94.3	-101.2	dBm	10MHz BW
	Band 48	-95.0	TBD	dBm	10MHz BW
NR	n1	-93.1	-96.1	dBm	SCS 15KHz 20MHz BW
	n2	-91.1	TBD	dBm	SCS 15KHz 20MHz BW
	n3	-90.1	-99.5	dBm	SCS 15KHz 20MHz BW
	n5	-86.1	-100.2	dBm	SCS 15KHz 20MHz BW
	n7	-91.1	-95.5	dBm	SCS 15KHz 20MHz BW
	n12	-83.3	TBD	dBm	SCS 15KHz 15MHz BW
	n14	-93.1	TBD	dBm	SCS 15KHz 10MHz BW
	n25	-89.6	TBD	dBm	SCS 15KHz 20MHz BW
	n28	-90.1	-101.3	dBm	SCS 15KHz 20MHz BW
	n29	-89.3	TBD	dBm	SCS 15KHz 10MHz BW

Model	Band	3GPP Requirements	Rx Sensitivity	Unit	Remarks
			Typ.		
	n38	-93.3	-100	dBm	SCS 30KHz 20MHz BW
	n40	-86.9	-93.4	dBm	SCS 30KHz 80MHz BW
	n41	-84	-92.3	dBm	SCS 30KHz 100MHz BW
	n48	-84.9	TBD	dBm	SCS 30KHz 100MHz BW
	n66	-92.6	TBD	dBm	SCS 15KHz 20MHz BW
	n71	-84	TBD	dBm	SCS 15KHz 20MHz BW
	n77	-84.4	-92.7	dBm	SCS 30KHz 100MHz BW
	n78	-84.9	-92.7	dBm	SCS 30KHz 100MHz BW

Warning

1. The sensitivity is EAU-H880 data, which is for reference only.

6.4 Four-Antenna RX Sensitivity

The AN758-NA-H880 series modules basically support 4 x 4 MIMO in both the medium and high frequencies.

Table 6-4 AN758-NA-H880 module RF reception sensitivity

Model	Band	3GPP Requirements	Rx Sensitivity	Unit	Remarks
			Typ.		
LTE FDD(10M)	Band 1	-99	-104.8	dBm	10MHz BW
	Band 2	-97	TBD	dBm	10MHz BW
	Band 3	-96	-104.5	dBm	10MHz BW
	Band 4	-99	TBD	dBm	10MHz BW
	Band 7	-97	-101	dBm	10MHz BW
	Band 25	-95.5	TBD	dBm	10MHz BW
	Band 66	-98.5	TBD	dBm	10MHz BW
	Band 71	-97	TBD	dBm	10MHz BW
LTE TDD(10M)	Band 38	-97	-103.9	dBm	10MHz BW
	Band 40	-99	TBD	dBm	10MHz BW
	Band 41	-97	-101.2	dBm	10MHz BW
	Band 48	-97	TBD	dBm	10MHz BW
NR	n1	-95.8	-100.2	dBm	SCS 15KHz 20MHz BW
	n2	-93.8	TBD	dBm	SCS 15KHz 20MHz BW
	n3	-92.8	-100.8	dBm	SCS 15KHz 20MHz BW
	n7	-93.8	-100.6	dBm	SCS 15KHz 20MHz BW
	n38	-96	-101.4	dBm	SCS 30KHz 20MHz BW
	n40	-89.6	TBD	dBm	SCS 30KHz 80MHz BW

Model	Band	3GPP Requirements	Rx Sensitivity	Unit	Remarks
			Typ.		
	n41	-86.8	-94.4	dBm	SCS 30KHz 100MHz BW
	n48	-87.1	TBD	dBm	SCS 30KHz 100MHz BW
	n66	-95.3	TBD	dBm	SCS 15KHz 20MHz BW
	n77	-86.6	-94.9	dBm	SCS 15KHz 100MHz BW
	n78	-87.1	-95.1	dBm	SCS 30KHz 100MHz BW

Warning

1. The sensitivity is NA-H880 data, which is for reference only.

6.5 GNSS and External LNAs

The AN758-NA-H880 series module adopts MTK program inside, GPS/GLONASS/BeiDou/Galileo multiple positioning systems, which can effectively improve the sensitivity of GNSS. Its performance index is shown in the following table:

Table 6-5 GNSS performance indicators and hard test confirmation indicators

Parameter	Description	Typ.	Unit	Remarks
Sensitivity	Position capture	-149	dBm	-
	Position tracking	-163	dBm	-
C/No	-130dBm	42.40	dB-Hz	-
TTFF	Cold start time	33	S	-
	Warm start time	24	S	-
	Hot start time	1.1	S	-
CEP	Static accuracy	1	m	-

Note

1. The test environment is GNSS + LNA, based on GPS 6 stars for testing, LNA gain factor is 16 dB.
2. Active antenna selection requirements: module ANT total gain=Active antenna LNA gain - RF cable loss=14~24dB.
   Module ANT total gain: The reference point is the total LNA gain of the ANT PIN of the module.
   Active antenna LNA gain: GNSS active antenna LNA gain. Customers need to choose the appropriate LNA gain according to the line loss to meet the requirements of 14~24dB.
   RF cable loss: GNSS transmission line + TBOX transmission loss.

6.6 Electrostatic Protection

In the module application, due to the human body static electricity, microelectronics between the charged friction and other static electricity, through a variety of ways to discharge to the module, may cause some damage to the module, so ESD protection should be taken seriously. In the process of research and development, production, assembly and testing, especially in product design, should take ESD protection measures. For example, in the circuit design of the interface and susceptible to electrostatic discharge damage or impact of the point, should increase the anti-static

protection; production should wear anti-static gloves etc..

ESD performance parameters (temperature: 25 ℃, humidity: 45 %) as shown in the table below:

Table 6-6 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
GND	±8	±15	KV
Antenna Interface	±8	±15	KV
USB Interface	±8	±15	KV

7 Structural Specification

7.1 Structural Dimensions

The structural dimensions of the AN758-NA-H880 series modules are shown in the figure:

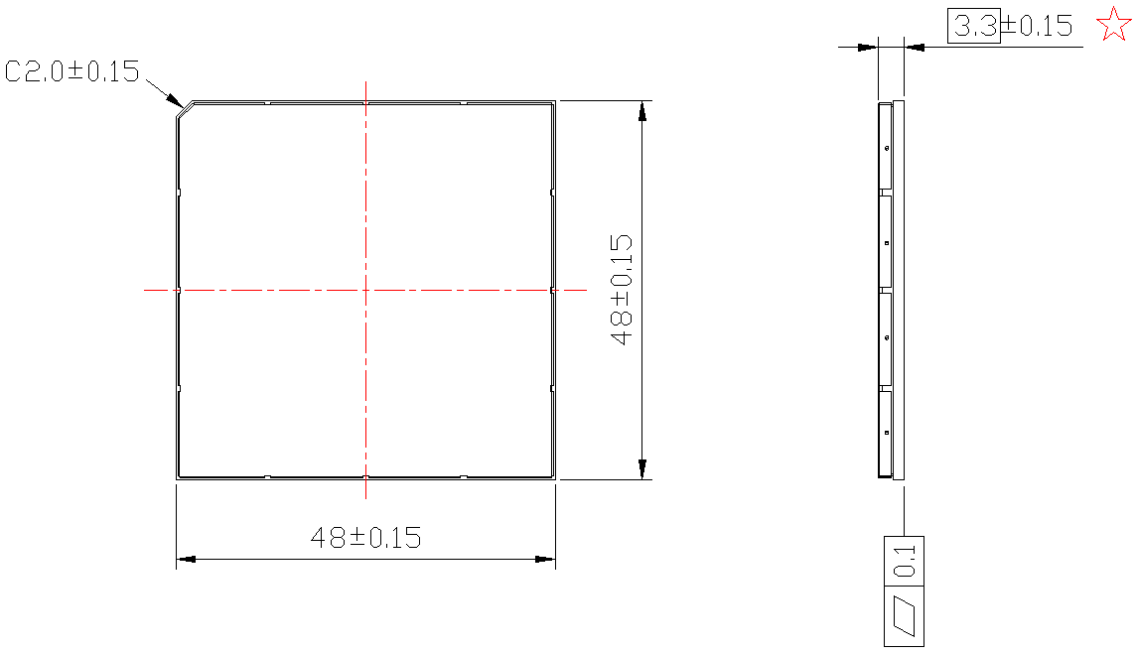


Figure 7-2 structural dimensions

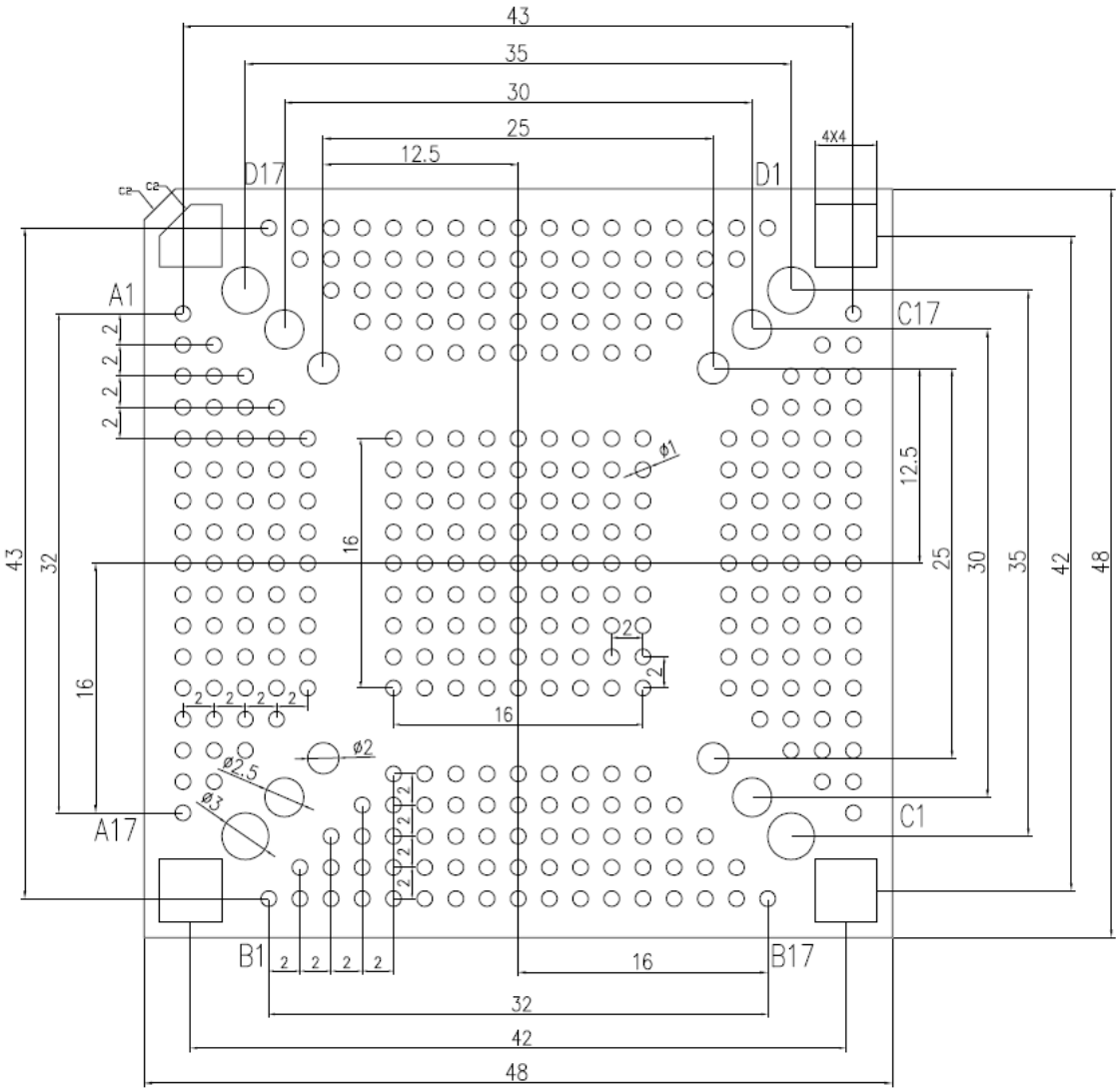


Figure 7-3 front perspective view

Note

1. The tolerance of unmarked dimensions is 0.1mm.

7.2 PCB Pad and Stencil Recommended Designs

Refer to "FIBOCOM_AN758 Series_SMT Application Design Notes".

7.3 SMT Mounting

Refer to "FIBOCOM_AN758 Series_SMT Application Design Notes".

7.4 Packaging and Storage

Refer to " FIBOCOM_AN758&AN758L Series Product Packing Specification".

8 Thermal Design

8.1 Thermal Simulation Design

Refer to "AN758 Thermal Simulation Report".

8.2 Thermal Design

Recommended design:

1）The whole heat dissipation program recommends that the surface of the shielding cover and the shell with a thermally conductive medium material tightly, while the device with a high temperature in the shielding cover increase.

2）Add thermally conductive gel on the surface of the chip (as shown in the figure below).

3）The whole heat dissipation program suggests that the bottom shell and the bottom of the module welding position with a thermally conductive medium material close (as shown in the figure below).

4）Increase the number of holes and thickness of copper cladding in PCB wiring.

5）Increase the area and thickness of PCB copper cladding.

6）High-power chips as far as possible according to the PCB size uniform distribution, while the module away from other heat source devices.

7）Increase the heat dissipation contact area of the source heaters and the pressure between the heat dissipation surfaces.

8）Improve the chip heat source surface and heat conduction surface of the two contact surfaces of the processing accuracy.

9）Appropriately increase the surface area of the shell heat sink teeth.

10）Improve the radiation heat transfer capacity: such as anodizing, surface painting, etc..

11）When the structure is designed to dissipate heat, the direction of the teeth and the direction of the natural convection transfer of heat to the same direction is more conducive to the heat dissipation of the machine.

12）If the cost allows, you can also consider increasing the TEC thermoelectric cooling method.

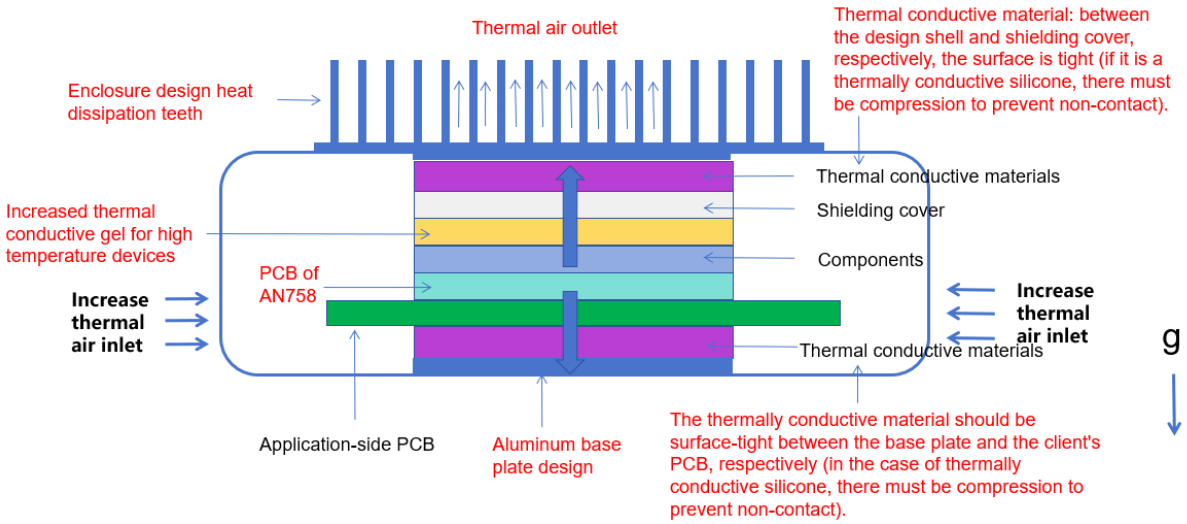


Figure 8-1 recommended design for the thermal solution

Note

1. The above recommendations are thermal design suggestions based on thermal simulation results and are for customer's reference only.
2. Please refer to "AN758 Thermal Simulation Report" for detailed information.

9 Appendix A Abbreviations

Terminology	Description
AR	Augmented Reality
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Downlink
DLCA	Downlink Carrier Aggregation
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock

Terminology	Description
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
VR	Virtual Reality
WCDMA	Wideband Code Division Multiple Access