# nRF52840 Objective Product Specification v0.5.1

**Key features**

- *Bluetooth*® 5, IEEE 802.15.4-2006, 2.4 GHz transceiver
  - -95 dBm sensitivity in 1 Mbps *Bluetooth*® low energy (BLE) mode
  - -103 dBm sensitivity in 125 kbps BLE mode (long range)
  - +8 dBm TX power (down to -20 dBm in 4 dB steps)
  - On-air compatible with nRF52, nRF51, nRF24L and nRF24AP Series
  - Supported data rates:
    - Bluetooth 5: 2 Mbps, 1 Mbps, 500 kbps, 125 kbps
    - IEEE 802.15.4-2006: 250 kbps
    - Proprietary 2.4 GHz: 2 Mbps, 1 Mbps
  - Single-ended antenna output (on-chip balun)
  - 4.9 mA peak current in TX (0 dBm)
  - 4.8 mA peak current in RX
  - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
  - 212 EEMBC CoreMark® score running from flash memory
  - 56 µA/MHz running from flash memory
  - Watchpoint and trace debug modules (DWT, ETM and ITM)
  - Serial wire debug (SWD)
- Flexible power management
  - Supply voltage range 1.7 V to 5.5 V
  - On-chip DC/DC and LDO regulators with automated low current modes
  - Regulated supply for external components from 1.8 V to 3.3 V
  - Automated peripheral power management
  - Fast wake-up using 64 MHz internal oscillator
  - 0.4 µA at 3 V in OFF mode, no RAM retention
  - 1.3 µA at 3 V in ON mode, no RAM retention, wake on RTC
- Memory
  - 1 MB flash/256 kB RAM
- HW accelerated security
  - ARM® TrustZone® Cryptocell 310 cryptographic accelerator
  - 128 bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
- Advanced on-chip interfaces
  - USB 2.0 full speed (12 Mbps) controller
  - QSPI 32 MHz interface
  - High speed 32 MHz SPI
  - Type 2 near field communication (NFC-A) tag with wake-on field
    - Touch-to-pair support
  - Programmable peripheral interconnect (PPI)
  - 48 general purpose I/O pins
  - EasyDMA automated data transfer without CPU processing on peripherals
- Nordic SoftDevice ready and with support for concurrent multi-protocol
- 12-bit, 200 ksps ADC - 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low-power comparator with wake-up from System OFF mode
- Temperature sensor
- 4x 4-channel pulse width modulator (PWM) units with EasyDMA
- Audio peripherals: I2S, digital microphone interface (PDM)
- 5x 32-bit timers with counter mode
- Up to 4x SPI masters/3x SPI slaves with EasyDMA
- Up to 2x I2C compatible 2-wire masters/slaves
- 2x UART (CTS/RTS) with EasyDMA
- Quadrature decoder (QDEC)
- 3x real-time counters (RTC)
- Package variants
  - AQFN73 package, 7 × 7 mm

**Applications**

- Advanced computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Advanced wearables
  - Health/fitness sensor and monitor devices
  - Wireless payment enabled devices
- Internet of things (IoT)
  - Smart home sensors and controllers
  - Industrial IoT sensors and controllers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers

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# 1 Revision history

| Date | Version | Description |
|---|---|---|
| July 2017 | 0.5.1 | The following content is changed in this version:<br>• *Pin assignments* on page 13: Added description for trace pins<br>• *CPU* on page 18: Improved SysTick timer description<br>• *Memory* on page 20: Memory map figure updated<br>• *AHB multilayer* on page 25: Added SPIM3 and updated RAMPRI registers<br>• *EasyDMA* on page 26: Miscellaneous documentation improvements<br>• *UICR — User information configuration registers* on page 44: Improved APPROTECT description and added DEBUGCTRL register<br>• *SPIM — Serial peripheral interface master with EasyDMA* on page 340: Fixed error in mode table and changed the base address of SPIM3<br>• *Debug and trace* on page 62: Added r_pull parameter for CTRL-AP, in addition to miscellaneous documentation improvements<br>• *POWER — Power supply* on page 66:<br>  • Added clarifications for supplying external circuitry<br>  • Improved register descriptions<br>  • Removed deprecated RAMON and RAMONB registers<br>  • Removed pin reset from CTRL-AP feature<br>  • Improved description of POFCON<br>• *CLOCK — Clock control* on page 141:<br>  • Added HFXO debounce functionality<br>  • Changed LFRC accuracy to +- 500 ppm<br>  • Improved description in TRACECONFIG register<br>• *RADIO — 2.4 GHz Radio* on page 249:<br>  • Removed 9 dBm output power option<br>  • Updated TX sequence figure<br>  • Improved TIFS description<br>  • Added PHYEND event<br>  • Added PDUSTAT register<br>  • Removed 250 kbit/s Nordic proprietary mode<br>  • Changed to using term bps instead of sps for data rate in electrical specifications<br>• *SAADC — Successive approximation analog-to-digital converter* on page 418: Updated VDD/5 input specification<br>• *COMP — Comparator* on page 453: REFSEL AREF value changed<br>• *PWM — Pulse width modulation* on page 558: Changed width of DECODER.LOAD field<br>• *PDM — Pulse density modulation interface* on page 499: Fixed error in electrical specification units<br>• *I2S — Inter-IC sound interface* on page 508: PSEL registers PORT field updated<br>• *Reference circuitry* on page 688: Reference schematics updated and erroneous sentence for VDD/VDDH connection removed<br>• *Block diagram* on page 12: Miscellaneous improvements |
| December 2016 | 0.5 | First release |

# 2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in *Recommended operating conditions* on page 17.

## 2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

**Table 1: Defined document names**

| Document name | Description |
|---|---|
| Objective Product Specification (OPS) | Applies to document versions up to 0.7. |
| Preliminary Product Specification (PPS) | This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0. |
| Product Specification (PS) | This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher.<br>This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

## 2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

## 2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

### 2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

## 2.4 Registers

### Table 2: Register Overview

| Register | Offset | Description |
|---|---|---|
| *DUMMY* | 0x514 | Example of a register controlling a dummy feature |

### 2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | D | D | D | D | | | | | | C | C | C | | | | | | | | B | | | | | | | A | A |
| **Reset 0x00050002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | |
| A | RW | FIELD_A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Example of a field with several enumerated values | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | The example feature is disabled | |
| | | | NormalMode | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | The example feature is enabled in normal mode | |
| | | | ExtendedMode | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | The example feature is enabled along with extra functionality | |
| B | RW | FIELD_B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Example of a deprecated field | Deprecated |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | The override feature is disabled | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | The override feature is enabled | |
| C | RW | FIELD_C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Example of a field with a valid range of values | |
| | | | ValidRange | [2..7] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Example of allowed values for this field | |
| D | RW | FIELD_D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Example of a field with no restriction on the values | |

# 3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

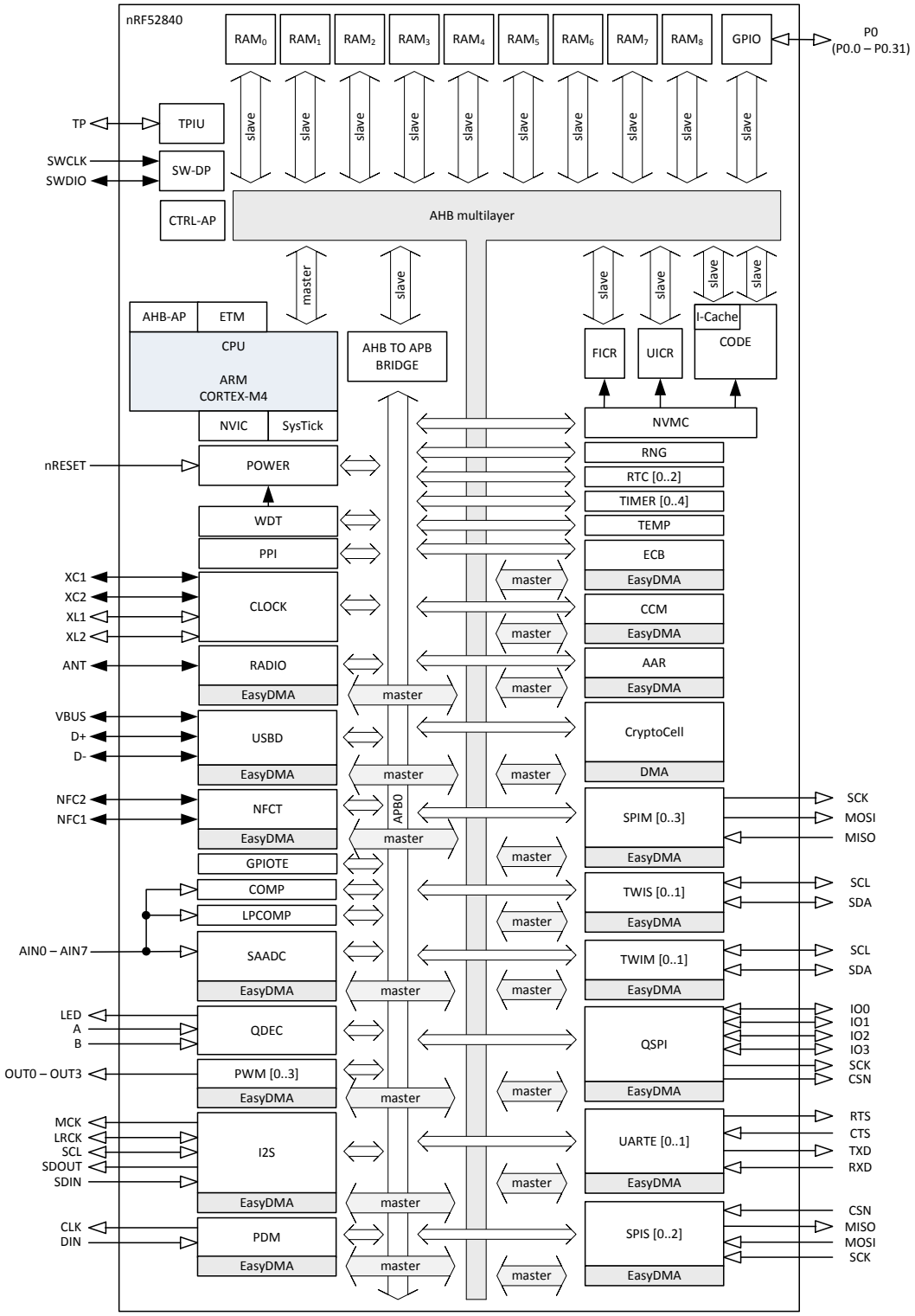



**Figure 1: Block diagram**

# 4 Pin assignments

This section describes the pin assignment and the pin functions.

This device provides flexibility when it comes to routing and configuration of the GPIO pins. However, some pins have recommendations for how the pin should be configured or what it should be used for. See *Table 3: QIAA pin assignments* on page 13 for more information about this.

## 4.1 QIAA pin assignments

This section describes the pin assignment and the pin functions.

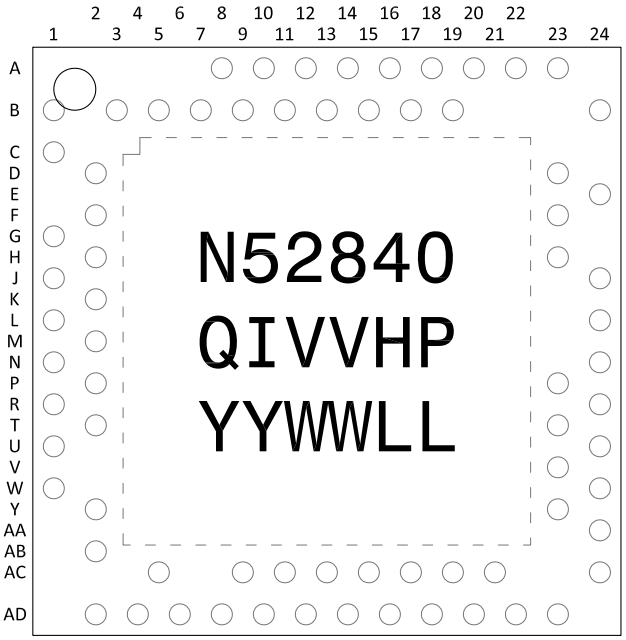



**Figure 2: QIAA pin assignments, top view**

**Table 3: QIAA pin assignments**

| Pin | Name | Function | Description | Recommended usage |
|---|---|---|---|---|
| A8 | P0.31 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN7 | Analog input | Analog input | |
| A10 | P0.29 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN5 | Analog input | Analog input | |
| A12 | P0.02 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN0 | Analog input | Analog input | |
| A14 | P1.15 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| A16 | P1.13 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| A18 | DEC2 | Power | 1.3 V regulator supply decoupling (Radio supply) | |
| A20 | P1.10 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| A22 | VDD | Power | Power supply | |
| A23 | XC2 | Analog input | Connection for 32 MHz crystal. | |
| B1 | VDD | Power | Power supply | |
| B3 | DCC | Power | DC/DC converter output | |

| Pin | Name | Function | Description | Recommended usage |
|---|---|---|---|---|
| B5 | DEC4 | Power | 1.3 V regulator supply decoupling | |
| B7 | VSS | Power | Ground | |
| B9 | P0.30 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN6 | Analog input | Analog input | |
| B11 | P0.28 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN4 | Analog input | Analog input | |
| B13 | P0.03 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | AIN1 | Analog input | Analog input | |
| B15 | P1.14 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| B17 | P1.12 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| B19 | P0.11 | Digital I/O | General purpose I/O pin. | Standard drive, low frequency I/O only. |
| | TRACEDATA2 | Trace data | Trace buffer TRACEDATA[2]. | |
| B24 | XC1 | Analog input | Connection for 32 MHz crystal | |
| C1 | DEC1 | Power | 1.1 V regulator supply decoupling | |
| D2 | P0.00 | Digital I/O | General purpose I/O | |
| | XL1 | Analog input | Connection for 32.768 kHz crystal | |
| D23 | DEC3 | Power | Power supply, decoupling | |
| E24 | DEC6 | Power | 1.3 V regulator supply decoupling (Radio supply) | |
| F2 | P0.01 | Digital I/O | General purpose I/O | |
| | XL2 | Analog input | Connection for 32.768 kHz crystal | |
| F23 | VSS_PA | Power | Ground (Radio supply) | |
| G1 | P0.26 | Digital I/O | General purpose I/O | |
| H2 | P0.27 | Digital I/O | General purpose I/O | |
| H23 | ANT | RF | Single-ended radio antenna connection | See *Reference circuitry* on page 688 for guidelines on how to ensure good RF performance. |
| J1 | P0.04 | Digital I/O | General purpose I/O | |
| | AIN2 | Analog input | Analog input | |
| J24 | P0.10 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | NFC2 | NFC input | NFC antenna connection | |
| K2 | P0.05 | Digital I/O | General purpose I/O | |
| | AIN3 | Analog input | Analog input | |
| L1 | P0.06 | Digital I/O | General purpose I/O | |
| L24 | P0.09 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| | NFC1 | NFC input | NFC antenna connection | |
| M2 | P0.07 | Digital I/O | General purpose I/O pin | |
| | TRACECLK | Trace clock | Trace buffer clock | |
| N1 | P0.08 | Digital I/O | General purpose I/O | |
| N24 | DEC5 | Power | 1.3 V regulator supply decoupling (flash supply) | |
| P2 | P1.08 | Digital I/O | General purpose I/O | |
| P23 | P1.07 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| R1 | P1.09 | Digital I/O | General purpose I/O pin. | |
| | TRACEDATA3 | Trace data | Trace buffer TRACEDATA[3]. | |
| R24 | P1.06 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| T2 | P0.11 | Digital I/O | General purpose I/O | |
| T23 | P1.05 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| U1 | P0.12 | Digital I/O | General purpose I/O pin. | |
| | TRACEDATA1 | Trace data | Trace buffer TRACEDATA[1]. | |

| Pin | Name | Function | Description | Recommended usage |
|---|---|---|---|---|
| U24 | P1.04 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| V23 | P1.03 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| W1 | VDD | Power | Power supply | |
| W24 | P1.02 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| Y2 | VDDH | Power | High voltage power supply | |
| Y23 | P1.01 | Digital I/O | General purpose I/O | Standard drive, low frequency I/O only. |
| AA24 | SWDCLK | Debug | Serial wire debug clock input for debug and programming | |
| AB2 | DCCH | Power | DC/DC converter output | |
| AC5 | DECUSB | Power | Decoupling for USB 3.3 V | |
| AC9 | P0.14 | Digital I/O | General purpose I/O | |
| AC11 | P0.16 | Digital I/O | General purpose I/O | |
| AC13 | P0.18<br>nRESET | Digital I/O | General purpose I/O<br>Configurable as system RESET | QSPI/CSN |
| AC15 | P0.19 | Digital I/O | General purpose I/O | QSPI/SCK |
| AC17 | P0.21 | Digital I/O | General purpose I/O | QSPI |
| AC19 | P0.23 | Digital I/O | General purpose I/O | QSPI |
| AC21 | P0.25 | Digital I/O | General purpose I/O | |
| AC24 | SWDIO | Debug | Debug serial data | |
| AD2 | VBUS | Power | 5 V input for USB 3.3 V regulator | |
| AD4 | D- | Digital I/O | USB D- | USB |
| AD6 | D+ | Digital I/O | USB D+ | USB |
| AD8 | P0.13 | Digital I/O | General purpose I/O | |
| AD10 | P0.15 | Digital I/O | General purpose I/O | |
| AD12 | P0.17 | Digital I/O | General purpose I/O | |
| AD14 | VDD | Power | Power supply | |
| AD16 | P0.20 | Digital I/O | General purpose I/O | |
| AD18 | P0.22 | Digital I/O | General purpose I/O | QSPI |
| AD20 | P0.24 | Digital I/O | General purpose I/O | |
| AD22 | P1.00<br>TRACEDATA0 | Digital I/O<br>Trace data | General purpose I/O pin.<br>Trace buffer TRACEDATA[0].<br>Serial wire output (SWO). | QSPI |
| AD23 | VDD | Power | Flash supply pad | |
| **Bottom of chip** | | | | |
| Die pad | VSS | Power | Ground pad. Exposed die pad must be connected to ground (VSS) for proper device operation. | |

**Important:** For more information on Standard drive, see *GPIO — General purpose input/output* on page 154. Low frequency I/O is signals with a frequency up to 10 kHz.

# 5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

**Table 4: Absolute maximum ratings**

| | Note | Min. | Max. | Unit |
|---|---|---|---|---|
| **Supply voltages** | | | | |
| VDD | | -0.3 | +3.9 | V |
| VDDH | | -0.3 | +5.8 | V |
| VBUS | | -0.3 | +5.8 | V |
| VSS | | | 0 | V |
| **I/O pin voltage** | | | | |
| $V_{I/O}$, VDD ≤3.6 V | | -0.3 | VDD + 0.3 V | V |
| $V_{I/O}$, VDD >3.6 V | | -0.3 | 3.9 V | V |
| **NFC antenna pin current** | | | | |
| $I_{NFC1/2}$ | | | 80 | mA |
| **Radio** | | | | |
| RF input level | | | 10 | dBm |
| **Environmental (AQFN package)** | | | | |
| Storage temperature | | -40 | +125 | °C |
| MSL | Moisture Sensitivity Level | | 2 | |
| ESD HBM | Human Body Model | | 4 | kV |
| ESD $CDM_{QF}$ | Charged Device Model<br>(AQFN73, 7×7 mm package) | | 750 | V |
| **Flash memory** | | | | |
| Endurance | | 10 000 | | Write/erase cycles |
| Retention | | 10 years at 40°C | | |



# 6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

**Table 5: Recommended operating conditions**

| Symbol | Parameter | Notes | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|---|
| VDD | VDD supply voltage, independent of DCDC enable | | 1.7 | 3.0 | 3.6 | V |
| $VDD_{POR}$ | VDD supply voltage needed during power-on reset | | 1.75 | | | V |
| VDDH | VDDH supply voltage, independent of DCDC enable | | 2.5 | 3.7 | 5.5 | V |
| VBUS | VBUS USB supply voltage | | 4.35 | 5 | 5.5 | V |
| $t_{R\_VDD}$ | Supply rise time (0 V to 1.7 V) | | | | 60 | ms |
| $t_{R\_VDDH}$ | Supply rise time (0 V to 3.7 V) | | | | 100 | ms |
| TA | Operating temperature | | -40 | 25 | 85 | °C |

**Important:** The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

# 7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing, including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 29. The section *Electrical specification* on page 18 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

The ARM System Timer (SysTick) is present on nRF52840. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

## 7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow, which in turn will trigger the FPU interrupt.

See *Instantiation* on page 23 for more information about the exceptions triggering the FPU interrupt.

To clear the IRQ (interrupt request) line when an exception has occurred, the relevant exception bit within the floating-point status and control register (FPSCR) needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

## 7.2 Electrical specification

### 7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $W_{FLASH}$ | CPU wait states, running CoreMark from flash, cache disabled | | | 2 | |
| $W_{FLASHCACHE}$ | CPU wait states, running CoreMark from flash, cache enabled | | | 3 | |
| $W_{RAM}$ | CPU wait states, running CoreMark from RAM | | | 0 | |
| $I_{DDFLASHCACHE}$ | CPU current, running CoreMark from flash, cache enabled, LDO | | 6.5 | | mA |
| $I_{DDFLASHCACHEDCDC}$ | CPU current, running CoreMark from flash, cache enabled, DCDC 3V | | 3.6 | | mA |
| $I_{DDFLASH}$ | CPU current, running CoreMark from flash, cache disabled, LDO | | | | mA |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{DDFLASHDCDC}$ | CPU current, running CoreMark from flash, cache disabled, DCDC 3V | | | | mA |
| $I_{DDRAM}$ | CPU current, running CoreMark from RAM, LDO | | | | mA |
| $I_{DDRAMDCDC}$ | CPU current, running CoreMark from RAM, DCDC 3V | | | | mA |
| $I_{DDFLASH/MHz}$ | CPU efficiency, running CoreMark from flash, cache enabled, LDO | | 102 | | µA/MHz |
| $I_{DDFLASHDCDC/MHz}$ | CPU efficiency, running CoreMark from flash, cache enabled, DCDC 3V | | 56 | | µA/MHz |
| $CM_{FLASH}$ | CoreMark, running CoreMark from flash, cache enabled | | 212 | | CoreM |
| $CM_{FLASH/MHz}$ | CoreMark per MHz, running CoreMark from flash, cache enabled | | 3.3 | | CoreM/MHz |
| $CM_{FLASH/mA}$ | CoreMark per mA, running CoreMark from flash, cache enabled, DCDC 3V | | 59 | | CoreM/mA |

## 7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

| Option / Module | Description | Implemented |
|---|---|---|
| Core options | | |
| NVIC | Nested vector interrupt controller | 37 vectors |
| PRIORITIES | Priority bits | 3 |
| WIC | Wakeup interrupt controller | NO |
| Endianness | Memory system endianness | Little endian |
| Bit-banding | Bit banded memory | NO |
| DWT | Data watchpoint and trace | YES |
| SysTick | System tick timer | YES |
| Modules | | |
| MPU | Memory protection unit | YES |
| FPU | Floating-point unit | YES |
| DAP | Debug access port | YES |
| ETM | Embedded trace macrocell | YES |
| ITM | Instrumentation trace macrocell | YES |
| TPIU | Trace port interface unit | YES |
| ETB | Embedded trace buffer | NO |
| FPB | Flash patch and breakpoint unit | YES |
| HTM | AMBA™ AHB trace macrocell | NO |

# 8 Memory

The nRF52840 contains 1 MB of flash and 256 kB of RAM that can be used for code and data storage.

The CPU and the peripherals having EasyDMA can access memory via the AHB multilayer interconnect.

The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 3: Memory layout* on page 20.

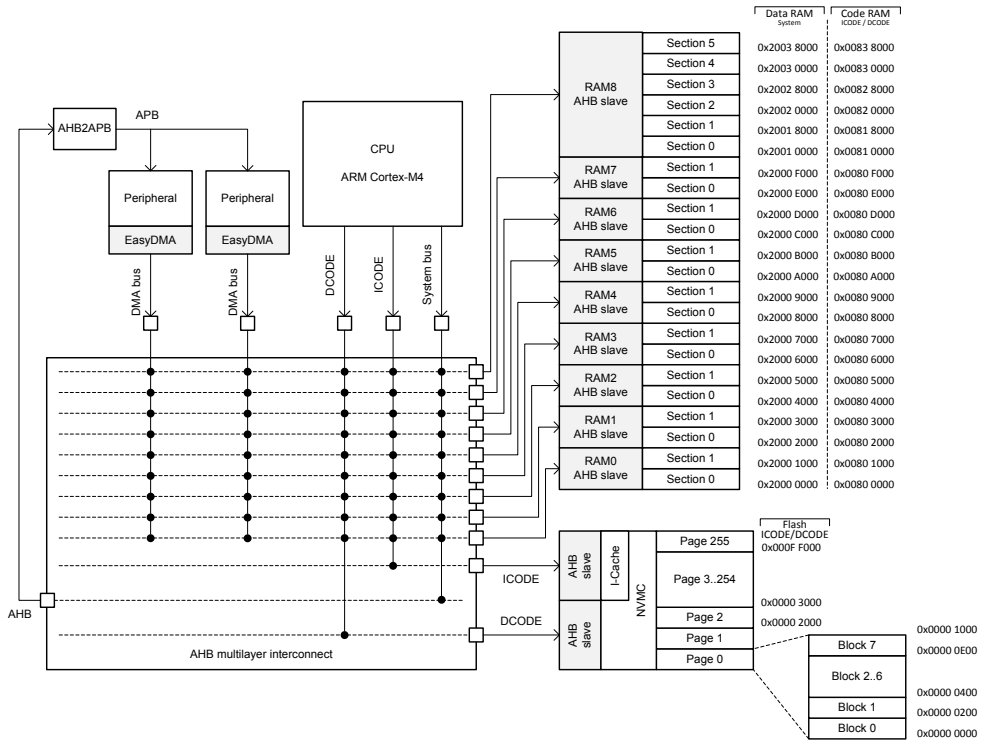



**Figure 3: Memory layout**

See *AHB multilayer* on page 25 and *EasyDMA* on page 26 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

## 8.1 RAM - Random access memory

The RAM interface is divided into 9 RAM AHB slaves.

RAM AHB slave 0-7 is connected to 2x4 kB RAM sections each and RAM AHB slave 8 is connected to 6x32 kB sections, as shown in *Figure 3: Memory layout* on page 20.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 66).

## 8.2 Flash - Non-volatile memory

The flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to flash is managed by the non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 28.

The flash is divided into 256x4 kB pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in *Figure 3: Memory layout* on page 20. Each page is divided into 8 blocks.

## 8.3 Memory map

The complete memory map is shown in *Figure 4: Memory map* on page 22. As described in *Memory* on page 20, Code RAM and the Data RAM are the same physical RAM.

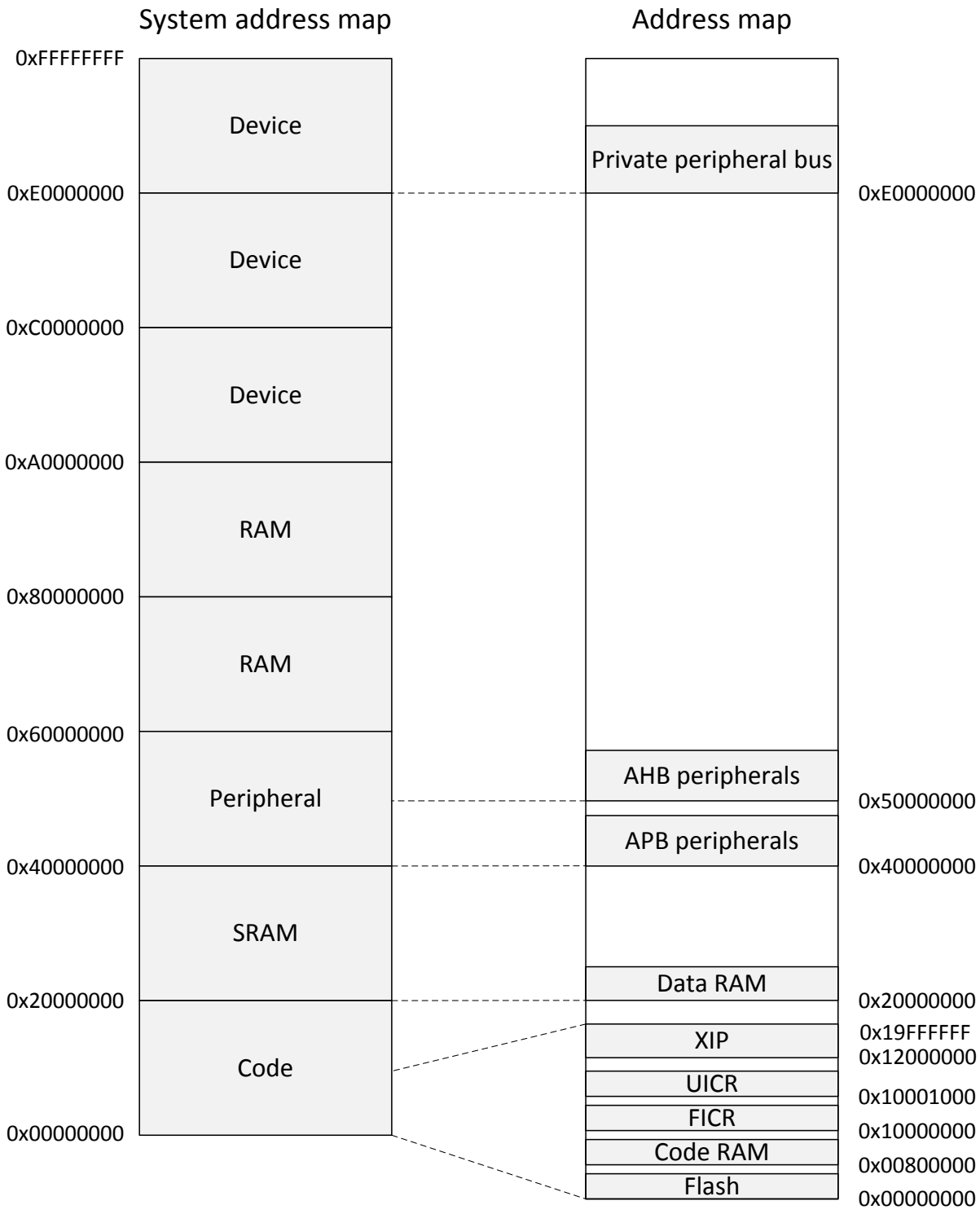



**Figure 4: Memory map**

## 8.4 Instantiation

### Table 6: Instantiation table

| ID | Base Address | Peripheral | Instance | Description | |
|---|---|---|---|---|---|
| 0 | 0x40000000 | CLOCK | CLOCK | Clock control | |
| 0 | 0x40000000 | POWER | POWER | Power control | |
| 1 | 0x40001000 | RADIO | RADIO | 2.4 GHz radio | |
| 2 | 0x40002000 | UARTE | UARTE0 | Universal asynchronous receiver/transmitter with EasyDMA, unit 0 | |
| 2 | 0x40002000 | UART | UART0 | Universal asynchronous receiver/transmitter | Deprecated |
| 3 | 0x40003000 | TWIM | TWIM0 | Two-wire interface master 0 | |
| 3 | 0x40003000 | SPIS | SPIS0 | SPI slave 0 | |
| 3 | 0x40003000 | SPIM | SPIM0 | SPI master 0 | |
| 3 | 0x40003000 | SPI | SPI0 | SPI master 0 | Deprecated |
| 3 | 0x40003000 | TWIS | TWIS0 | Two-wire interface slave 0 | |
| 3 | 0x40003000 | TWI | TWI0 | Two-wire interface master 0 | Deprecated |
| 4 | 0x40004000 | TWIS | TWIS1 | Two-wire interface slave 1 | |
| 4 | 0x40004000 | SPIS | SPIS1 | SPI slave 1 | |
| 4 | 0x40004000 | SPIM | SPIM1 | SPI master 1 | |
| 4 | 0x40004000 | TWI | TWI1 | Two-wire interface master 1 | Deprecated |
| 4 | 0x40004000 | TWIM | TWIM1 | Two-wire interface master 1 | |
| 4 | 0x40004000 | SPI | SPI1 | SPI master 1 | Deprecated |
| 5 | 0x40005000 | NFCT | NFCT | Near field communication tag | |
| 6 | 0x40006000 | GPIOTE | GPIOTE | GPIO tasks and events | |
| 7 | 0x40007000 | SAADC | SAADC | Analog to digital converter | |
| 8 | 0x40008000 | TIMER | TIMER0 | Timer 0 | |
| 9 | 0x40009000 | TIMER | TIMER1 | Timer 1 | |
| 10 | 0x4000A000 | TIMER | TIMER2 | Timer 2 | |
| 11 | 0x4000B000 | RTC | RTC0 | Real-time counter 0 | |
| 12 | 0x4000C000 | TEMP | TEMP | Temperature sensor | |
| 13 | 0x4000D000 | RNG | RNG | Random number generator | |
| 14 | 0x4000E000 | ECB | ECB | AES electronic code book (ECB) mode block encryption | |
| 15 | 0x4000F000 | AAR | AAR | Accelerated address resolver | |
| 15 | 0x4000F000 | CCM | CCM | AES counter with CBC-MAC (CCM) mode block encryption | |
| 16 | 0x40010000 | WDT | WDT | Watchdog timer | |
| 17 | 0x40011000 | RTC | RTC1 | Real-time counter 1 | |
| 18 | 0x40012000 | QDEC | QDEC | Quadrature decoder | |
| 19 | 0x40013000 | LPCOMP | LPCOMP | Low power comparator | |
| 19 | 0x40013000 | COMP | COMP | General purpose comparator | |
| 20 | 0x40014000 | EGU | EGU0 | Event generator unit 0 | |
| 20 | 0x40014000 | SWI | SWI0 | Software interrupt 0 | |
| 21 | 0x40015000 | EGU | EGU1 | Event generator unit 1 | |
| 21 | 0x40015000 | SWI | SWI1 | Software interrupt 1 | |
| 22 | 0x40016000 | EGU | EGU2 | Event generator unit 2 | |
| 22 | 0x40016000 | SWI | SWI2 | Software interrupt 2 | |
| 23 | 0x40017000 | EGU | EGU3 | Event generator unit 3 | |
| 23 | 0x40017000 | SWI | SWI3 | Software interrupt 3 | |
| 24 | 0x40018000 | SWI | SWI4 | Software interrupt 4 | |
| 24 | 0x40018000 | EGU | EGU4 | Event generator unit 4 | |
| 25 | 0x40019000 | SWI | SWI5 | Software interrupt 5 | |
| 25 | 0x40019000 | EGU | EGU5 | Event generator unit 5 | |
| 26 | 0x4001A000 | TIMER | TIMER3 | Timer 3 | |
| 27 | 0x4001B000 | TIMER | TIMER4 | Timer 4 | |
| 28 | 0x4001C000 | PWM | PWM0 | Pulse width modulation unit 0 | |
| 29 | 0x4001D000 | PDM | PDM | Pulse Density modulation (digital microphone) interface | |
| 30 | 0x4001E000 | ACL | ACL | Access control lists | |
| 30 | 0x4001E000 | NVMC | NVMC | Non-volatile memory controller | |

| ID | Base Address | Peripheral | Instance | Description | |
|---|---|---|---|---|---|
| 31 | 0x4001F000 | PPI | PPI | Programmable peripheral interconnect | |
| 32 | 0x40020000 | MWU | MWU | Memory watch unit | |
| 33 | 0x40021000 | PWM | PWM1 | Pulse width modulation unit 1 | |
| 34 | 0x40022000 | PWM | PWM2 | Pulse width modulation unit 2 | |
| 35 | 0x40023000 | SPIM | SPIM2 | SPI master 2 | |
| 35 | 0x40023000 | SPIS | SPIS2 | SPI slave 2 | |
| 35 | 0x40023000 | SPI | SPI2 | SPI master 2 | Deprecated |
| 36 | 0x40024000 | RTC | RTC2 | Real-time counter 2 | |
| 37 | 0x40025000 | I2S | I2S | Inter-IC sound interface | |
| 38 | 0x40026000 | FPU | FPU | FPU interrupt | |
| 39 | 0x40027000 | USBD | USBD | Universal serial bus device | |
| 40 | 0x40028000 | UARTE | UARTE1 | Universal asynchronous receiver/transmitter with EasyDMA, unit 1 | |
| 41 | 0x40029000 | QSPI | QSPI | External memory interface | |
| 45 | 0x4002D000 | PWM | PWM3 | Pulse width modulation unit 3 | |
| 47 | 0x4002F000 | SPIM | SPIM3 | SPI master 3 | |
| 0 | 0x50000000 | GPIO | GPIO | General purpose input and output | Deprecated |
| 0 | 0x50000000 | GPIO | P0 | General purpose input and output, port 0 | |
| 0 | 0x50000300 | GPIO | P1 | General purpose input and output, port 1 | |
| 42 | 0x5002A000 | CRYPTOCELL | CRYPTOCELL | CryptoCell subsystem control interface | |
| N/A | 0x10000000 | FICR | FICR | Factory information configuration | |
| N/A | 0x10001000 | UICR | UICR | User information configuration | |

# 9 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to the slave devices using an interconnection matrix. The bus masters are assigned priorities. Priorities are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted the access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- Bus masters that have the same priority are mutually exclusive, thus cannot be used concurrently.

Below is a list of bus masters in the system and their priorities.

**Table 7: AHB bus masters (listed in priority order, highest to lowest)**

| Bus master name | Description |
|---|---|
| CPU | |
| CTRL-AP | |
| USB | |
| CRYPTOCELL | |
| SPIM1/SPIS1/TWIM1/TWIS1 | Same priority and mutually exclusive |
| RADIO | |
| CCM/ECB/AAR | Same priority and mutually exclusive |
| SAADC | |
| UARTE0 | |
| SPIM0/SPIS0/TWIM0/TWIS0 | Same priority and mutually exclusive |
| SPIM2/SPIS2 | Same priority and mutually exclusive |
| NFCT | |
| I2S | |
| PDM | |
| PWM0 | |
| PWM1 | |
| PWM2 | |
| QSPI | |
| PWM3 | |
| UARTE1 | |
| SPIM3 | |

Defined bus masters are the CPU and the peripherals with implemented EasyDMA, and the available slaves are RAM AHB slaves. How the bus masters and slaves are connected using the interconnection matrix is illustrated in *Memory* on page 20.

# 10 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in *Figure 5: EasyDMA example* on page 26.

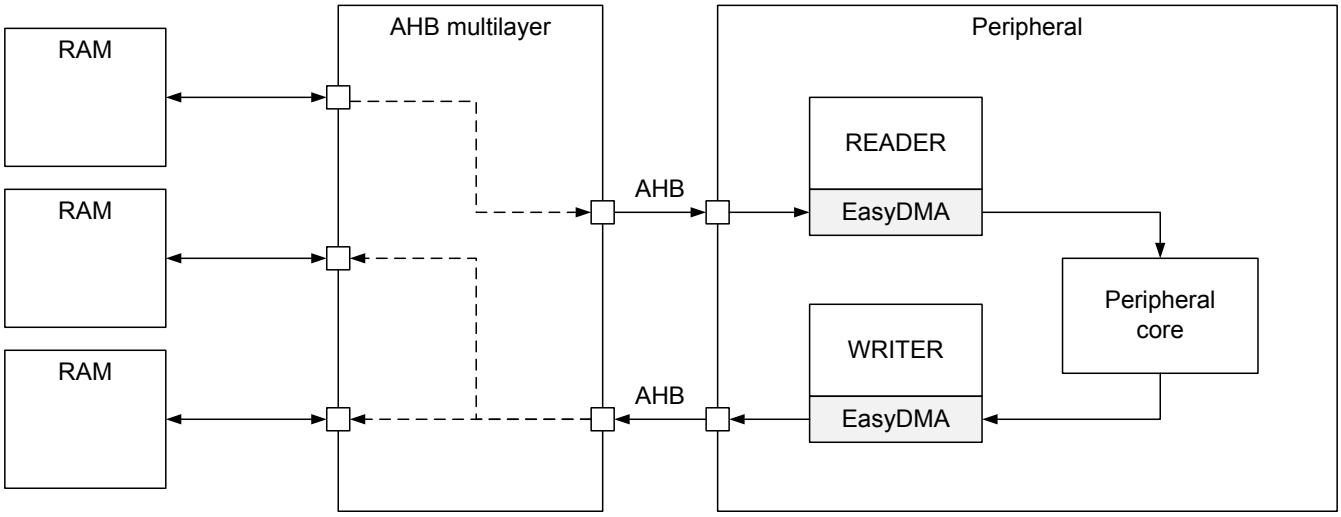



**Figure 5: EasyDMA example**

An EasyDMA channel is usually implemented like illustrated by the code below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE]  __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE]  __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000.
- Process the data.
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005.

The memory layout of these buffers is illustrated in *Figure 6: EasyDMA memory layout* on page 27.

| | | | | |
|---|---|---|---|---|
| 0x20000000 | readerBuffer[0] | readerBuffer[1] | readerBuffer[2] | readerBuffer[3] |
| 0x20000004 | readerBuffer[4] | writerBuffer[0] | writerBuffer[1] | writerBuffer[2] |
| 0x20000008 | writerBuffer[3] | writerBuffer[4] | writerBuffer[5] | |

**Figure 6: EasyDMA memory layout**

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

## 10.1 EasyDMA array list

EasyDMA is able to operate in a mode called array list.

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA array list can be implemented by using the data structure ArrayList_type as illustrated in the code example below:

```
#define BUFFER_SIZE  4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

The data structure only includes a buffer with size equal to the size of READER.MAXCNT register. EasyDMA uses the READER.MAXCNT register to determine when the buffer is full.

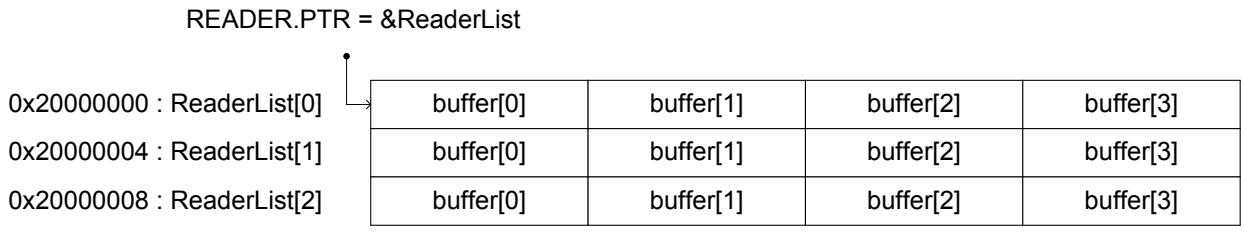



**Figure 7: EasyDMA array list**

# 11 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing the internal flash memory and the UICR.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see *CONFIG* on page 30. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

## 11.1 Writing to flash

When writing is enabled, the flash is written by writing a full 32-bit word to a word-aligned address in the flash.

The NVMC is only able to write '0' to bits in the flash that are erased, that is, set to '1'. It cannot write back a bit to '1'.

As illustrated in *Memory* on page 20, the flash is divided into multiple pages that are further divided into multiple blocks. The same block in the flash can only be written $n_{WRITE}$ number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 20 for block size.

Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits to flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to the flash is specified by $t_{WRITE}$. The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

## 11.2 Erasing a page in flash

When erase is enabled, the flash can be erased page by page using the ERASEPAGE register.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

## 11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written $n_{WRITE}$ number of times before an erase must be performed using *ERASEUICR* or *ERASEALL*.

The time it takes to write a word to the UICR is specified by $t_{WRITE}$. The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the UICR.

## 11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to '1'. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

## 11.5 Erase all

When erase is enabled, the whole flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

## 11.6 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in *Memory map* on page 21 for the location of flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from flash, depends on the processor frequency and is shown in *CPU* on page 18

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

## 11.7 Registers

### Table 8: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4001E000 | NVMC | NVMC | Non-volatile memory controller | |

### Table 9: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| *READY* | 0x400 | Ready flag | |
| *CONFIG* | 0x504 | Configuration register | |
| *ERASEPAGE* | 0x508 | Register for erasing a page in code area | |
| *ERASEPCR1* | 0x508 | Register for erasing a page in code area. Equivalent to ERASEPAGE. | Deprecated |
| *ERASEALL* | 0x50C | Register for erasing all non-volatile user memory | |
| *ERASEPCR0* | 0x510 | Register for erasing a page in code area. Equivalent to ERASEPAGE. | Deprecated |
| *ERASEUICR* | 0x514 | Register for erasing user information configuration registers | |
| *ICACHECNF* | 0x540 | I-code cache configuration register. | |
| *IHIT* | 0x548 | I-code cache hit counter. | |
| *IMISS* | 0x54C | I-code cache miss counter. | |

### 11.7.1 READY

Address offset: 0x400

Ready flag

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Busy | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ready | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 11.7.2 CONFIG

Address offset: 0x504

Configuration register

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | WEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ren | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Wen | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Een | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 11.7.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in code area

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ERASEPAGE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Register for starting erase of a page in code area

The value is the address to the page to be erased. (Addresses of first word in page). Note that the erase must be enabled using CONFIG.WEN before the page can be erased. Attempts to erase pages that are outside the code area may result in undesirable behaviour, e.g. the wrong page may be erased.

## 11.7.4 ERASEPCR1 ( Deprecated )

Address offset: 0x508

Register for erasing a page in code area. Equivalent to ERASEPAGE.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ERASEPCR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Register for erasing a page in code area. Equivalent to ERASEPAGE.

## 11.7.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ERASEALL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Erase all non-volatile memory including UICR registers. Note that the erase must be enabled using CONFIG.WEN before the non-volatile memory can be erased. |
| | | | NoOperation | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No operation |
| | | | Erase | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Start chip erase |

## 11.7.6 ERASEPCR0 ( Deprecated )

Address offset: 0x510

Register for erasing a page in code area. Equivalent to ERASEPAGE.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ERASEPCR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Register for starting erase of a page in code area. Equivalent to ERASEPAGE. |

## 11.7.7 ERASEUICR

Address offset: 0x514

Register for erasing user information configuration registers

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ERASEUICR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Register starting erase of all user information configuration registers. Note that the erase must be enabled using CONFIG.WEN before the UICR can be erased. |
| | | | NoOperation | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No operation |
| | | | Erase | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Start erase of UICR |

## 11.7.8 ICACHECNF

Address offset: 0x540

I-code cache configuration register.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | B | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | CACHEEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Cache enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable cache. Invalidates all cache entries. |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable cache |
| B | RW | CACHEPROFEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Cache profiling enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable cache profiling |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable cache profiling |

## 11.7.9 IHIT

Address offset: 0x548

I-code cache hit counter.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | HITS | | | Number of cache hits |

## 11.7.10 IMISS

Address offset: 0x54C

I-code cache miss counter.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MISSES | | | Number of cache misses |

# 11.8 Electrical specification

## 11.8.1 Flash programming

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $n_{WRITE,BLOCK}$ | Amount of writes allowed in a block between erase | | | 403 | |
| $n_{WRITE}$ | Number of times an address can be written between erase[1] | | | 2 | |
| $t_{WRITE}$ | Time to write one 32-bit word | | | 41[2] | µs |
| $t_{ERASEPAGE}$ | Time to erase one page | | | 85[3] | ms |
| $t_{ERASEALL}$ | Time to erase all flash | | | 169[4] | ms |
| $I_{write}$ | Flash write current | | | 5 | mA |
| $I_{erasepage}$ | Flash erase page current | | | 5 | mA |
| $I_{eraseall}$ | Flash erase all current | | | 5 | mA |

## 11.8.2 Cache size

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $Size_{ICODE}$ | I-Code cache size | | 2048 | | Bytes |

[1] The page must be erased when either of $n_{WRITE,BLOCK}$ or $n_{WRITE}$ is not satisfied
[2] HFXO is used here, this may vary upto +/-5% when HFINT is used
[3] HFXO is used here, this may vary upto +/-5% when HFINT is used
[4] HFXO is used here, this may vary upto +/-5% when HFINT is used

# 12 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

## 12.1 Registers

### Table 10: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x10000000 | FICR | FICR | Factory information configuration | |

### Table 11: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| *CODEPAGESIZE* | 0x010 | Code memory page size | |
| *CODESIZE* | 0x014 | Code memory size | |
| *DEVICEID[0]* | 0x060 | Device identifier | |
| *DEVICEID[1]* | 0x064 | Device identifier | |
| *ER[0]* | 0x080 | Encryption root, word 0 | |
| *ER[1]* | 0x084 | Encryption root, word 1 | |
| *ER[2]* | 0x088 | Encryption root, word 2 | |
| *ER[3]* | 0x08C | Encryption root, word 3 | |
| *IR[0]* | 0x090 | Identity Root, word 0 | |
| *IR[1]* | 0x094 | Identity Root, word 1 | |
| *IR[2]* | 0x098 | Identity Root, word 2 | |
| *IR[3]* | 0x09C | Identity Root, word 3 | |
| *DEVICEADDRTYPE* | 0x0A0 | Device address type | |
| *DEVICEADDR[0]* | 0x0A4 | Device address 0 | |
| *DEVICEADDR[1]* | 0x0A8 | Device address 1 | |
| *INFO.PART* | 0x100 | Part code | |
| *INFO.VARIANT* | 0x104 | Part variant (hardware version and production configuration) | |
| *INFO.PACKAGE* | 0x108 | Package option | |
| *INFO.RAM* | 0x10C | RAM variant | |
| *INFO.FLASH* | 0x110 | Flash variant | |
| | 0x114 | | Reserved |
| | 0x118 | | Reserved |
| | 0x11C | | Reserved |
| *TEMP.A0* | 0x404 | Slope definition A0 | |
| *TEMP.A1* | 0x408 | Slope definition A1 | |
| *TEMP.A2* | 0x40C | Slope definition A2 | |
| *TEMP.A3* | 0x410 | Slope definition A3 | |
| *TEMP.A4* | 0x414 | Slope definition A4 | |
| *TEMP.A5* | 0x418 | Slope definition A5 | |
| *TEMP.B0* | 0x41C | Y-intercept B0 | |
| *TEMP.B1* | 0x420 | Y-intercept B1 | |
| *TEMP.B2* | 0x424 | Y-intercept B2 | |
| *TEMP.B3* | 0x428 | Y-intercept B3 | |
| *TEMP.B4* | 0x42C | Y-intercept B4 | |
| *TEMP.B5* | 0x430 | Y-intercept B5 | |
| *TEMP.T0* | 0x434 | Segment end T0 | |
| *TEMP.T1* | 0x438 | Segment end T1 | |
| *TEMP.T2* | 0x43C | Segment end T2 | |
| *TEMP.T3* | 0x440 | Segment end T3 | |
| *TEMP.T4* | 0x444 | Segment end T4 | |

| Register | Offset | Description |
|---|---|---|
| NFC.TAGHEADER0 | 0x450 | Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| NFC.TAGHEADER1 | 0x454 | Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| NFC.TAGHEADER2 | 0x458 | Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| NFC.TAGHEADER3 | 0x45C | Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |

## 12.1.1 CODEPAGESIZE

Address offset: 0x010

Code memory page size

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | RW | Field | | Value Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | CODEPAGESIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Code memory page size

## 12.1.2 CODESIZE

Address offset: 0x014

Code memory size

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | RW | Field | | Value Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | CODESIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Code memory size in number of pages

Total code space is: CODEPAGESIZE * CODESIZE

## 12.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | RW | Field | | Value Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | DEVICEID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

64 bit unique device identifier

DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

## 12.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | RW | Field | | Value Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | DEVICEID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

64 bit unique device identifier

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 12.1.5 ER[0]

Address offset: 0x080

Encryption root, word 0

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ER | | | Encryption root, word 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 12.1.6 ER[1]

Address offset: 0x084

Encryption root, word 1

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ER | | | Encryption root, word 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 12.1.7 ER[2]

Address offset: 0x088

Encryption root, word 2

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ER | | | Encryption root, word 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 12.1.8 ER[3]

Address offset: 0x08C

Encryption root, word 3

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ER | | | Encryption root, word 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 12.1.9 IR[0]

Address offset: 0x090

Identity Root, word 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | IR | | | | | | | | | | | | | | | | | | | | | | | | Identity Root, word 0 | | | | | | | | | |

## 12.1.10 IR[1]

Address offset: 0x094

Identity Root, word 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | IR | | | | | | | | | | | | | | | | | | | | | | | | Identity Root, word 1 | | | | | | | | | |

## 12.1.11 IR[2]

Address offset: 0x098

Identity Root, word 2

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | IR | | | | | | | | | | | | | | | | | | | | | | | | Identity Root, word 2 | | | | | | | | | |

## 12.1.12 IR[3]

Address offset: 0x09C

Identity Root, word 3

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | IR | | | | | | | | | | | | | | | | | | | | | | | | Identity Root, word 3 | | | | | | | | | |

## 12.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | DEVICEADDRTYPE | | | | | | | | | | | | | | | | | | | | | | | | Device address type | | | | | | | | | |
| | | | Public | 0 | | | | | | | | | | | | | | | | | | | | | | Public address | | | | | | | | | |
| | | | Random | 1 | | | | | | | | | | | | | | | | | | | | | | Random address | | | | | | | | | |

## 12.1.14 DEVICEADDR[0]

Address offset: 0x0A4

Device address 0

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | DEVICEADDR | | | 48 bit device address<br>DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used. |

## 12.1.15 DEVICEADDR[1]

Address offset: 0x0A8

Device address 1

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | DEVICEADDR | | | 48 bit device address<br>DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used. |

## 12.1.16 INFO.PART

Address offset: 0x100

Part code

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00052840** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 0 0 1 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | PART | | | Part code |
| | | | N52840 | 0x52840 | nRF52840 |
| | | | Unspecified | 0xFFFFFFFF | Unspecified |

## 12.1.17 INFO.VARIANT

Address offset: 0x104

Part variant (hardware version and production configuration)

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | VARIANT | | | Part variant (hardware version and production configuration).<br>Encoded as ASCII. |
| | | | AAAA | 0x41414141 | AAAA |
| | | | AAAB | 0x41414142 | AAAB |
| | | | AABA | 0x41414241 | AABA |
| | | | AABB | 0x41414242 | AABB |
| | | | AAB0 | 0x41414230 | AAB0 |
| | | | ABBA | 0x41424241 | ABBA |
| | | | Unspecified | 0xFFFFFFFF | Unspecified |

## 12.1.18 INFO.PACKAGE

Address offset: 0x108

Package option

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | PACKAGE | | | Package option |
| | | | QI | 0x2004 | QIxx - 73-pin aQFN |
| | | | Unspecified | 0xFFFFFFFF | Unspecified |

## 12.1.19 INFO.RAM

Address offset: 0x10C

RAM variant

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | RAM | | | RAM variant |
| | | | K16 | 0x10 | 16 kByte RAM |
| | | | K32 | 0x20 | 32 kByte RAM |
| | | | K64 | 0x40 | 64 kByte RAM |
| | | | K128 | 0x80 | 128 kByte RAM |
| | | | K256 | 0x100 | 256 kByte RAM |
| | | | Unspecified | 0xFFFFFFFF | Unspecified |

## 12.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | FLASH | | | Flash variant |
| | | | K128 | 0x80 | 128 kByte FLASH |
| | | | K256 | 0x100 | 256 kByte FLASH |
| | | | K512 | 0x200 | 512 kByte FLASH |
| | | | K1024 | 0x400 | 1 MByte FLASH |
| | | | K2048 | 0x800 | 2 MByte FLASH |
| | | | Unspecified | 0xFFFFFFFF | Unspecified |

## 12.1.21 TEMP.A0

Address offset: 0x404

Slope definition A0

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0xFFFFF320** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 0 0 1 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | A | | | A (slope definition) register. |

## 12.1.22 TEMP.A1

Address offset: 0x408

Slope definition A1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFF343** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | A | | | A (slope definition) register. |

## 12.1.23 TEMP.A2

Address offset: 0x40C

Slope definition A2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFF35D** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **0** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | A | | | A (slope definition) register. |

## 12.1.24 TEMP.A3

Address offset: 0x410

Slope definition A3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFF400** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | A | | | A (slope definition) register. |

## 12.1.25 TEMP.A4

Address offset: 0x414

Slope definition A4

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFF452** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | A | | | A (slope definition) register. |

## 12.1.26 TEMP.A5

Address offset: 0x418

Slope definition A5

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFF37B** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | A | | | A (slope definition) register. |

## 12.1.27 TEMP.B0

Address offset: 0x41C

Y-intercept B0

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF3FCC** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.28 TEMP.B1

Address offset: 0x420

Y-intercept B1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF3F98** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.29 TEMP.B2

Address offset: 0x424

Y-intercept B2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF3F98** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.30 TEMP.B3

Address offset: 0x428

Y-intercept B3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF0012** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.31 TEMP.B4

Address offset: 0x42C

Y-intercept B4

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF004D** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.32 TEMP.B5

Address offset: 0x430

Y-intercept B5

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFF3E10** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | B | | | B (y-intercept) |

## 12.1.33 TEMP.T0

Address offset: 0x434

Segment end T0

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFE2** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | T | | | T (segment end) register |

## 12.1.34 TEMP.T1

Address offset: 0x438

Segment end T1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFF00** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | T | | | T (segment end) register |

## 12.1.35 TEMP.T2

Address offset: 0x43C

Segment end T2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFF14** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | T | | | T (segment end) register |

## 12.1.36 TEMP.T3

Address offset: 0x440

Segment end T3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFF19** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | T | | | T (segment end) register |

## 12.1.37 TEMP.T4

Address offset: 0x444

Segment end T4

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFF50** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | R | T | | | | | | | | | | | | | | | | | | | | | | | | | | T (segment end) register | | | | | | | |

## 12.1.38 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFF5F** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | R | MFGID | | | | | | | | | | | | | | | | | | | | | | | | | | Default Manufacturer ID: Nordic Semiconductor ASA has ICM 0x5F | | | | | | | |
| B | R | UD1 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 1 | | | | | | | |
| C | R | UD2 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 2 | | | | | | | |
| D | R | UD3 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 3 | | | | | | | |

## 12.1.39 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | R | UD4 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 4 | | | | | | | |
| B | R | UD5 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 5 | | | | | | | |
| C | R | UD6 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 6 | | | | | | | |
| D | R | UD7 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 7 | | | | | | | |

## 12.1.40 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | R | UD8 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 8 | | | | | | | |
| B | R | UD9 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 9 | | | | | | | |
| C | R | UD10 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 10 | | | | | | | |
| D | R | UD11 | | | | | | | | | | | | | | | | | | | | | | | | | | Unique identifier byte 11 | | | | | | | |

## 12.1.41 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | UD12 | | | | | | | | | | Unique identifier byte 12 | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | UD13 | | | | | | | | | | Unique identifier byte 13 | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | UD14 | | | | | | | | | | Unique identifier byte 14 | | | | | | | | | | | | | | | | | | | | | | | |
| D | R | UD15 | | | | | | | | | | Unique identifier byte 15 | | | | | | | | | | | | | | | | | | | | | | | |

# 13 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user-specific settings.

For information on writing UICR registers, see the *NVMC — Non-volatile memory controller* on page 28 and *Memory* on page 20 chapters.

## 13.1 Registers

### Table 12: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x10001000 | UICR | UICR | User information configuration | |

### Table 13: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| | 0x000 | | Reserved |
| | 0x004 | | Reserved |
| | 0x008 | | Reserved |
| | 0x010 | | Reserved |
| *NRFFW[0]* | 0x014 | Reserved for Nordic firmware design | |
| *NRFFW[1]* | 0x018 | Reserved for Nordic firmware design | |
| *NRFFW[2]* | 0x01C | Reserved for Nordic firmware design | |
| *NRFFW[3]* | 0x020 | Reserved for Nordic firmware design | |
| *NRFFW[4]* | 0x024 | Reserved for Nordic firmware design | |
| *NRFFW[5]* | 0x028 | Reserved for Nordic firmware design | |
| *NRFFW[6]* | 0x02C | Reserved for Nordic firmware design | |
| *NRFFW[7]* | 0x030 | Reserved for Nordic firmware design | |
| *NRFFW[8]* | 0x034 | Reserved for Nordic firmware design | |
| *NRFFW[9]* | 0x038 | Reserved for Nordic firmware design | |
| *NRFFW[10]* | 0x03C | Reserved for Nordic firmware design | |
| *NRFFW[11]* | 0x040 | Reserved for Nordic firmware design | |
| *NRFFW[12]* | 0x044 | Reserved for Nordic firmware design | |
| *NRFFW[13]* | 0x048 | Reserved for Nordic firmware design | |
| *NRFFW[14]* | 0x04C | Reserved for Nordic firmware design | |
| *NRFHW[0]* | 0x050 | Reserved for Nordic hardware design | |
| *NRFHW[1]* | 0x054 | Reserved for Nordic hardware design | |
| *NRFHW[2]* | 0x058 | Reserved for Nordic hardware design | |
| *NRFHW[3]* | 0x05C | Reserved for Nordic hardware design | |
| *NRFHW[4]* | 0x060 | Reserved for Nordic hardware design | |
| *NRFHW[5]* | 0x064 | Reserved for Nordic hardware design | |
| *NRFHW[6]* | 0x068 | Reserved for Nordic hardware design | |
| *NRFHW[7]* | 0x06C | Reserved for Nordic hardware design | |
| *NRFHW[8]* | 0x070 | Reserved for Nordic hardware design | |
| *NRFHW[9]* | 0x074 | Reserved for Nordic hardware design | |
| *NRFHW[10]* | 0x078 | Reserved for Nordic hardware design | |
| *NRFHW[11]* | 0x07C | Reserved for Nordic hardware design | |
| *CUSTOMER[0]* | 0x080 | Reserved for customer | |
| *CUSTOMER[1]* | 0x084 | Reserved for customer | |
| *CUSTOMER[2]* | 0x088 | Reserved for customer | |
| *CUSTOMER[3]* | 0x08C | Reserved for customer | |
| *CUSTOMER[4]* | 0x090 | Reserved for customer | |
| *CUSTOMER[5]* | 0x094 | Reserved for customer | |
| *CUSTOMER[6]* | 0x098 | Reserved for customer | |

| Register | Offset | Description |
|---|---|---|
| CUSTOMER[7] | 0x09C | Reserved for customer |
| CUSTOMER[8] | 0x0A0 | Reserved for customer |
| CUSTOMER[9] | 0x0A4 | Reserved for customer |
| CUSTOMER[10] | 0x0A8 | Reserved for customer |
| CUSTOMER[11] | 0x0AC | Reserved for customer |
| CUSTOMER[12] | 0x0B0 | Reserved for customer |
| CUSTOMER[13] | 0x0B4 | Reserved for customer |
| CUSTOMER[14] | 0x0B8 | Reserved for customer |
| CUSTOMER[15] | 0x0BC | Reserved for customer |
| CUSTOMER[16] | 0x0C0 | Reserved for customer |
| CUSTOMER[17] | 0x0C4 | Reserved for customer |
| CUSTOMER[18] | 0x0C8 | Reserved for customer |
| CUSTOMER[19] | 0x0CC | Reserved for customer |
| CUSTOMER[20] | 0x0D0 | Reserved for customer |
| CUSTOMER[21] | 0x0D4 | Reserved for customer |
| CUSTOMER[22] | 0x0D8 | Reserved for customer |
| CUSTOMER[23] | 0x0DC | Reserved for customer |
| CUSTOMER[24] | 0x0E0 | Reserved for customer |
| CUSTOMER[25] | 0x0E4 | Reserved for customer |
| CUSTOMER[26] | 0x0E8 | Reserved for customer |
| CUSTOMER[27] | 0x0EC | Reserved for customer |
| CUSTOMER[28] | 0x0F0 | Reserved for customer |
| CUSTOMER[29] | 0x0F4 | Reserved for customer |
| CUSTOMER[30] | 0x0F8 | Reserved for customer |
| CUSTOMER[31] | 0x0FC | Reserved for customer |
| PSELRESET[0] | 0x200 | Mapping of the nRESET function |
| PSELRESET[1] | 0x204 | Mapping of the nRESET function |
| APPROTECT | 0x208 | Access port protection |
| NFCPINS | 0x20C | Setting of pins dedicated to NFC functionality: NFC antenna or GPIO |
| DEBUGCTRL | 0x210 | Processor debug control |
| EXTSUPPLY | 0x300 | Enable external circuitry to be supplied from VDD pin. Applicable in high voltage mode only. |
| REGOUT0 | 0x304 | GPIO reference voltage / external output supply voltage in high voltage mode |

### 13.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

### 13.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

### 13.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NRFFW | | | Reserved for Nordic firmware design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NRFFW | | | Reserved for Nordic firmware design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NRFFW | | | Reserved for Nordic firmware design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NRFFW | | | Reserved for Nordic firmware design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NRFFW | | | Reserved for Nordic firmware design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

## 13.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

## 13.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

## 13.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

## 13.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

## 13.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

### 13.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

### 13.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFFW | | | Reserved for Nordic firmware design |

### 13.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

## 13.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

## 13.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

## 13.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

## 13.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

## 13.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | NRFHW | | | Reserved for Nordic hardware design |

### 13.1.28 CUSTOMER[0]

Address offset: 0x080

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.29 CUSTOMER[1]

Address offset: 0x084

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.30 CUSTOMER[2]

Address offset: 0x088

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.31 CUSTOMER[3]

Address offset: 0x08C

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.32 CUSTOMER[4]

Address offset: 0x090

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.33 CUSTOMER[5]

Address offset: 0x094

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.34 CUSTOMER[6]

Address offset: 0x098

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.35 CUSTOMER[7]

Address offset: 0x09C

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.36 CUSTOMER[8]

Address offset: 0x0A0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.37 CUSTOMER[9]

Address offset: 0x0A4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.38 CUSTOMER[10]

Address offset: 0x0A8

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.39 CUSTOMER[11]

Address offset: 0x0AC

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.40 CUSTOMER[12]

Address offset: 0x0B0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.41 CUSTOMER[13]

Address offset: 0x0B4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.42 CUSTOMER[14]

Address offset: 0x0B8

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.43 CUSTOMER[15]

Address offset: 0x0BC

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.44 CUSTOMER[16]

Address offset: 0x0C0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.45 CUSTOMER[17]

Address offset: 0x0C4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.46 CUSTOMER[18]

Address offset: 0x0C8

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.47 CUSTOMER[19]

Address offset: 0x0CC

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.48 CUSTOMER[20]

Address offset: 0x0D0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.49 CUSTOMER[21]

Address offset: 0x0D4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.50 CUSTOMER[22]

Address offset: 0x0D8

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.51 CUSTOMER[23]

Address offset: 0x0DC

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.52 CUSTOMER[24]

Address offset: 0x0E0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.53 CUSTOMER[25]

Address offset: 0x0E4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.54 CUSTOMER[26]

Address offset: 0x0E8

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.55 CUSTOMER[27]

Address offset: 0x0EC

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.56 CUSTOMER[28]

Address offset: 0x0F0

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

## 13.1.57 CUSTOMER[29]

Address offset: 0x0F4

Reserved for customer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CUSTOMER | | | Reserved for customer |

### 13.1.58 CUSTOMER[30]

Address offset: 0x0F8

Reserved for customer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CUSTOMER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reserved for customer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 13.1.59 CUSTOMER[31]

Address offset: 0x0FC

Reserved for customer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CUSTOMER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reserved for customer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 13.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they do not, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin number of PORT onto which nRESET is exposed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number onto which nRESET is exposed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 13.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they do not, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin number of PORT onto which nRESET is exposed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number onto which nRESET is exposed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.62 APPROTECT

Address offset: 0x208

Access port protection

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PALL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0xFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 0x00 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PROTECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NFC | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.64 DEBUGCTRL

Address offset: 0x210

Processor debug control

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CPUNIDEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 0xFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0x00 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CPUFPBEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 0xFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0x00 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.65 EXTSUPPLY

Address offset: 0x300

Enable external circuitry to be supplied from VDD pin. Applicable in high voltage mode only.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EXTSUPPLY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 13.1.66 REGOUT0

Address offset: 0x304

GPIO reference voltage / external output supply voltage in high voltage mode

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | VOUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Output voltage from of REG0 regulator stage. The maximum output voltage from this stage is given as VDDH - VEXDIF. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1V8 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1.8 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2V1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 2.1 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2V4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 2.4 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2V7 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 2.7 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3V0 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 3.0 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3V3 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 3.3 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DEFAULT | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Default voltage: 1.8 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 14 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

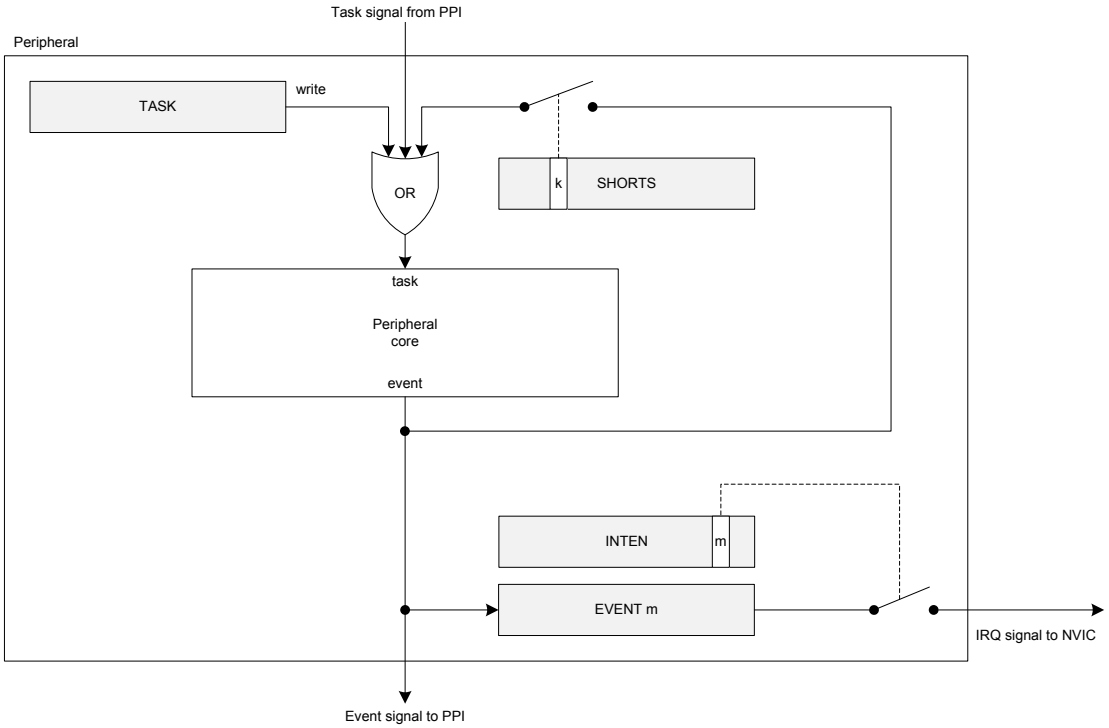



**Figure 8: Tasks, events, shortcuts, and interrupts**

## 14.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 23 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

## 14.2 Peripherals with shared ID

In general (with the exception of ID 0), peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one peripheral at the time on this specific ID.

When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:

- Disable the previously used peripheral.
- Remove any programmable peripheral interconnect (PPI) connections set up for the peripheral that is being disabled.
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- Enable the now configured peripheral.

See *Instantiation* on page 23 to see which peripherals are sharing ID.

## 14.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

## 14.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing `1` to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing `0` to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

**Restriction:** The main register may not be visible and hence not directly accessible in all cases.

## 14.5 Tasks

Tasks are used to trigger actions in a peripheral, for example to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes `1` to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59.

## 14.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral’s event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59. An event register is only cleared when firmware writes `0` to it.

Events can be generated by the peripheral even when the event register is set to `1`.

## 14.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

## 14.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59.

### 14.8.1 Interrupt clearing

When clearing an interrupt by writing `0` to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

> **Important:** To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.

# 15 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

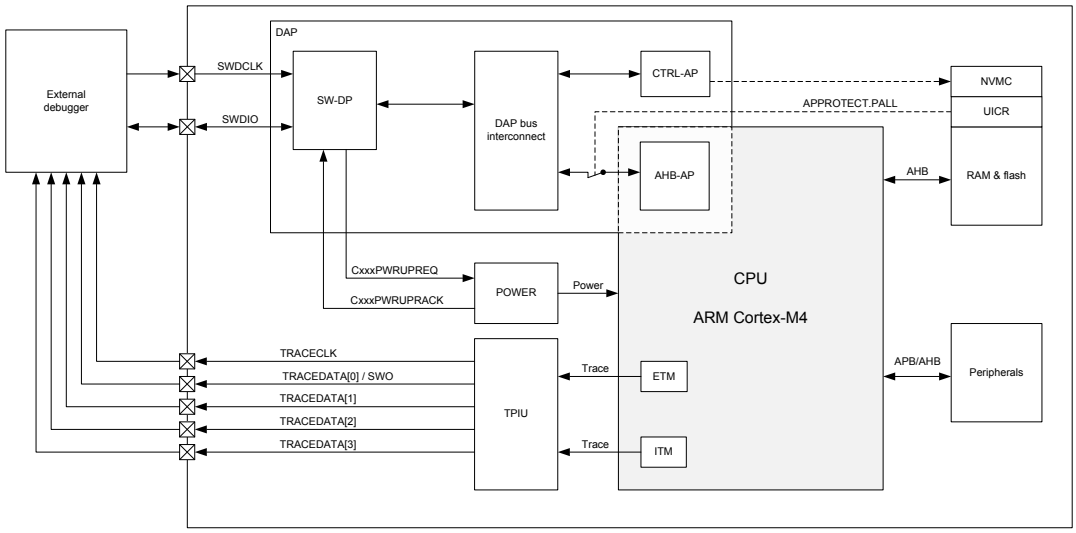



**Figure 9: Overview**

The main features of the debug and trace system are:

- Two-pin serial wire debug (SWD) interface
- Flash patch and breakpoint unit (FPB) supports:
  - Two literal comparators
  - Six instruction comparators
- Data watchpoint and trace unit (DWT)
  - Four comparators
- Instrumentation trace macrocell (ITM)
- Embedded trace macrocell (ETM)
- Trace port interface unit (TPIU)
  - 4-bit parallel trace of ITM and ETM trace data
  - Serial wire output (SWO) trace of ITM data

## 15.1 DAP - Debug access port

An external debugger can access the device via the DAP.

The DAP implements a standard ARM® CoreSight™ SW-DP (serial wire debug port).

The SW-DP implements the SWD (serial wire debug) protocol that is a two-pin serial interface, see SWDCLK and SWDIO in *Debug and trace* on page 62.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom control access port (CTRL-AP). The CTRL-AP is described in more detail in *CTRL-AP - Control access port* on page 63.

**Important:**

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

## 15.2 CTRL-AP - Control access port

The control access port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 57 for more information about enabling access port protection.

This access port enables the following features:

- Soft reset, see *Reset* on page 73 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase flash, UICR, and RAM.

### 15.2.1 Registers

**Table 14: Register Overview**

| Register | Offset | Description |
|---|---|---|
| *RESET* | 0x000 | Soft reset triggered through CTRL-AP |
| *ERASEALL* | 0x004 | Erase all |
| *ERASEALLSTATUS* | 0x008 | Status register for the ERASEALL operation |
| *APPROTECTSTATUS* | 0x00C | Status register for access port protection |
| *IDR* | 0x0FC | CTRL-AP identification register, IDR |

#### RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoReset | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reset | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

#### ERASEALL

Address offset: 0x004

Erase all

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | ERASEALL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoOperation | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Erase | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

#### ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ERASEALLSTATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ready | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Busy | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | APPROTECTSTATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### IDR

Address offset: 0x0FC

CTRL-AP identification register, IDR

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | E | E | E | E | D | D | D | D | C | C | C | C | C | C | B | B | B | B | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x02880000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | APID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | CLASS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDefined | 0x0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | MEMAP | 0x8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | JEP106ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | R | JEP106CONT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | R | REVISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 15.2.2 Electrical specification

### Control access port

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{pull}$ | Internal SWDIO and SWDCLK pull up/down resistance | | 13 | | kΩ |

# 15.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the control access port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 77 will be set.

## 15.4 Real-time debug

The nRF52840 supports real-time debugging.

Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

## 15.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3] and TRACECLK in *Figure 9: Overview* on page 62. In addition to parallel trace, the TPIU supports serial trace via the serial wire output (SWO) trace protocol. Parallel and serial trace cannot be used at the same time.

ETM trace is only supported in parallel trace mode, while ITM trace is supported in both parallel and serial trace modes. For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, and SWO and TRACEDATA[0] use the same GPIO, see *Pin assignments* on page 13 for more information. The speed of the trace pins depends on the drive setting of the GPIOs that the trace pins are multiplexed with. Trace speed is configured in the *TRACECONFIG* on page 149 register.

Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default drive at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user must make sure that these GPIOs' drive is not overwritten by software during the debugging session.

### 15.5.1 Electrical specification

#### Trace port

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{cyc}$ | Clock period, as defined by ARM (See ARM Infocenter, Embedded Trace Macrocell Architecture Specification, Trace Port Physical Interface, Timing specifications) | 62.5 | | 500 | ns |

# 16 POWER — Power supply

The power supply consists of a number of LDO and DC/DC regulators that are utilized to maximize the system's power efficiency.

This device has the following power supply features:

- On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- Supervisor HW to manage power-on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- External circuitry supply
- Separate USB supply

## 16.1 Main supply

The main supply voltage is connected to **VDD**/**VDDH** pins. The system will enter one of two supply voltage modes, normal or high voltage mode, depending on how the supply voltage is connected to these pins.

Normal voltage mode is entered when the supply voltage is connected to both the **VDD** and **VDDH** pins (so that **VDD** equals **VDDH**).

High voltage mode is entered when the supply voltage is only connected to the **VDDH** pin and the **VDD** pin is not connected to any voltage supply.

The *MAINREGSTATUS* on page 81 register can be used for reading out the current supply voltage mode.

For the supply voltage range of the two supply voltage modes, see *Regulator operating conditions* on page 138.

### 16.1.1 Main voltage regulators

The system contains two main supply regulator stages, REG0 and REG1.

Each of the regulator stages have the following regulator type options:

- Low-dropout regulator (LDO)
- Buck regulator (DC/DC)

In normal voltage mode, only the REG1 regulator stage is used and the REG0 stage is automatically disabled. In high voltage mode, both regulator stages (REG0 and REG1) are used. The output voltage of REG0 can be configured in register *REGOUT0* on page 58 listed in *UICR — User information configuration registers* on page 44. This output voltage is connected to **VDD** and is the input voltage to REG1.

By default, the LDO regulators are enabled and the DC/DC regulators are disabled. Registers *DCDCEN0* on page 81 and *DCDCEN* on page 80 are used to independently enable the DC/DC regulators for the two stages (REG0 and REG1 respectively).

When a DC/DC converter is enabled, the LDO for the corresponding regulator stage will be disabled. External LC filters must be connected for each of the DC/DC regulators being used. The advantage of using a DC/DC regulator is that the overall power consumption is normally reduced as the efficiency of such a regulator is higher than that of a LDO. The efficiency benefit of using a DC/DC regulator becomes particularly prominent at high dropout voltage (between the input voltage and the output voltage). The efficiency of internal regulators vary with the supply voltage and the current drawn from the regulators.

> **Important:** Do not enable DCDC regulator without an external LC filter being connected as this will inhibit device operation, including debug access, until an LC filter is connected.

### 16.1.2 GPIO levels

The GPIO high reference voltage always equals the level on the **VDD** pin.

In normal voltage mode, the GPIO high level equals the voltage supplied to the **VDD** pin, and in high voltage mode it equals the level specified in the register *REGOUT0* on page 58 listed in *UICR — User information configuration registers* on page 44.

### 16.1.3 External circuitry supply

In high voltage mode, the output from REG0 can be used to supply external circuitry from the **VDD** pin.

Before any current can be drawn from the **VDD** pin, this feature must be enabled in the *EXTSUPPLY* on page 57 UICR register.

The VDD output voltage is configured in the *REGOUT0* on page 58 UICR register.

The supported output voltage range depends on the supply voltage provided on the **VDDH** pin. Minimum difference between voltage supplied on the **VDDH** pin and the voltage output on the **VDD** pin is defined by $V_{EXDIF}$ parameter in *Regulator operating conditions* on page 138.

Supplying external circuitry is allowed in both System OFF and System ON mode.

> **Important:** When in System OFF mode, 1 mA is the maximum current draw allowed by external circuitry (as defined by the $I_{EX,OFF}$ parameter in *Regulator operating conditions* on page 138).

### 16.1.4 Regulator configuration examples

The voltage regulators can be configured in several ways, depending on the selected supply voltage mode (normal/high) and the regulator type option (LDO or DC/DC).

Four configuration examples are illustrated in images below.

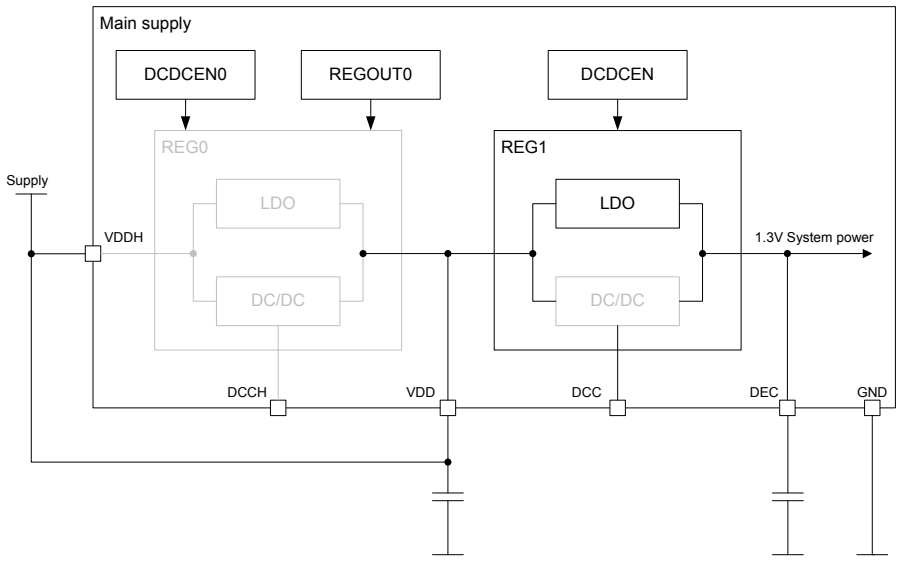



**Figure 10: Normal voltage mode, LDO only**

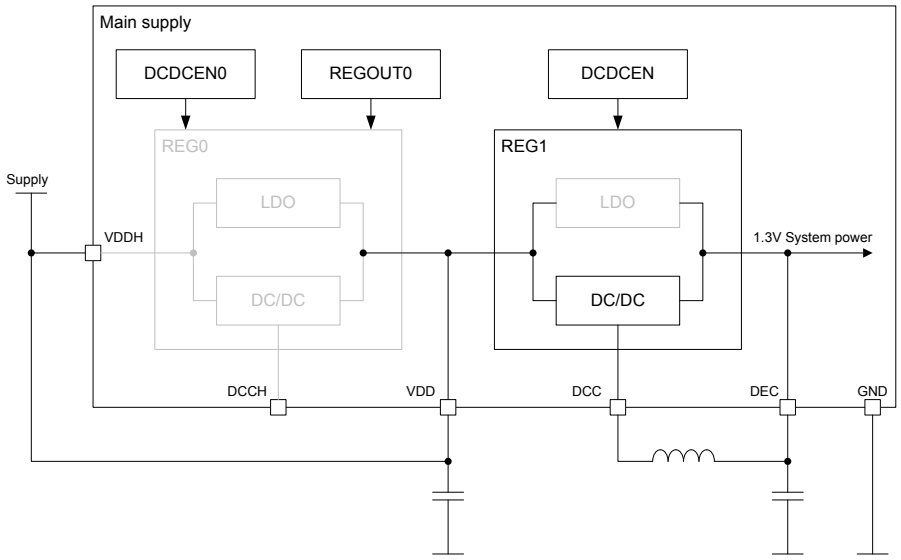



**Figure 11: Normal voltage mode, DC/DC REG1 enabled**

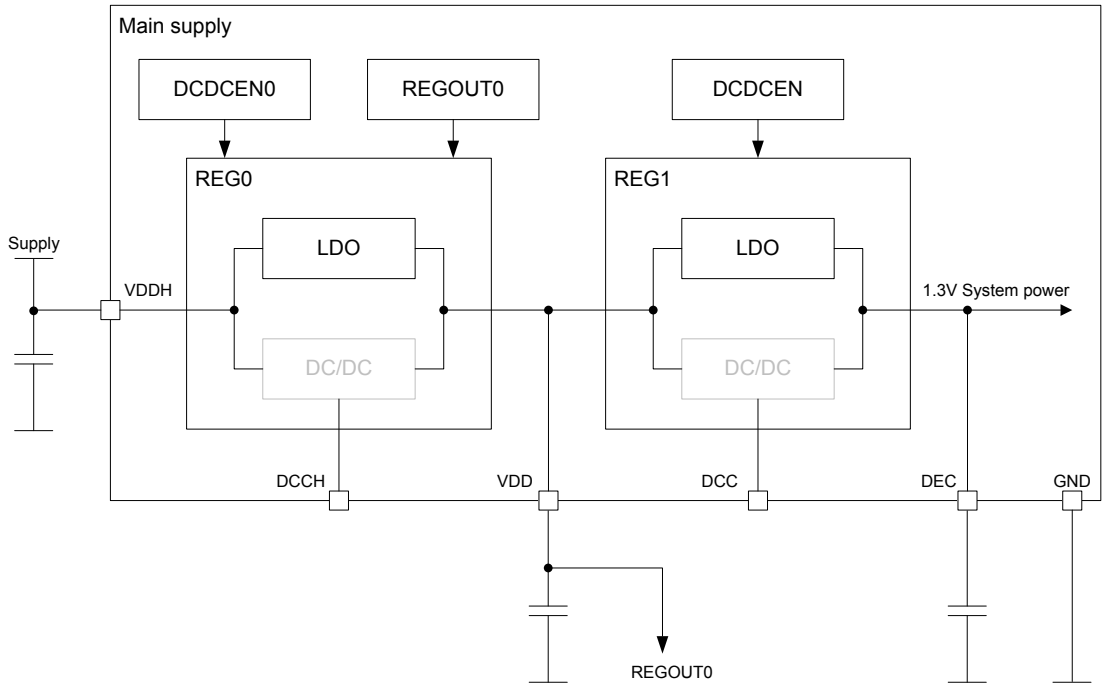



**Figure 12: High voltage mode, LDO only**

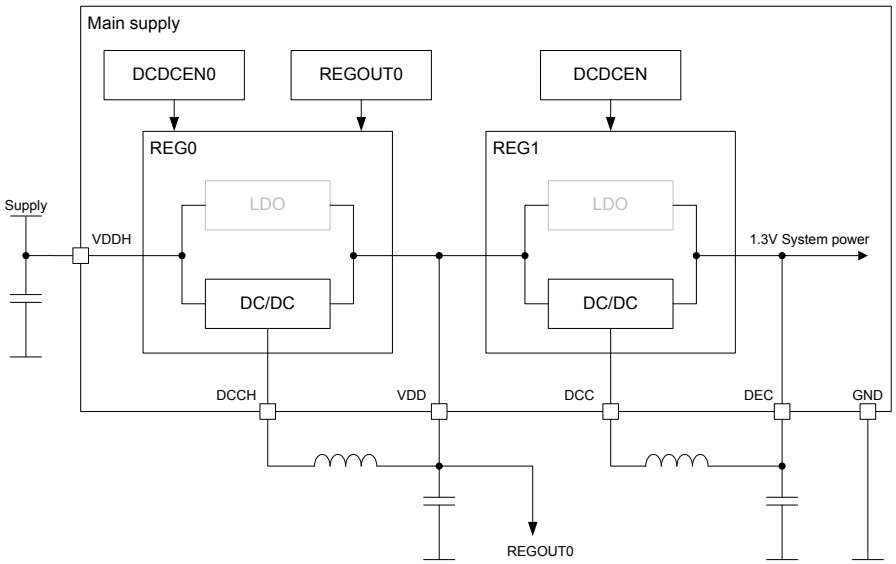



**Figure 13: High voltage mode, DC/DC for REG0 and REG1 enabled**

### 16.1.5 Power supply supervisor

The power supply supervisor enables monitoring of the connected power supply.

The power supply supervisor provides:

- Power-on reset, signalling to the circuit when a supply is connected.
- An optional power-fail comparator (POF), to signal the application when the supply voltages drop below a configured threshold.
- A fixed brownout reset detector, to hold the system in reset when the voltage is too low for safe operation.

The power supply supervisor is illustrated in *Figure 14: Power supply supervisor* on page 70. To enable and configure the power-fail comparator, see the register *POFCON* on page 79.

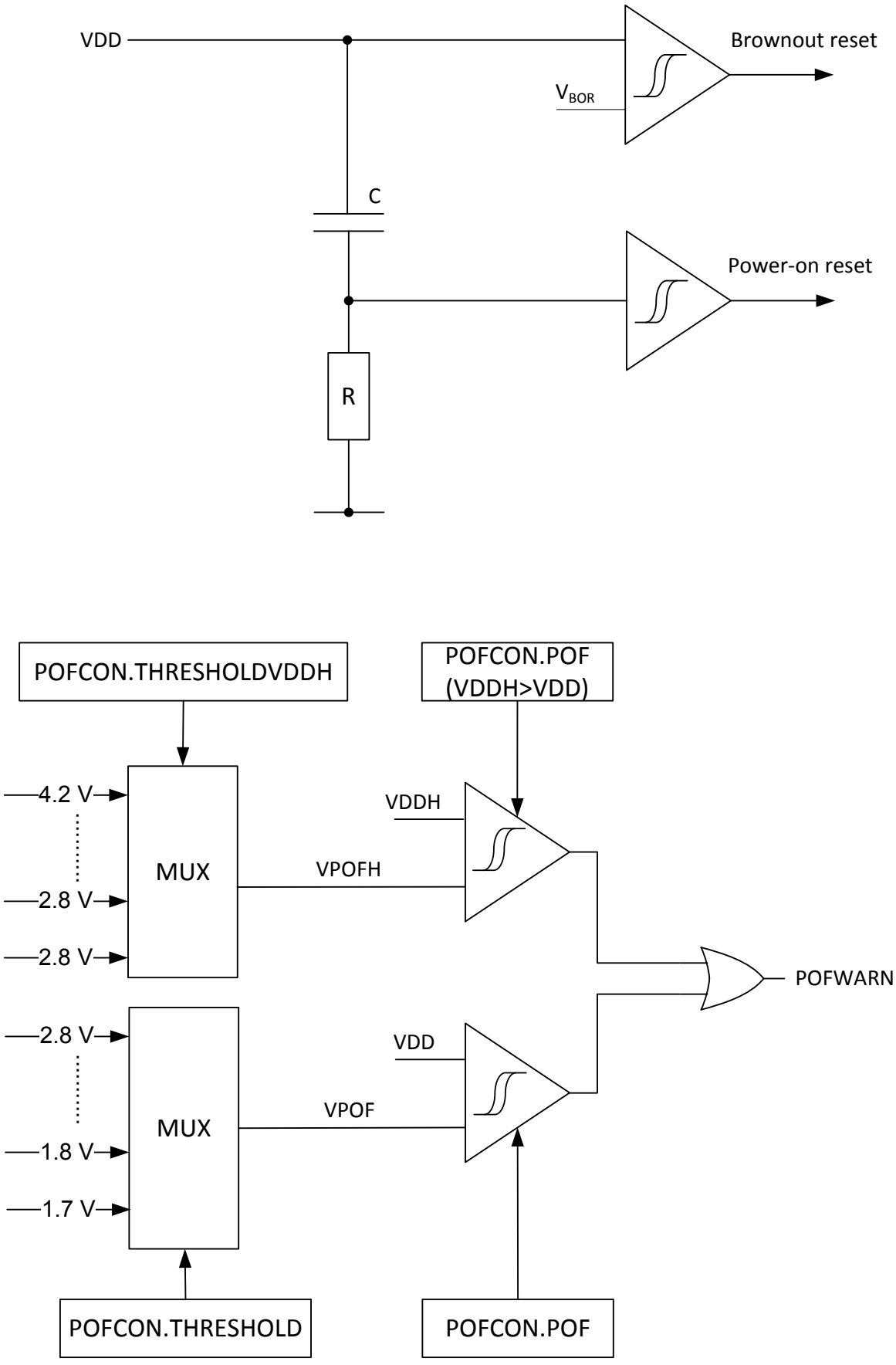



**Figure 14: Power supply supervisor**

### 16.1.6 Power-fail comparator

Using the power-fail comparator (POF) is optional. When enabled, it can provide the CPU with an early warning of an impending power supply failure.

To enable and configure the power-fail comparator, see the register *POFCON* on page 79.

The threshold ($V_{POF}$) must be configured to a suitable level. When the supply voltage falls below the defined threshold, the power-fail comparator will generate an event (POFWARN) which can be used by an application to prepare for power failure. This event will also be generated if the supply voltage is already below the threshold at the time the power-fail comparator is enabled, or if the threshold is re-configured to a level above the supply voltage.

If the power-fail warning is enabled and the supply voltage is below the threshold, the power-fail comparator will prevent the *NVMC* from performing write operations to the NVM.

The comparator features a hysteresis of $V_{HYST}$, as illustrated in *Figure 15: Power-fail comparator (BOR = brownout reset)* on page 71.

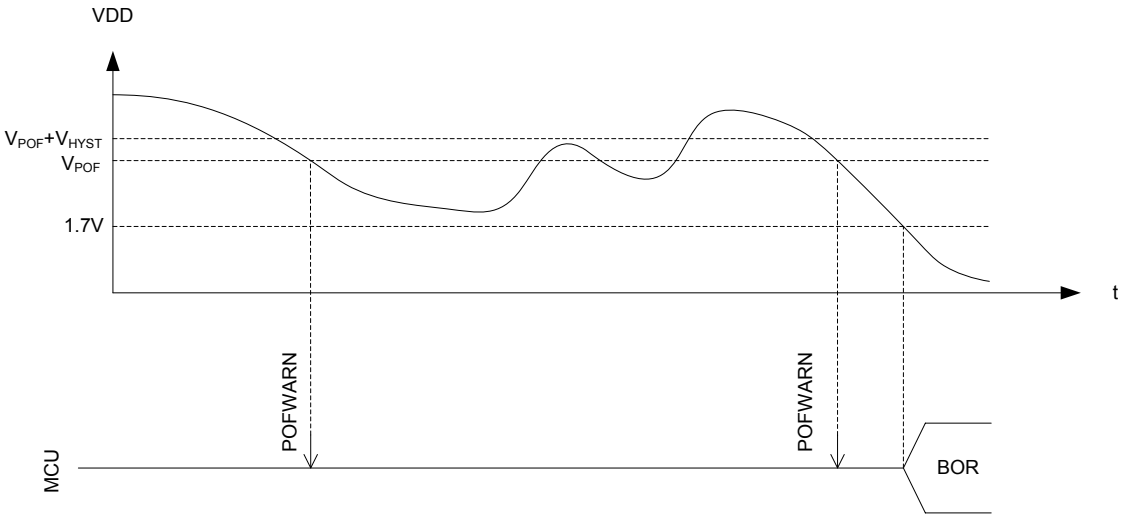



**Figure 15: Power-fail comparator (BOR = brownout reset)**

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.

## 16.2 USB supply

When using the USB peripheral, a 5 V USB supply needs to be provided on the VBUS pin.

The USB peripheral has a dedicated internal voltage regulator for converting the $V_{BUS}$ supply to 3.3 V used by the USB signalling interface (D+ and D- lines, and pull-up on D+). The rest of the USB peripheral (USBD) is supplied through the main supply like any other on-chip feature. As a consequence, both $V_{BUS}$ and either $V_{DDH}$ or $V_{DD}$ supplies are required for USB peripheral operation.

When $V_{BUS}$ rises into its valid range, the software is notified through a USBDETECTED event. A USBREMOVED event is sent when $V_{BUS}$ goes below its valid range. Use these events to implement the USBD start-up sequence described in the *USBD* chapter.

When $V_{BUS}$ rises into its valid range while the device is in System OFF, the device resets and transitions to System ON mode. The *RESETREAS* register will have the VBUS bit set to indicate the source of the wake-up.

See *VBUS detection specifications* on page 140 for the levels at which the events are sent ($V_{BUS,DETECT}$ and $V_{BUS,REMOVE}$) or at which the system is woken up from System OFF ( $V_{BUS,DETECT}$).

When the USBD peripheral is enabled through the *ENABLE* register and $V_{BUS}$ is detected, the regulator is turned on. A USBPWRRDY event is sent when the regulator's worst case settling time has elapsed, indicating to the software that it can enable the USB pull-up to signal a USB connection to the host.

The software can read the state of the $V_{BUS}$ detection and regulator output readiness at any time through the *USBREGSTATUS* register.

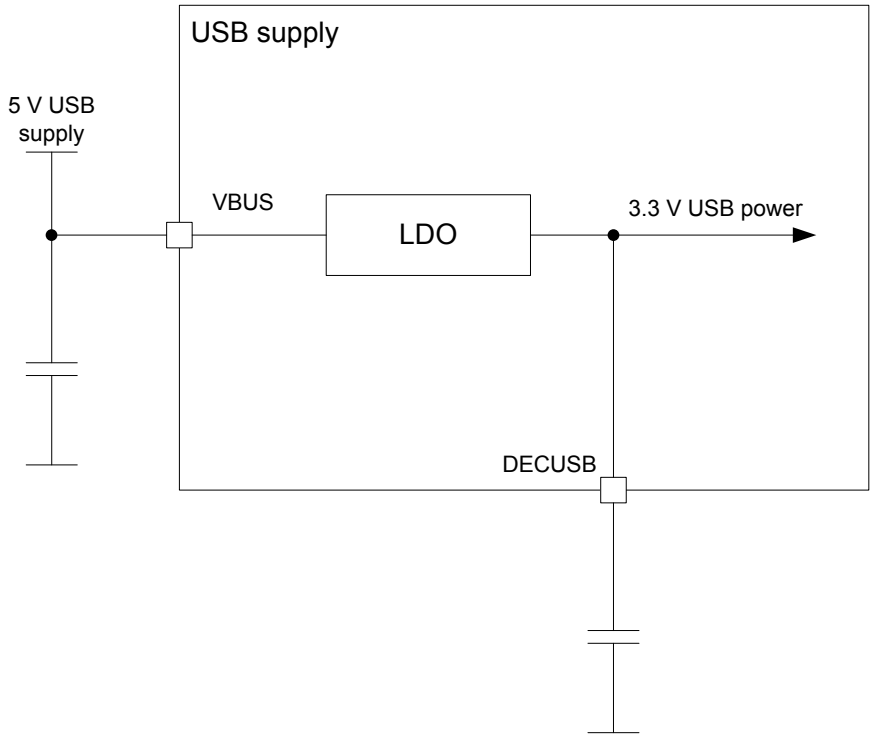



**Figure 16: USB voltage regulator**

To ensure stability, the input and output of the USB regulator need to be decoupled with a suitable decoupling capacitor. See *Reference circuitry* on page 688 for the recommended values.

## 16.3 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

1. The DETECT signal, optionally generated by the GPIO peripheral.
2. The ANADETECT signal, optionally generated by the LPCOMP module.
3. The SENSE signal, optionally generated by the NFC module to wake-on-field.
4. Detecting a *valid USB voltage* on the $V_{BUS}$ pin ($V_{BUS,DETECT}$).
5. A reset.

The system is reset when it wakes up from the System OFF mode.

One or more RAM sections can be retained in System OFF mode, depending on the settings in the RAM[n].POWER registers. RAM[n].POWER are retained registers. Note that these registers are usually overwritten by the start-up code provided with the nRF application examples.

Before entering the System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. See peripheral specific chapters for more information about how to acquire the status of EasyDMA transactions.

### 16.3.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug and trace* on page 62 for more information. Required resources needed for debugging include the following key components: *Debug and trace* on page 62, *CLOCK — Clock control* on page 141, *POWER — Power supply* on page 66, *NVMC — Non-volatile memory controller* on page 28, CPU, flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.

## 16.4 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register *RESETREAS* on page 77 provides information about the source causing the wakeup or reset.

The system can switch the appropriate internal power sources on and off , depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

### 16.4.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- Constant latency
- Low power

In constant latency mode, the CPU wakeup latency and the PPI task response are constant and kept at a minimum. This is secured by forcing a set of basic resources to be turned on while in sleep. Having a constant and predictable latency is at cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode, the automatic power management system described in *System ON mode* on page 73 ensures that the most efficient supply option is chosen to save most power. Having the lowest power possible is at cost of having a varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it is by default in low power sub power mode.

## 16.5 RAM power control

RAM power control is used for RAM retention in System OFF mode and for powering down unused sections in System ON mode.

Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* on page 20 for more information on RAM sections.

RAM sections can be retained in System OFF mode, depending on the settings in the RAM[n].POWER registers. RAM[n].POWER are retained registers.

## 16.6 Reset

Several sources may trigger a reset.

After a reset has occurred, register *RESETREAS* can be read to determine which source has triggered the reset.

### 16.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in a reset state until the power supply has reached the minimum operating voltage and the internal voltage regulators have started.

### 16.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

### 16.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The debug access port (DAP) is not reset following a wake up from System OFF mode if the device is in debug interface mode. See chapter *Debug and trace* on page 62 for more information.

### 16.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

See *ARM documentation* for more details.

A soft reset can also be generated via the register *RESET* on page 63 in the CTRL-AP.

### 16.6.5 Watchdog reset

A watchdog reset is generated when the watchdog times out.

See chapter *WDT — Watchdog timer* on page 470 for more information.

### 16.6.6 Brownout reset

The brownout reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

See section *Power fail comparator* on page 139 for more information.

## 16.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.

## 16.8 Reset behavior

Reset behavior of the different reset sources is summarized in a table.

| Reset source | Reset target CPU | Peripherals | GPIO | Debug[a] | SWJ-DP | RAM | WDT | Retained registers | RESETREAS |
|---|---|---|---|---|---|---|---|---|---|
| CPU lockup [5] | x | x | x | | | | | | |
| Soft reset | x | x | x | | | | | | |

[a] All debug components excluding SWJ-DP. See *Debug and trace* on page 62 chapter for more information about the different debug components.

[5] Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

| Reset source | Reset target CPU | Peripherals | GPIO | Debug[a] | SWJ-DP | RAM | WDT | Retained registers | RESETREAS |
|---|---|---|---|---|---|---|---|---|---|
| Wakeup from System OFF mode reset | x | x | | x [6] | | x [7] | | | |
| Watchdog reset [8] | x | x | x | x | | x | x | x | |
| Pin reset | x | x | x | x | | x | x | x | |
| Brownout reset | x | x | x | x | x | x | x | x | x |
| Power-on reset | x | x | x | x | x | x | x | x | x |

**Important:** The RAM is never reset, but depending on a reset source the content of RAM may be corrupted.

# 16.9 Registers

### Table 15: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40000000 | POWER | POWER | Power control | |

### Table 16: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| TASKS_CONSTLAT | 0x078 | Enable constant latency mode | |
| TASKS_LOWPWR | 0x07C | Enable low power mode (variable latency) | |
| EVENTS_POFWARN | 0x108 | Power failure warning | |
| EVENTS_SLEEPENTER | 0x114 | CPU entered WFI/WFE sleep | |
| EVENTS_SLEEPEXIT | 0x118 | CPU exited WFI/WFE sleep | |
| EVENTS_USBDETECTED | 0x11C | Voltage supply detected on VBUS | |
| EVENTS_USBREMOVED | 0x120 | Voltage supply removed from VBUS | |
| EVENTS_USBPWRRDY | 0x124 | USB 3.3 V supply ready | |
| *INTENSET* | 0x304 | Enable interrupt | |
| *INTENCLR* | 0x308 | Disable interrupt | |
| *RESETREAS* | 0x400 | Reset reason | |
| *RAMSTATUS* | 0x428 | RAM status register | Deprecated |
| *USBREGSTATUS* | 0x438 | USB supply status | |
| *SYSTEMOFF* | 0x500 | System OFF register | |
| *POFCON* | 0x510 | Power failure comparator configuration | |
| *GPREGRET* | 0x51C | General purpose retention register | |
| *GPREGRET2* | 0x520 | General purpose retention register | |
| *DCDCEN* | 0x578 | Enable DC/DC converter for REG1 stage. | |
| *DCDCEN0* | 0x580 | Enable DC/DC converter for REG0 stage. | |
| *MAINREGSTATUS* | 0x640 | Main supply status | |
| *RAM[0].POWER* | 0x900 | RAM0 power control register | |
| *RAM[0].POWERSET* | 0x904 | RAM0 power control set register | |
| *RAM[0].POWERCLR* | 0x908 | RAM0 power control clear register | |
| *RAM[1].POWER* | 0x910 | RAM1 power control register | |
| *RAM[1].POWERSET* | 0x914 | RAM1 power control set register | |
| *RAM[1].POWERCLR* | 0x918 | RAM1 power control clear register | |
| *RAM[2].POWER* | 0x920 | RAM2 power control register | |
| *RAM[2].POWERSET* | 0x924 | RAM2 power control set register | |
| *RAM[2].POWERCLR* | 0x928 | RAM2 power control clear register | |
| *RAM[3].POWER* | 0x930 | RAM3 power control register | |
| *RAM[3].POWERSET* | 0x934 | RAM3 power control set register | |
| *RAM[3].POWERCLR* | 0x938 | RAM3 power control clear register | |
| *RAM[4].POWER* | 0x940 | RAM4 power control register | |

6 The Debug components will not be reset if the device is in debug interface mode.

7 RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM registers parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

8 Watchdog reset is not available in System OFF.

| Register | Offset | Description |
|---|---|---|
| *RAM[4].POWERSET* | 0x944 | RAM4 power control set register |
| *RAM[4].POWERCLR* | 0x948 | RAM4 power control clear register |
| *RAM[5].POWER* | 0x950 | RAM5 power control register |
| *RAM[5].POWERSET* | 0x954 | RAM5 power control set register |
| *RAM[5].POWERCLR* | 0x958 | RAM5 power control clear register |
| *RAM[6].POWER* | 0x960 | RAM6 power control register |
| *RAM[6].POWERSET* | 0x964 | RAM6 power control set register |
| *RAM[6].POWERCLR* | 0x968 | RAM6 power control clear register |
| *RAM[7].POWER* | 0x970 | RAM7 power control register |
| *RAM[7].POWERSET* | 0x974 | RAM7 power control set register |
| *RAM[7].POWERCLR* | 0x978 | RAM7 power control clear register |
| *RAM[8].POWER* | 0x980 | RAM8 power control register |
| *RAM[8].POWERSET* | 0x984 | RAM8 power control set register |
| *RAM[8].POWERCLR* | 0x988 | RAM8 power control clear register |

## 16.9.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | POFWARN | | | Write '1' to Enable interrupt for POFWARN event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_POFWARN* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SLEEPENTER | | | Write '1' to Enable interrupt for SLEEPENTER event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_SLEEPENTER* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SLEEPEXIT | | | Write '1' to Enable interrupt for SLEEPEXIT event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_SLEEPEXIT* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | USBDETECTED | | | Write '1' to Enable interrupt for USBDETECTED event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_USBDETECTED* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | USBREMOVED | | | Write '1' to Enable interrupt for USBREMOVED event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_USBREMOVED* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | USBPWRRDY | | | Write '1' to Enable interrupt for USBPWRRDY event | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_USBPWRRDY* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | F | E | D | C | B | | | A | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | POFWARN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SLEEPENTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SLEEPEXIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | USBDETECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | USBREMOVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | USBPWRRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | I | H | G | F | E | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESETPIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOG | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | I | H | G | F | E | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SREQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset from soft reset detected | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | LOCKUP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset from CPU lock-up detected | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | LPCOMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | DIF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | NFC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset due to wake up from System OFF mode by NFC field detect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | VBUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reset due to wake up from System OFF mode by Vbus rising into valid range | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.4 RAMSTATUS ( Deprecated )

Address offset: 0x428

RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RAMBLOCK0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM block 0 is on or off/powering up | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | RAMBLOCK1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM block 1 is on or off/powering up | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | RAMBLOCK2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM block 2 is on or off/powering up | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | R | RAMBLOCK3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM block 3 is on or off/powering up | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.5 USBREGSTATUS

Address offset: 0x438

USB supply status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | VBUSDETECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoVbus | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VbusPresent | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | OUTPUTRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotReady | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ready | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.6 SYSTEMOFF

Address offset: 0x500

System OFF register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | SYSTEMOFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enter | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.7 POFCON

Address offset: 0x510

Power failure comparator configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | D | D | D | D | | | B | B | B | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | POF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | THRESHOLD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V17 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V18 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V19 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V20 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V21 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V22 | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V23 | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V24 | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V25 | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V26 | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V27 | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V28 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | D | D | D | D | | | | B | B | B | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | THRESHOLDVDDH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V27 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V28 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V29 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V30 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V31 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V32 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V33 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V34 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V35 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V36 | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V37 | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V38 | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V39 | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V40 | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V41 | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | V42 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.8 GPREGRET

Address offset: 0x51C

General purpose retention register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | GPREGRET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.9 GPREGRET2

Address offset: 0x520

General purpose retention register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | GPREGRET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.10 DCDCEN

Address offset: 0x578

Enable DC/DC converter for REG1 stage.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DCDCEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 16.9.11 DCDCEN0

Address offset: 0x580

Enable DC/DC converter for REG0 stage.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DCDCEN | | | Enable DC/DC converter for REG0 stage. |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 16.9.12 MAINREGSTATUS

Address offset: 0x640

Main supply status

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | MAINREGSTATUS | | | Main supply status |
| | | | NORMAL | 0 | Normal voltage mode. Voltage supplied on VDD. |
| | | | HIGH | 1 | High voltage mode. Voltage supplied on VDDH. |

## 16.9.13 RAM[0].POWER

Address offset: 0x900

RAM0 power control register

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x0000FFFF** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | S0POWER | | | Keep RAM section S0 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S0RETENTION.<br>All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| B | RW | S1POWER | | | Keep RAM section S1 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.<br>All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| C | RW | S2POWER | | | Keep RAM section S2 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION.<br>All RAM sections will be OFF in System OFF mode. |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 ON or OFF in System ON mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.14 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.15 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM0 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.16 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | Keep RAM section S11 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.17 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.18 RAM[1].POWERCLR

Address offset: 0x918

RAM1 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| d | W | S13RETENTION | | | Keep retention on RAM section S13 when RAM section is switched off |
| | | | Off | 1 | Off |
| e | W | S14RETENTION | | | Keep retention on RAM section S14 when RAM section is switched off |
| | | | Off | 1 | Off |
| f | W | S15RETENTION | | | Keep retention on RAM section S15 when RAM section is switched off |
| | | | Off | 1 | Off |

## 16.9.19 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | S0POWER | | | Keep RAM section S0 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S0RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| B | RW | S1POWER | | | Keep RAM section S1 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| C | RW | S2POWER | | | Keep RAM section S2 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| D | RW | S3POWER | | | Keep RAM section S3 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| E | RW | S4POWER | | | Keep RAM section S4 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| F | RW | S5POWER | | | Keep RAM section S5 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION. All RAM sections will be OFF in System OFF mode. |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.20 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.21 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM2 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.22 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | S11RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| M | RW | S12POWER | | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| N | RW | S13POWER | | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| O | RW | S14POWER | | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| P | RW | S15POWER | | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| Q | RW | S0RETENTION | | | Keep retention on RAM section S0 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| R | RW | S1RETENTION | | | Keep retention on RAM section S1 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| S | RW | S2RETENTION | | | Keep retention on RAM section S2 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| T | RW | S3RETENTION | | | Keep retention on RAM section S3 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| U | RW | S4RETENTION | | | Keep retention on RAM section S4 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| V | RW | S5RETENTION | | | Keep retention on RAM section S5 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| W | RW | S6RETENTION | | | Keep retention on RAM section S6 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.23 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM3 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.24 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
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| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.25 RAM[4].POWER

Address offset: 0x940

RAM4 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S0RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 ON or OFF in System ON mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | Keep RAM section S11 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.26 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.27 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM4 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.28 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
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| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| N | RW | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.29 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.30 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM5 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.31 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | |
| Id | | | | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A | |
| **Reset 0x0000FFFF** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** | |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | | | S11RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| M | RW | S12POWER | | | Keep RAM section S12 ON or OFF in System ON mode.<br><br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| N | RW | S13POWER | | | Keep RAM section S13 ON or OFF in System ON mode.<br><br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| O | RW | S14POWER | | | Keep RAM section S14 ON or OFF in System ON mode.<br><br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| P | RW | S15POWER | | | Keep RAM section S15 ON or OFF in System ON mode.<br><br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| Q | RW | S0RETENTION | | | Keep retention on RAM section S0 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| R | RW | S1RETENTION | | | Keep retention on RAM section S1 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| S | RW | S2RETENTION | | | Keep retention on RAM section S2 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| T | RW | S3RETENTION | | | Keep retention on RAM section S3 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| U | RW | S4RETENTION | | | Keep retention on RAM section S4 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| V | RW | S5RETENTION | | | Keep retention on RAM section S5 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |
| W | RW | S6RETENTION | | | Keep retention on RAM section S6 when RAM section is in OFF |
| | | | Off | 0 | Off |
| | | | On | 1 | On |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.32 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM6 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.33 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
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## 16.9.34 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | Keep RAM section S11 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.35 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.36 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM7 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.37 RAM[8].POWER

Address offset: 0x980

RAM8 power control register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S0RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION.<br>All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 ON or OFF in System ON mode.<br>RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is in OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.38 RAM[8].POWERSET

Address offset: 0x984

RAM8 power control set register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S8 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S9 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S10 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S11 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S12 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S13 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S14 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S15 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 16.9.39 RAM[8].POWERCLR

Address offset: 0x988

RAM8 power control clear register

When read, this register will return the value of the POWER register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | S0POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S0 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | S1POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S1 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | S2POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S2 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | W | S3POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S3 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | W | S4POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S4 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | W | S5POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S5 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | W | S6POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S6 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | W | S7POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S7 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | W | S8POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S8 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | W | S9POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S9 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | W | S10POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S10 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | W | S11POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S11 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | W | S12POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S12 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | W | S13POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S13 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | W | S14POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S14 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | W | S15POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep RAM section S15 of RAM8 on or off in System ON mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | W | S0RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S0 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | W | S1RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S1 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | W | S2RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S2 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | W | S3RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S3 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | W | S4RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S4 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | W | S5RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S5 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | W | S6RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S6 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | W | S7RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep retention on RAM section S7 when RAM section is switched off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x0000FFFF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | W | S8RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | W | S9RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | W | S10RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | W | S11RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | W | S12RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | W | S13RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | W | S14RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | W | S15RETENTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 16.10 Electrical specification

## 16.10.1 Regulator operating conditions

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD,POR}$ | VDD supply voltage needed during power-on reset. | 1.75 | | | V |
| $V_{DD}$ | VDD operating voltage. | 1.7 | 3.0 | 3.6 | V |
| $V_{DDH}$ | VDDH operating voltage. | 2.5 | 3.7 | 5.5 | V |
| $V_{DDOUT}$ | Voltage output on VDD when supplied from internal regulator (REG0). Note: VDDH is the input to REG0. | 1.8 | | 3.3 | V |
| $I_{EX,OFF}$ | Current draw of external circuitry from VDD in High voltage mode (supply on VDDH) with *EXTSUPPLY* enabled in UICR, during System OFF. | | | 1 | mA |
| $I_{EX,ON}$ | Current that can be drawn by external circuitry from VDD in High voltage mode (supply on VDDH) with *EXTSUPPLY* enabled in UICR, during System ON.[9] | | 25 | | mA |
| $I_{REG0}$ | Current draw from VDD in High voltage mode (supply on VDDH) of both external circuits and nRF device. | | | 50 | mA |
| $V_{EXDIF}$ | Minimum difference between voltage supplied on VDDH pin and voltage output on VDD pin. | 0.3 | | | V |

[9] The sum of nRF device load current and external circuit load current cannot exceed $I_{REG0}$; At high TX power settings or other operating modes of the nRF device where peak load current is high, the current available for external circuits may be less than $I_{EX,ON}$ nominal.

## 16.10.2 Current consumption, sleep

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OFF,NV}$ | System OFF current, no RAM retention, Normal voltage mode (supply on VDD) | | 0.4 | | µA |
| $I_{ON,NV}$ | System ON base current, no RAM retention, Normal voltage mode (supply on VDD) | | 0.7 | | µA |
| $I_{OFF,HV}$ | System OFF current, no RAM retention, High voltage mode (supply on VDDH) | | 0.4 | | µA |
| $I_{ON,HV}$ | System ON base current, no RAM retention, High voltage mode (supply on VDDH) | | 0.7 | | µA |
| $I_{RAM}$ | Additional RAM retention current per 4 KB RAM section | | 30 | | nA |

## 16.10.3 Device startup times

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{POR}$ | Time in power-on reset after VDD reaches V,dd,start for all supply voltages and temperatures. Dependent on supply rise time. | | | | |
| $t_{POR,10µs}$ | VDD rise time 10 µs | | 1 | 10 | ms |
| $t_{POR,10ms}$ | VDD rise time 10 ms[10] | | 9 | | ms |
| $t_{POR,60ms}$ | VDD rise time 60 ms[10] | | 23 | 110 | ms |
| $t_{RISE,REG0OUT}$ | REG0 output (VDD) rise time after VDDH reaches minimum VDDH supply voltage[10] | | | | |
| $t_{RISE,REG0OUT,10µs}$ | VDDH rise time 10 µs[10] | | 0.22 | 1.55 | ms |
| $t_{RISE,REG0OUT,10ms}$ | VDDH rise time 10 ms[10] | | 5 | | ms |
| $t_{RISE,REG0OUT,100ms}$ | VDDH rise time 100 ms[10] | 30 | 50 | 80 | ms |
| $t_{PINR}$ | If a GPIO pin is configured as reset, the maximum time taken to pull up the pin and release reset after power-on reset. Dependent on the pin capacitive load. | | | | |
| $t_{PINR,500nF}$ | 500 nF capacitance at reset pin | | | 32.5 | ms |
| $t_{PINR,10µF}$ | 10 µF capacitance at reset pin | | | 650 | ms |
| $t_{R2ON}$ | Time from power-on reset to System ON | | | | |
| $t_{R2ON,NOTCONF}$ | If reset pin not configured. | tPOR | | | ms |
| $t_{R2ON,CONF}$ | If reset pin configured. | tPOR + tPINR | | | ms |
| $t_{OFF2ON}$ | Time from OFF to CPU execute. | | 16.5 | | µs |
| $t_{IDLE2CPU}$ | Time from IDLE to CPU execute. | | 3.0 | | µs |
| $t_{EVTSET,CL1}$ | Time from HW event to PPI event in Constant Latency System ON mode. | | 0.0625 | | µs |
| $t_{EVTSET,CL0}$ | Time from HW event to PPI event in Low Power System ON mode | | 0.0625 | | µs |

## 16.10.4 Power fail comparator

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{POF,NV}$ | Nominal power level warning thresholds (falling supply voltage) in Normal voltage mode (supply on VDD). Levels are configurable between Min. and Max. in 100 mV increments. | 1.7 | | 2.8 | V |
| $V_{POF,HV}$ | Nominal power level warning thresholds (falling supply voltage) in High voltage mode (supply on VDDH). Levels are configurable in 100 mV increments. | 2.7 | | 4.2 | V |
| $V_{POFTOL}$ | Threshold voltage tolerance (applies in both Normal voltage mode and High voltage mode) | -5 | | 5 | % |
| $V_{POFHYST}$ | Threshold voltage hysteresis (applies in both Normal voltage mode and High voltage mode) | 40 | 50 | 60 | mV |

[10] See *Recommended operating conditions* on page 17 for more information.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{BOR,OFF}$ | Brownout reset voltage range System OFF mode. Brownout only applies to the voltage on VDD. | 1.2 | | 1.62 | V |
| $V_{BOR,ON}$ | Brownout reset voltage range System ON mode. Brownout only applies to the voltage on VDD. | 1.57 | 1.6 | 1.63 | V |

## 16.10.5 USB operating conditions

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{BUS}$ | Supply voltage on VBUS pin. | 4.35 | 5 | 5.5 | V |
| $V_{DPDM}$ | Voltage on D+ and D- lines | VSS - 0.3 V | | VUSB33 + 0.3 V | V |

## 16.10.6 USB regulator specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{USB,QUIES}$ | USB regulator quiescence current drawn from Vbus (USBD enabled). | | 170 | | µA |
| $t_{USBPWRRDY}$ | Time from USB enabled to USBPWRRDY event triggered, $V_{BUS}$ supply provided. | | 1 | | ms |
| $V_{USB33}$ | On voltage at the USB regulator output (DECUSB pin) | 3.0 | 3.3 | 3.6 | V |
| $R_{SOURCE,VBUS}$ | Maximum source resistance on Vbus, incl. cable | | | 2 | Ω |

## 16.10.7 VBUS detection specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{BUS,DETECT}$ | Voltage at which rising VBUS gets reported by USBDETECTED | 3.45 | 4.01 | 4.26 | V |
| $V_{BUS,REMOVE}$ | Voltage at which decreasing VBUS gets reported by USBREMOVED | 3.1 | 3.61 | 3.84 | V |

# 17 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-500 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of crystal oscillator activity for low latency start up
- Automatic internal oscillator and clock control, and distribution for ultra-low power

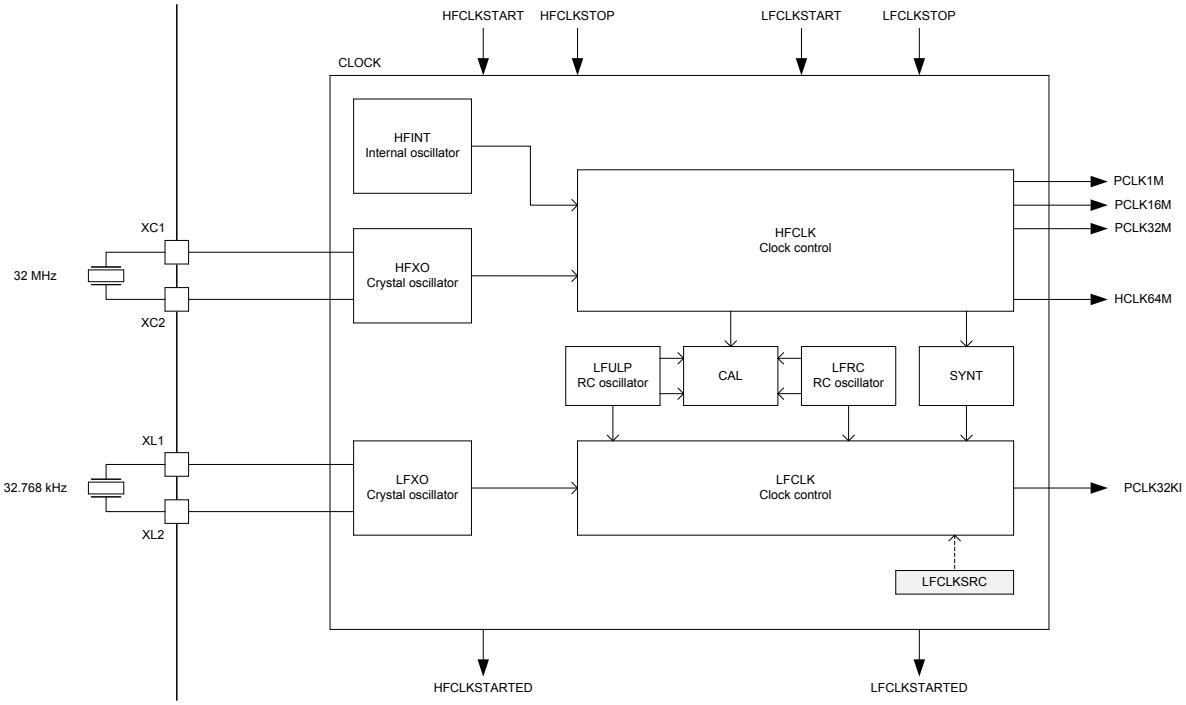



**Figure 17: Clock control**

## 17.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see *Figure 17: Clock control* on page 141.

When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started.

The HFXO is started by triggering the HFCLKSTART task and stopped by triggering the HFCLKSTOP task. When the HFCLKSTART task is triggered, the HFCLKSTARTED event is generated once the HFXO startup time has elapsed. The HFXO startup time is given as the sum of the following:

- HFXO power-up time, as specified in *64 MHz crystal oscillator (HFXO)* on page 150.
- HFXO debounce time, as specified in the *HFXODEBOUNCE* on page 148 register.

The HFXO must be running to use the RADIO or the calibration mechanism associated with the 32.768 kHz RC oscillator.

### 17.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

*Figure 18: Circuit diagram of the 64 MHz crystal oscillator* on page 142 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

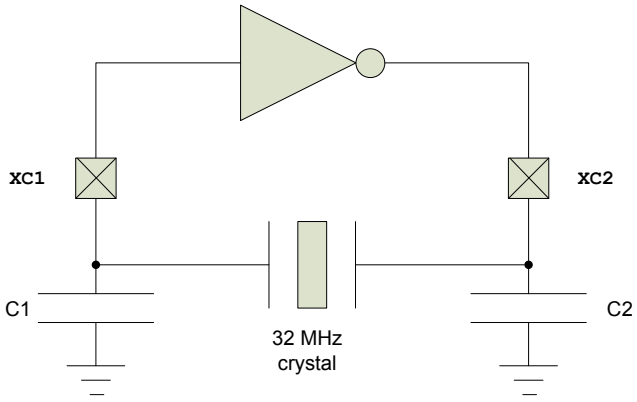



**Figure 18: Circuit diagram of the 64 MHz crystal oscillator**

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 688. $C_{pcb1}$ and $C_{pcb2}$ are stray capacitances on the PCB. $C_{pin}$ is the pin input capacitance on the `XC1` and `XC2` pins. See table *64 MHz crystal oscillator (HFXO)* on page 150. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table *64 MHz crystal oscillator (HFXO)* on page 150. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.

## 17.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 17: Clock control* on page 141, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 148 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

The *LFCLKSRC* on page 148 register controls the clock source, and its allowed swing. The truth table for various situations is as follows:

**Table 17: LFCLKSRC configuration depending on clock source**

| SRC | EXTERNAL | BYPASS | Comment |
|---|---|---|---|
| 0 | 0 | 0 | Normal operation, RC is source |
| 0 | 0 | 1 | DO NOT USE |
| 0 | 1 | X | DO NOT USE |
| 1 | 0 | 0 | Normal XTAL operation |
| 1 | 1 | 0 | Apply external low swing signal to XL1, ground XL2 |
| 1 | 1 | 1 | Apply external full swing signal to XL1, leave XL2 grounded or unconnected |
| 1 | 0 | 1 | DO NOT USE |
| 2 | 0 | 0 | Normal operation, synth is source |
| 2 | 0 | 1 | DO NOT USE |
| 2 | 1 | X | DO NOT USE |

It is not allowed to write to register *LFCLKSRC* on page 148 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 147 indicates a 'LFCLK running' state.

The synthesized 32.768 kHz clock depends on the HFCLK to run. If high accuracy is required for the LFCLK running off the synthesized 32.768 kHz clock, the HFCLK must be generated from the HFCLK crystal oscillator.

### 17.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC oscillator has two modes of operation, that is normal and ultra-low power (ULP) mode, enabling the user to trade power consumption against accuracy of the clock. The mode/status of the LFRC is selected/read in the *LFRCMODE* on page 149 register. It is allowed to change LFRC mode when the LFRC oscillator is running.

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. The LFRC oscillator does not require additional external components.

### 17.2.2 Calibrating the 32.768 kHz RC oscillator

After any of the two 32.768 kHz RC oscillators are started and running, they can be calibrated by triggering the CAL task. The 32.768 kHz RC oscillator will then temporarily request the HFCLK to be used as a reference for the calibration.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

It is not allowed to stop the LFRC or write to *LFRCMODE* on page 149 during an ongoing calibration.

### 17.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

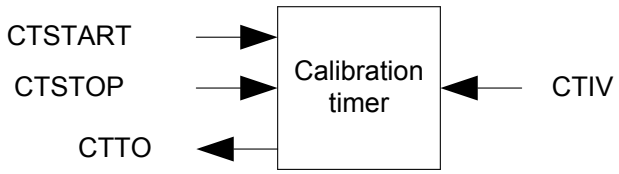



**Figure 19: Calibration timer**

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.

### 17.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 500 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the *XL1* pin. The *XL2* pin shall then be grounded.
- Rail-to-rail clock signal applied to the *XL1* pin. The *XL2* pin shall then be grounded or left unconnected.

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. *Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator* on page 144 shows the LFXO circuitry.

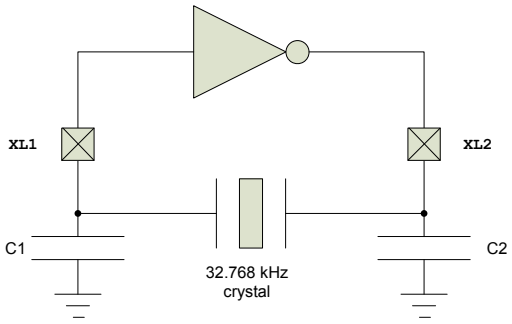



**Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator**

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. $C_{pcb1}$ and $C_{pcb2}$ are stray capacitances on the PCB. $C_{pin}$ is the pin input capacitance on the XC1 and XC2 pins (see *Low frequency crystal oscillator (LFXO)* on page 150). The load capacitors C1 and C2 should have the same value.

For more information, see *Reference circuitry* on page 688.

### 17.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

## 17.3 Registers

**Table 18: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40000000 | CLOCK | CLOCK | Clock control | |

**Table 19: Register Overview**

| Register | Offset | Description | |
|---|---|---|---|
| TASKS_HFCLKSTART | 0x000 | Start HFCLK crystal oscillator | |
| TASKS_HFCLKSTOP | 0x004 | Stop HFCLK crystal oscillator | |
| TASKS_LFCLKSTART | 0x008 | Start LFCLK source | |
| TASKS_LFCLKSTOP | 0x00C | Stop LFCLK source | |
| TASKS_CAL | 0x010 | Start calibration of LFRC or LFULP oscillator | |
| TASKS_CTSTART | 0x014 | Start calibration timer | |
| TASKS_CTSTOP | 0x018 | Stop calibration timer | |
| EVENTS_HFCLKSTARTED | 0x100 | HFCLK oscillator started | |
| EVENTS_LFCLKSTARTED | 0x104 | LFCLK started | |
| EVENTS_DONE | 0x10C | Calibration of LFCLK RC oscillator complete event | |
| EVENTS_CTTO | 0x110 | Calibration timer timeout | |
| *INTENSET* | 0x304 | Enable interrupt | |
| *INTENCLR* | 0x308 | Disable interrupt | |
| *HFCLKRUN* | 0x408 | Status indicating that HFCLKSTART task has been triggered | |
| *HFCLKSTAT* | 0x40C | HFCLK status | |
| *LFCLKRUN* | 0x414 | Status indicating that LFCLKSTART task has been triggered | |
| *LFCLKSTAT* | 0x418 | LFCLK status | |
| *LFCLKSRCCOPY* | 0x41C | Copy of LFCLKSRC register, set when LFCLKSTART task was triggered | |
| *LFCLKSRC* | 0x518 | Clock source for the LFCLK | |
| *HFXODEBOUNCE* | 0x528 | HFXO debounce time. The HFXO is started by triggering the TASKS_HFCLKSTART task. | |
| *CTIV* | 0x538 | Calibration timer interval | Retained |
| *TRACECONFIG* | 0x55C | Clocking options for the Trace Port debug interface | |
| *LFRCMODE* | 0x5B4 | LFRC mode configuration | |

## 17.3.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | HFCLKSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | LFCLKSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CTTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Write '1' to Enable interrupt for HFCLKSTARTED event

See *EVENTS_HFCLKSTARTED*

Enable

Read: Disabled

Read: Enabled

Write '1' to Enable interrupt for LFCLKSTARTED event

See *EVENTS_LFCLKSTARTED*

Enable

Read: Disabled

Read: Enabled

Write '1' to Enable interrupt for DONE event

See *EVENTS_DONE*

Enable

Read: Disabled

Read: Enabled

Write '1' to Enable interrupt for CTTO event

See *EVENTS_CTTO*

Enable

Read: Disabled

Read: Enabled

## 17.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | HFCLKSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | LFCLKSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CTTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Write '1' to Disable interrupt for HFCLKSTARTED event

See *EVENTS_HFCLKSTARTED*

Disable

Read: Disabled

Read: Enabled

Write '1' to Disable interrupt for LFCLKSTARTED event

See *EVENTS_LFCLKSTARTED*

Disable

Read: Disabled

Read: Enabled

Write '1' to Disable interrupt for DONE event

See *EVENTS_DONE*

Disable

Read: Disabled

Read: Enabled

Write '1' to Disable interrupt for CTTO event

See *EVENTS_CTTO*

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | STATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotTriggered | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Triggered | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | B | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Xtal | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | STATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotRunning | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Running | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | STATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotTriggered | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Triggered | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | B | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | B | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Xtal | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Synth | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | STATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotRunning | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Running | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Xtal | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Synth | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | C | B | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Xtal | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Synth | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | BYPASS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | EXTERNAL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.9 HFXODEBOUNCE

Address offset: 0x528

HFXO debounce time. The HFXO is started by triggering the TASKS_HFCLKSTART task.

The EVENTS_HFCLKSTARTED event is generated after the HFXO power up time + the HFXO debounce time has elapsed. It is not allowed to change the value of this register while the HFXO is starting.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000010** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | HFXODEBOUNCE | | 0x01..0xFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | HFXO debounce time. Debounce time = HFXODEBOUNCE * 16 us. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.10 CTIV ( Retained )

Address offset: 0x538

This register is a retained register

Calibration timer interval

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CTIV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Calibration timer interval in multiple of 0.25 seconds. Range: 0.25 seconds to 31.75 seconds. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.11 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | B | B | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TRACEPORTSPEED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Speed of Trace Port clock. Note that the TRACECLK pin will output this clock divided by two. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 32MHz | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 32 MHz Trace Port clock (TRACECLK = 16 MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 16MHz | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 16 MHz Trace Port clock (TRACECLK = 8 MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 8MHz | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 8 MHz Trace Port clock (TRACECLK = 4 MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4MHz | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 4 MHz Trace Port clock (TRACECLK = 2 MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | TRACEMUX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin multiplexing of trace signals. See pin assignment chapter for more details. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | GPIO | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No trace signals routed to pins. All pins can be used as regular GPIOs. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Serial | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | SWO trace signal routed to pin. Remaining pins can be used as regular GPIOs. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Parallel | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | All trace signals (TRACECLK and TRACEDATA[n]) routed to pins. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 17.3.12 LFRCMODE

Address offset: 0x5B4

LFRC mode configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | B | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Set LFRC mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Normal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Normal mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ULP | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Ultra-low power mode (ULP) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active LFRC mode. This field is read only. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Normal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Normal mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | B | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | ULP | 1 | Ultra-low power mode (ULP) |

# 17.4 Electrical specification

## 17.4.1 64 MHz internal oscillator (HFINT)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_HFINT}$ | Nominal output frequency | | 64 | | MHz |
| $f_{TOL\_HFINT}$ | Frequency tolerance | | ±1.5 | ±8 | % |

## 17.4.2 64 MHz crystal oscillator (HFXO)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_HFXO}$ | Nominal output frequency | | 64 | | MHz |
| $f_{XTAL\_HFXO}$ | External crystal frequency | | 32 | | MHz |
| $f_{TOL\_HFXO}$ | Frequency tolerance requirement for 2.4 GHz proprietary radio applications | | | ±60 | ppm |
| $f_{TOL\_HFXO\_BLE}$ | Frequency tolerance requirement, Bluetooth low energy applications | | | ±40 | ppm |
| $C_{L\_HFXO}$ | Load capacitance | | | 12 | pF |
| $C_{0\_HFXO}$ | Shunt capacitance | | | 7 | pF |
| $R_{S\_HFXO\_7PF}$ | Equivalent series resistance C0 = 7 pF | | | 60 | ohm |
| $R_{S\_HFXO\_5PF}$ | Equivalent series resistance C0 = 5 pF | | | 60 | ohm |
| $R_{S\_HFXO\_3PF}$ | Equivalent series resistance C0 = 3 pF | | | 100 | ohm |
| $P_{D\_HFXO}$ | Drive level | | | 100 | µW |
| $C_{PIN\_HFXO}$ | Input capacitance XC1 and XC2 | | 3 | | pF |
| $I_{STBY\_X32M}$ | Core standby current for various crystals | | | | |
| $I_{STBY\_X32M\_X0}$ | Epson TSX-3225 | | 80 | | µA |
| $I_{STBY\_X32M\_X1}$ | Epson FA-20H | | 72 | | µA |
| $I_{STBY\_X32M\_X2}$ | Epson FA-128 | | 70 | | µA |
| $I_{STBY\_X32M\_X3}$ | NDK NX1612AA | | 136 | | µA |
| $I_{STBY\_X32M\_X4}$ | NDK NX1210AB | | 143 | | µA |
| $I_{START\_X32M}$ | Average startup current for various crystals, first 1 ms | | | | |
| $I_{START\_X32M\_X0}$ | Epson TSX-3225 | | 328 | | µA |
| $I_{START\_X32M\_X1}$ | Epson FA-20H | | 363 | | µA |
| $I_{START\_X32M\_X2}$ | Epson FA-128 | | 396 | | µA |
| $I_{START\_X32M\_X3}$ | NDK NX1612AA | | 783 | | µA |
| $I_{START\_X32M\_X4}$ | NDK NX1210AB | | 833 | | µA |
| $t_{POWER\_X32M}$ | Power-up time | .. | .. | .. | µs |
| $t_{START\_X32M}$ | Startup time for various crystals | | | | |
| $t_{START\_X32M\_X0}$ | Epson TSX-3225 | | 304 | | µs |
| $t_{START\_X32M\_X1}$ | Epson FA-20H | | 316 | | µs |
| $t_{START\_X32M\_X2}$ | Epson FA-128 | | 328 | | µs |
| $t_{START\_X32M\_X3}$ | NDK NX1612AA | | | | µs |
| $t_{START\_X32M\_X4}$ | NDK NX1210AB | | | | µs |

## 17.4.3 Low frequency crystal oscillator (LFXO)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_LFXO}$ | Crystal frequency | | 32.768 | | kHz |
| $f_{TOL\_LFXO\_BLE}$ | Frequency tolerance requirement for BLE stack | | | ±500 | ppm |
| $f_{TOL\_LFXO\_ANT}$ | Frequency tolerance requirement for ANT stack | | | ±50 | ppm |
| $C_{L\_LFXO}$ | Load capacitance | | | 12.5 | pF |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{0\_LFXO}$ | Shunt capacitance | | | 2 | pF |
| $R_{S\_LFXO}$ | Equivalent series resistance | | | 100 | kohm |
| $P_{D\_LFXO}$ | Drive level | | | 1 | uW |
| $C_{pin}$ | Input capacitance on XL1 and XL2 pads | | 4 | | pF |
| $I_{LFXO}$ | Run current for 32.768 kHz crystal oscillator | | 0.23 | | µA |
| $t_{START\_LFXO}$ | Startup time for 32.768 kHz crystal oscillator | | 0.25 | | s |

### 17.4.4 Low frequency RC oscillator (LFRC), Normal mode

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_LFRC}$ | Nominal frequency | | 32.768 | | kHz |
| $f_{TOL\_LFRC}$ | Frequency tolerance, uncalibrated | | | ±2.5 | % |
| $f_{TOL\_CAL\_LFRC}$ | Frequency tolerance after calibration[11] | | | ±500 | ppm |
| $I_{LFRC}$ | Run current | | 0.7 | | µA |
| $t_{START\_LFRC}$ | Startup time | | 1000 | | us |

### 17.4.5 Low frequency RC oscillator (LFRC), Ultra-low power mode (ULP)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_LFULP}$ | Nominal frequency | | 32.768 | | kHz |
| $f_{TOL\_UNCAL\_LFULP}$ | Frequency tolerance, uncalibrated | | | ±7 | % |
| $f_{TOL\_CAL\_LFULP}$ | Frequency tolerance after calibration[12] | | | ±2000 | ppm |
| $I_{LFULP}$ | Run current | | 0.2 | | µA |
| $t_{START\_LFULP}$ | Startup time | | 1500 | | us |

### 17.4.6 Synthesized low frequency clock (LFSYNT)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{NOM\_LFSYNT}$ | Nominal frequency | | 32.768 | | kHz |

[11] Constant temperature within ±0.5 °C and calibration performed at least every 8 seconds, defined as 3 sigma

[12] Constant temperature within ±0.5 °C and calibration performed at least every 8 seconds, defined as 3 sigma

# 18 Power and clock management

Power and clock management in nRF52840 is optimized for ultra-low power applications.

The core of the power and clock management system is the Power Management Unit (PMU) illustrated in *Figure 21: Power Management Unit* on page 152.

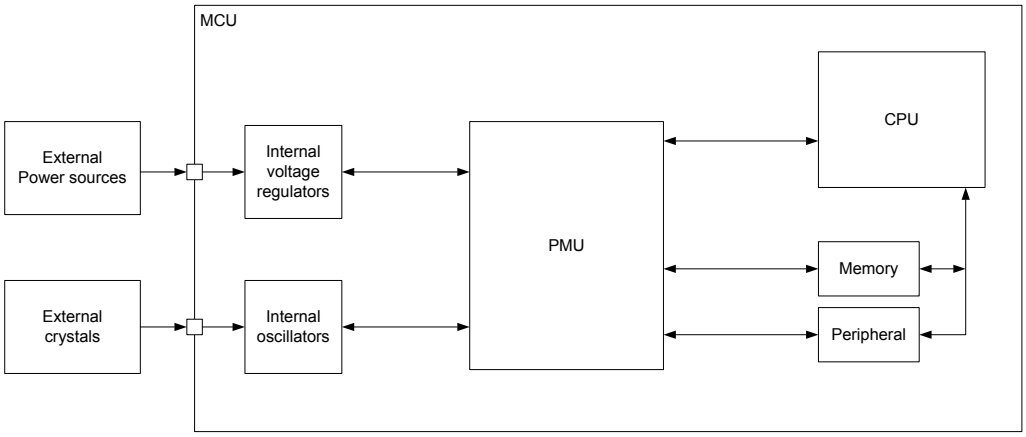



**Figure 21: Power Management Unit**

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

## 18.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. To facilitate this process, there is a defined set of current consumption scenarios.

See *Electrical specification* on page 152 for application scenarios showing average current drawn from the VDD supply.

Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 20: Current consumption scenarios, common conditions* on page 152 shows the conditions used for a scenario unless otherwise is stated in the scenario description.

**Table 20: Current consumption scenarios, common conditions**

| Condition | Value |
|---|---|
| VDD | 3 V |
| Temperature | 25°C |
| CPU | WFI/WFE sleep |
| Peripherals | All idle |
| Clock | Not running |
| Regulator | DC/DC |

### 18.1.1 Electrical specification

#### Current consumption: Radio

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{RADIO\_TX0}$ | 0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO | | 6.6 | | mA |
| $I_{RADIO\_TX1}$ | -40 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO | | | | mA |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{RADIO\_RX0}$ | Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO | | 6.4 | | mA |
| $I_{RADIO\_RX1}$ | Radio RX @ 2 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Regulator = LDO | | 11 | | mA |
| $I_{RADIO\_RX2}$ | Radio RX @ 2 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Regulator = LDO | | 12.6 | | mA |
| $I_{RADIO\_RX2}$ | Radio RX @ 125 kb/s Bluetooth Low Energy mode, Clock = HFXO, Regulator = LDO | | 10.9 | | mA |

### Current consumption: Radio protocol configurations

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{S0}$ | CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Cache enabled | | 9.1 | | mA |
| $I_{S1}$ | CPU running CoreMark from Flash, Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Cache enabled | | 8.9 | | mA |
| $I_{S4}$ | CPU running CoreMark from Flash, Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Cache enabled, VDDH = 5V, REG0 out = 3V | | 7.5 | | mA |

### Current consumption: Ultra-low power

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{ON\_RAMOFF\_EVENT}$ | System ON, No RAM retention, Wake on any event | | | | µA |
| $I_{ON\_RAMON\_EVENT}$ | System ON, Full RAM retention, Wake on any event | | | | µA |
| $I_{ON\_RAMOFF\_RTC}$ | System ON, No RAM retention, Wake on RTC (LFCLK = LFRC, normal mode) | | 1.3 | | µA |
| $I_{OFF\_RAMOFF\_RESET}$ | System OFF, No RAM retention, Wake on reset | | | | µA |
| $I_{OFF\_RAMOFF\_GPIO}$ | System OFF, No RAM retention, Wake on GPIO | | | | µA |
| $I_{OFF\_RAMOFF\_LPCOMP}$ | System OFF, No RAM retention, Wake on LPCOMP | | | | µA |
| $I_{OFF\_RAMOFF\_NFC}$ | System OFF, No RAM retention, Wake on NFC field | | | | µA |
| $I_{OFF\_RAMON\_RESET}$ | System OFF, Full RAM retention, Wake on reset | | | | µA |

### Current consumption: Serial interfaces

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{SPIM,IDLE}$ | SPIM Idle (enabled, no ongoing data transfer) | | | | mA |
| $I_{SPIM,ACTIVE}$ | SPIM R+W data transfer, 1 MHz SCK frequency, Clock = HFINT | | | | mA |
| $I_{SPIS,IDLE}$ | SPIS Idle (enabled, started, no activity on CSN, CLK, MISO or MOSI) | | | | mA |
| $I_{SPIS,ACTIVE}$ | SPIS R+W data transfer, 1 MHz SCK frequency, Clock = HFINT | | | | mA |
| $I_{TWIM,IDLE}$ | TWIM Idle (enabled, no ongoing data transfer) | | | | mA |
| $I_{TWIM,ACTIVE}$ | SPIM data transfer @ 400 kb/s, Clock = HFINT | | | | mA |
| $I_{TWIS,IDLE}$ | SPIS Idle (enabled, no ongoing data transfer, PREPARETX and/or PREPARERX tasks triggered) | | | | mA |
| $I_{TWIS,ACTIVE}$ | SPIM data transfer @ 400 kb/s, Clock = HFINT | | | | mA |

### Current consumption: CPU

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{CPU0}$ | CPU running from Flash, Clock = HFXO | | | | mA |
| $I_{CPU1}$ | CPU running from RAM, Clock = HFXO | | | | mA |
| $I_{CPU2}$ | CPU running from Flash, Clock = HFINT | | | | mA |

# 19 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port might vary with product variant and package. Refer to *Registers* on page 156 and *Pin assignments* on page 13 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, `PIN0` through `PIN31`. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER — Power supply* on page 66 chapter for more information about retained registers.

## 19.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. This mechanism is functional in both ON and OFF mode.

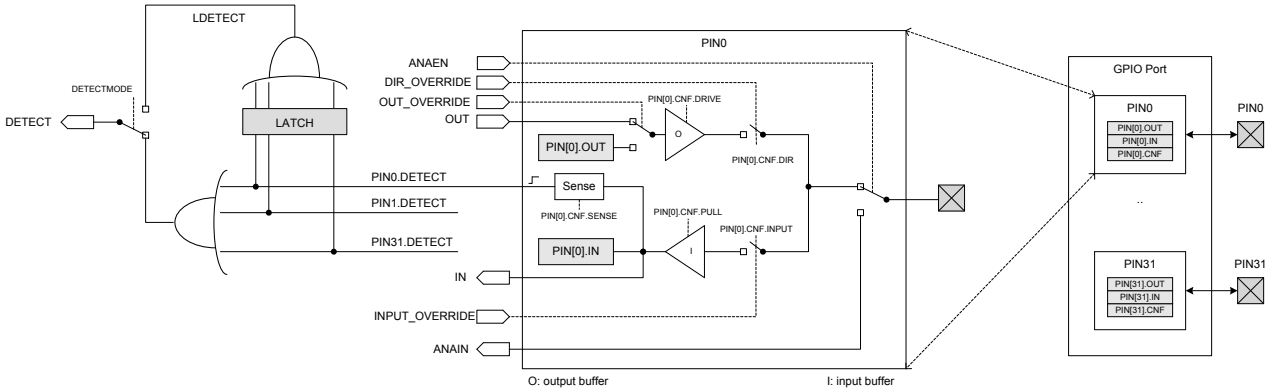



**Figure 22: GPIO Port and the GPIO pin details**

*Figure 22: GPIO Port and the GPIO pin details* on page 155 illustrates the GPIO port containing 32 individual pins, where `PIN0` is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE — GPIO tasks and events* on page 200.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 23: DETECT signal behavior* on page 156.

> **Important:** The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. *Figure 23: DETECT signal behavior* on page 156 illustrates the DETECT signals behaviour for these two alternatives.

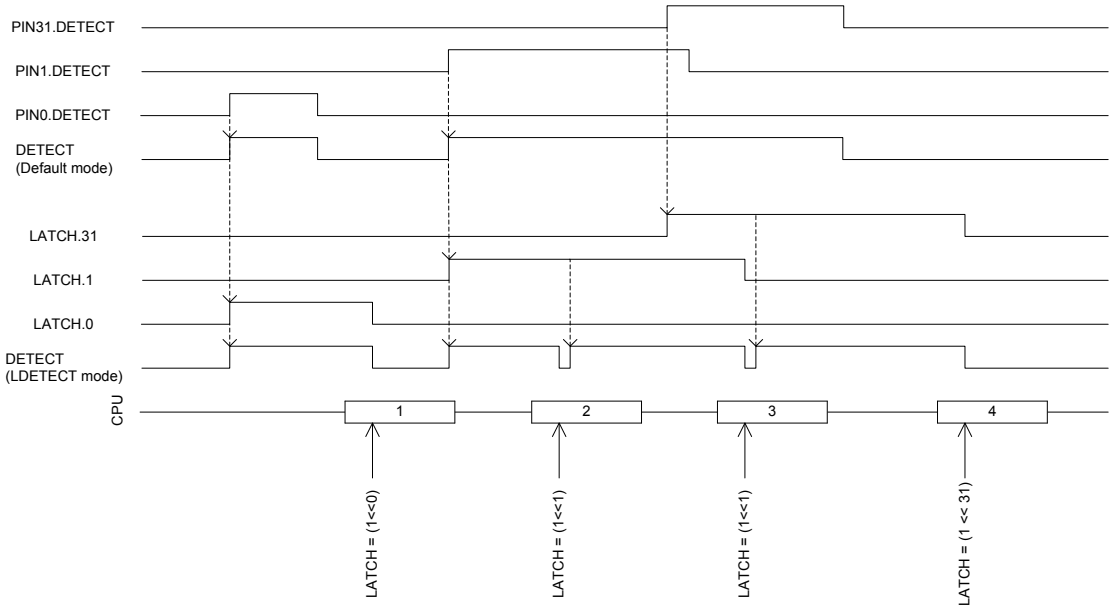



**Figure 23: DETECT signal behavior**

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 22: GPIO Port and the GPIO pin details* on page 155.

Selected pins also support analog input signals, see ANAIN in *Figure 22: GPIO Port and the GPIO pin details* on page 155. The assignment of the analog pins can be found in *Pin assignments* on page 13.

> **Important:** When a pin is configured as digital input, care has been taken in the nRF52840 design to minimize increased current consumption when the input voltage is between $V_{IL}$ and $V_{IH}$. However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between $V_{IL}$ and $V_{IH}$ for a long period of time.

## 19.2 GPIO located near the RADIO

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Refer to *Pin assignments* on page 13 for recommended usage guidelines to maximize radio performance in an application.

## 19.3 Registers

**Table 21: Instances**

| Base address | Peripheral | Instance | Description | Configuration | |
|---|---|---|---|---|---|
| 0x50000000 | GPIO | GPIO | General purpose input and output | | Deprecated |
| 0x50000000 | GPIO | P0 | General purpose input and output, port 0 | P0.00 to P0.31 implemented | |
| 0x50000300 | GPIO | P1 | General purpose input and output, port 1 | P1.00 to P1.15 implemented | |

### Table 22: Register Overview

| Register | Offset | Description |
|---|---|---|
| *OUT* | 0x504 | Write GPIO port |
| *OUTSET* | 0x508 | Set individual bits in GPIO port |
| *OUTCLR* | 0x50C | Clear individual bits in GPIO port |
| *IN* | 0x510 | Read GPIO port |
| *DIR* | 0x514 | Direction of GPIO pins |
| *DIRSET* | 0x518 | DIR set register |
| *DIRCLR* | 0x51C | DIR clear register |
| *LATCH* | 0x520 | Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers |
| *DETECTMODE* | 0x524 | Select between default DETECT signal behaviour and LDETECT mode |
| *PIN_CNF[0]* | 0x700 | Configuration of GPIO pins |
| *PIN_CNF[1]* | 0x704 | Configuration of GPIO pins |
| *PIN_CNF[2]* | 0x708 | Configuration of GPIO pins |
| *PIN_CNF[3]* | 0x70C | Configuration of GPIO pins |
| *PIN_CNF[4]* | 0x710 | Configuration of GPIO pins |
| *PIN_CNF[5]* | 0x714 | Configuration of GPIO pins |
| *PIN_CNF[6]* | 0x718 | Configuration of GPIO pins |
| *PIN_CNF[7]* | 0x71C | Configuration of GPIO pins |
| *PIN_CNF[8]* | 0x720 | Configuration of GPIO pins |
| *PIN_CNF[9]* | 0x724 | Configuration of GPIO pins |
| *PIN_CNF[10]* | 0x728 | Configuration of GPIO pins |
| *PIN_CNF[11]* | 0x72C | Configuration of GPIO pins |
| *PIN_CNF[12]* | 0x730 | Configuration of GPIO pins |
| *PIN_CNF[13]* | 0x734 | Configuration of GPIO pins |
| *PIN_CNF[14]* | 0x738 | Configuration of GPIO pins |
| *PIN_CNF[15]* | 0x73C | Configuration of GPIO pins |
| *PIN_CNF[16]* | 0x740 | Configuration of GPIO pins |
| *PIN_CNF[17]* | 0x744 | Configuration of GPIO pins |
| *PIN_CNF[18]* | 0x748 | Configuration of GPIO pins |
| *PIN_CNF[19]* | 0x74C | Configuration of GPIO pins |
| *PIN_CNF[20]* | 0x750 | Configuration of GPIO pins |
| *PIN_CNF[21]* | 0x754 | Configuration of GPIO pins |
| *PIN_CNF[22]* | 0x758 | Configuration of GPIO pins |
| *PIN_CNF[23]* | 0x75C | Configuration of GPIO pins |
| *PIN_CNF[24]* | 0x760 | Configuration of GPIO pins |
| *PIN_CNF[25]* | 0x764 | Configuration of GPIO pins |
| *PIN_CNF[26]* | 0x768 | Configuration of GPIO pins |
| *PIN_CNF[27]* | 0x76C | Configuration of GPIO pins |
| *PIN_CNF[28]* | 0x770 | Configuration of GPIO pins |
| *PIN_CNF[29]* | 0x774 | Configuration of GPIO pins |
| *PIN_CNF[30]* | 0x778 | Configuration of GPIO pins |
| *PIN_CNF[31]* | 0x77C | Configuration of GPIO pins |

## 19.3.1 OUT

Address offset: 0x504

Write GPIO port

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| d | RW | PIN29 | | | Pin 29 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Set | 1 | Write: writing a '1' sets the pin high; writing a '0' has no effect |
| e | RW | PIN30 | | | Pin 30 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Set | 1 | Write: writing a '1' sets the pin high; writing a '0' has no effect |
| f | RW | PIN31 | | | Pin 31 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Set | 1 | Write: writing a '1' sets the pin high; writing a '0' has no effect |

### 19.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port

Read: reads value of OUT register.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN0 | | | Pin 0 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| B | RW | PIN1 | | | Pin 1 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| C | RW | PIN2 | | | Pin 2 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| D | RW | PIN3 | | | Pin 3 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| E | RW | PIN4 | | | Pin 4 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| F | RW | PIN5 | | | Pin 5 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| G | RW | PIN6 | | | Pin 6 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |
| H | RW | PIN7 | | | Pin 7 |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.4 IN

Address offset: 0x510

Read GPIO port

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | R | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | R | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | R | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | R | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | R | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | R | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | R | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | R | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | R | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | R | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | R | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | R | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | R | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | R | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | R | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | R | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | R | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | R | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | R | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | R | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | R | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | R | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | R | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | R | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | R | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | R | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | R | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | R | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | R | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.5 DIR

Address offset: 0x514

Direction of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Set as output pin 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Read: pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Read: pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write: writing a '1' sets pin to output; writing a '0' has no effect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Set as output pin 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Read: pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Read: pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write: writing a '1' sets pin to output; writing a '0' has no effect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Set as output pin 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | Set | 1 | Write: writing a '1' sets pin to output; writing a '0' has no effect |
| e | RW | PIN30 | | | Set as output pin 30 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Set | 1 | Write: writing a '1' sets pin to output; writing a '0' has no effect |
| f | RW | PIN31 | | | Set as output pin 31 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Set | 1 | Write: writing a '1' sets pin to output; writing a '0' has no effect |

## 19.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN0 | | | Set as input pin 0 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| B | RW | PIN1 | | | Set as input pin 1 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| C | RW | PIN2 | | | Set as input pin 2 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| D | RW | PIN3 | | | Set as input pin 3 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| E | RW | PIN4 | | | Set as input pin 4 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| F | RW | PIN5 | | | Set as input pin 5 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| G | RW | PIN6 | | | Set as input pin 6 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| H | RW | PIN7 | | | Set as input pin 7 |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |
| I | RW | PIN8 | | | Set as input pin 8 |
| | | | Input | 0 | Read: pin set as input |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | PIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | PIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | PIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | PIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PIN9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PIN10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PIN11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | PIN12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | PIN13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | PIN14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | PIN15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | PIN16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | PIN17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | PIN18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PIN19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PIN20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | PIN21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | PIN22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | PIN23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | PIN24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PIN25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | PIN26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | PIN27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | PIN28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | PIN29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | PIN30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | PIN31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLatched | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Latched | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DETECTMODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Default | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LDETECT | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.10 PIN_CNF[0]

Address offset: 0x700

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.12 PIN_CNF[2]

Address offset: 0x708

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.13 PIN_CNF[3]

Address offset: 0x70C

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | D0H1 | | | | | | | | 5 | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | |
| | | | S0D1 | | | | | | | | 6 | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | |
| | | | H0D1 | | | | | | | | 7 | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | |
| | | | High | | | | | | | | 2 | | | | | | | | | | | | | | | | Sense for high level | | | | | | | |
| | | | Low | | | | | | | | 3 | | | | | | | | | | | | | | | | Sense for low level | | | | | | | |

## 19.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register | | | | | | | |
| | | | Input | | | | | | | | 0 | | | | | | | | | | | | | | | | Configure pin as an input pin | | | | | | | |
| | | | Output | | | | | | | | 1 | | | | | | | | | | | | | | | | Configure pin as an output pin | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer | | | | | | | |
| | | | Connect | | | | | | | | 0 | | | | | | | | | | | | | | | | Connect input buffer | | | | | | | |
| | | | Disconnect | | | | | | | | 1 | | | | | | | | | | | | | | | | Disconnect input buffer | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | No pull | | | | | | | |
| | | | Pulldown | | | | | | | | 1 | | | | | | | | | | | | | | | | Pull down on pin | | | | | | | |
| | | | Pullup | | | | | | | | 3 | | | | | | | | | | | | | | | | Pull up on pin | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration | | | | | | | |
| | | | S0S1 | | | | | | | | 0 | | | | | | | | | | | | | | | | Standard '0', standard '1' | | | | | | | |
| | | | H0S1 | | | | | | | | 1 | | | | | | | | | | | | | | | | High drive '0', standard '1' | | | | | | | |
| | | | S0H1 | | | | | | | | 2 | | | | | | | | | | | | | | | | Standard '0', high drive '1' | | | | | | | |
| | | | H0H1 | | | | | | | | 3 | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' | | | | | | | |
| | | | D0S1 | | | | | | | | 4 | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | |
| | | | D0H1 | | | | | | | | 5 | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | |
| | | | S0D1 | | | | | | | | 6 | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | |
| | | | H0D1 | | | | | | | | 7 | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | |
| | | | High | | | | | | | | 2 | | | | | | | | | | | | | | | | Sense for high level | | | | | | | |
| | | | Low | | | | | | | | 3 | | | | | | | | | | | | | | | | Sense for low level | | | | | | | |

## 19.3.15 PIN_CNF[5]

Address offset: 0x714

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.16 PIN_CNF[6]

Address offset: 0x718

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.18 PIN_CNF[8]

Address offset: 0x720

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.19 PIN_CNF[9]

Address offset: 0x724

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin direction. Same physical register as DIR register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.21 PIN_CNF[11]

Address offset: 0x72C

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disabled |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for high level |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for low level |

## 19.3.22 PIN_CNF[12]

Address offset: 0x730

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin direction. Same physical register as DIR register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.24 PIN_CNF[14]

Address offset: 0x738

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disabled |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for high level |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for low level |

## 19.3.25 PIN_CNF[15]

Address offset: 0x73C

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin direction. Same physical register as DIR register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.27 PIN_CNF[17]

Address offset: 0x744

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.28 PIN_CNF[18]

Address offset: 0x748

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.29 PIN_CNF[19]

Address offset: 0x74C

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin direction. Same physical register as DIR register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.30 PIN_CNF[20]

Address offset: 0x750

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.31 PIN_CNF[21]

Address offset: 0x754

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.33 PIN_CNF[23]

Address offset: 0x75C

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.34 PIN_CNF[24]

Address offset: 0x760

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | D0H1 | | | | | | | | 5 | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | |
| | | | S0D1 | | | | | | | | 6 | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | |
| | | | H0D1 | | | | | | | | 7 | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | |
| | | | High | | | | | | | | 2 | | | | | | | | | | | | | | | | Sense for high level | | | | | | | |
| | | | Low | | | | | | | | 3 | | | | | | | | | | | | | | | | Sense for low level | | | | | | | |

## 19.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register | | | | | | | |
| | | | Input | | | | | | | | 0 | | | | | | | | | | | | | | | | Configure pin as an input pin | | | | | | | |
| | | | Output | | | | | | | | 1 | | | | | | | | | | | | | | | | Configure pin as an output pin | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer | | | | | | | |
| | | | Connect | | | | | | | | 0 | | | | | | | | | | | | | | | | Connect input buffer | | | | | | | |
| | | | Disconnect | | | | | | | | 1 | | | | | | | | | | | | | | | | Disconnect input buffer | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | No pull | | | | | | | |
| | | | Pulldown | | | | | | | | 1 | | | | | | | | | | | | | | | | Pull down on pin | | | | | | | |
| | | | Pullup | | | | | | | | 3 | | | | | | | | | | | | | | | | Pull up on pin | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration | | | | | | | |
| | | | S0S1 | | | | | | | | 0 | | | | | | | | | | | | | | | | Standard '0', standard '1' | | | | | | | |
| | | | H0S1 | | | | | | | | 1 | | | | | | | | | | | | | | | | High drive '0', standard '1' | | | | | | | |
| | | | S0H1 | | | | | | | | 2 | | | | | | | | | | | | | | | | Standard '0', high drive '1' | | | | | | | |
| | | | H0H1 | | | | | | | | 3 | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' | | | | | | | |
| | | | D0S1 | | | | | | | | 4 | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | |
| | | | D0H1 | | | | | | | | 5 | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | |
| | | | S0D1 | | | | | | | | 6 | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | |
| | | | H0D1 | | | | | | | | 7 | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism | | | | | | | |
| | | | Disabled | | | | | | | | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | |
| | | | High | | | | | | | | 2 | | | | | | | | | | | | | | | | Sense for high level | | | | | | | |
| | | | Low | | | | | | | | 3 | | | | | | | | | | | | | | | | Sense for low level | | | | | | | |

## 19.3.36 PIN_CNF[26]

Address offset: 0x768

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', disconnect '1' (normally used for wired-and connections) |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin sensing mechanism |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disabled |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for high level |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Sense for low level |

## 19.3.37 PIN_CNF[27]

Address offset: 0x76C

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pin direction. Same physical register as DIR register |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an input pin |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Configure pin as an output pin |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect or disconnect input buffer |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connect input buffer |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect input buffer |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull configuration |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | No pull |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull down on pin |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull up on pin |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Drive configuration |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', standard '1' |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', standard '1' |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Standard '0', high drive '1' |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect '0' standard '1' (normally used for wired-or connections) |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.39 PIN_CNF[29]

Address offset: 0x774

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.3.40 PIN_CNF[30]

Address offset: 0x778

Configuration of GPIO pins

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 19.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | E | E | | | | | | D | D | D | | | | | C | C | B | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an input pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure pin as an output pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | INPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect or disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connect | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Connect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnect | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect input buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PULL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No pull | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull down on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pull up on pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DRIVE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Drive configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0S1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0S1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', standard '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0H1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0', high drive '1' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0H1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', high 'drive '1'' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0S1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0' standard '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | D0H1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disconnect '0', high drive '1' (normally used for wired-or connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | S0D1 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Standard '0'. disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | H0D1 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | High drive '0', disconnect '1' (normally used for wired-and connections) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pin sensing mechanism | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for high level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sense for low level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 19.4 Electrical specification

### 19.4.1 GPIO Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7 x VDD | | VDD | V |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | VSS | | 0.3 x VDD | V |
| $V_{OH,SD}$ | Output high voltage, standard drive, 0.5 mA, VDD ≥1.7 | VDD-0.4 | | VDD | V |
| $V_{OH,HDH}$ | Output high voltage, high drive, 5 mA, VDD >= 2.7 V | VDD-0.4 | | VDD | V |
| $V_{OH,HDL}$ | Output high voltage, high drive, 3 mA, VDD >= 1.7 V | VDD-0.4 | | VDD | V |
| $V_{OL,SD}$ | Output low voltage, standard drive, 0.5 mA, VDD ≥1.7 | VSS | | VSS+0.4 | V |
| $V_{OL,HDH}$ | Output low voltage, high drive, 5 mA, VDD >= 2.7 V | VSS | | VSS+0.4 | V |
| $V_{OL,HDL}$ | Output low voltage, high drive, 3 mA, VDD >= 1.7 V | VSS | | VSS+0.4 | V |
| $I_{OL,SD}$ | Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7 | 1 | 2 | 4 | mA |
| $I_{OL,HDH}$ | Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V | 6 | 10 | 15 | mA |
| $I_{OL,HDL}$ | Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V | 3 | | | mA |
| $I_{OH,SD}$ | Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7 | 1 | 2 | 4 | mA |
| $I_{OH,HDH}$ | Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V | 6 | 9 | 14 | mA |
| $I_{OH,HDL}$ | Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V | 3 | | | mA |
| $t_{RF,15pF}$ | Rise/fall time, standard drive mode, 10-90%, 15 pF load[1] | | 9 | | ns |
| $t_{RF,25pF}$ | Rise/fall time, standard drive mode, 10-90%, 25 pF load[1] | | 13 | | ns |
| $t_{RF,50pF}$ | Rise/fall time, standard drive mode, 10-90%, 50 pF load[1] | | 25 | | ns |
| $t_{HRF,15pF}$ | Rise/Fall time, high drive mode, 10-90%, 15 pF load[1] | | 4 | | ns |
| $t_{HRF,25pF}$ | Rise/Fall time, high drive mode, 10-90%, 25 pF load[1] | | 5 | | ns |
| $t_{HRF,50pF}$ | Rise/Fall time, high drive mode, 10-90%, 50 pF load[1] | | 8 | | ns |
| $R_{PU}$ | Pull-up resistance | 11 | 13 | 16 | kΩ |
| $R_{PD}$ | Pull-down resistance | 11 | 13 | 16 | kΩ |
| $C_{PAD}$ | Pad capacitance | | 3 | | pF |
| $C_{PAD\_NFC}$ | Pad capacitance on NFC pads | | 4 | | pF |
| $I_{NFC\_LEAK}$ | Leakage current between NFC pads when driven to different states | | 1 | 4 | µA |

The current drawn from the battery when GPIO is active as an output is calculated as follows:

$I_{GPIO}=V_{DD}\ C_{load}\ f$

$C_{load}$ being the load capacitance and “f” is the switching frequency.

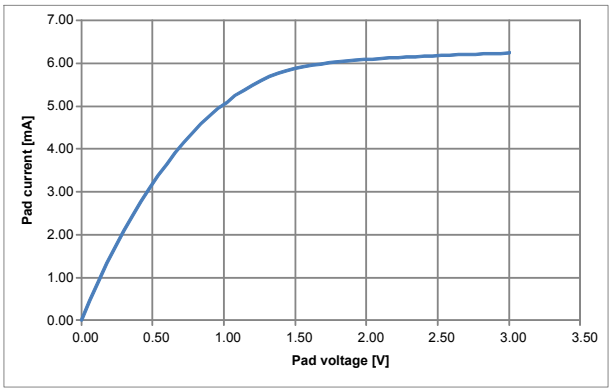



**Figure 24: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V**

[1] Rise and fall times based on simulations

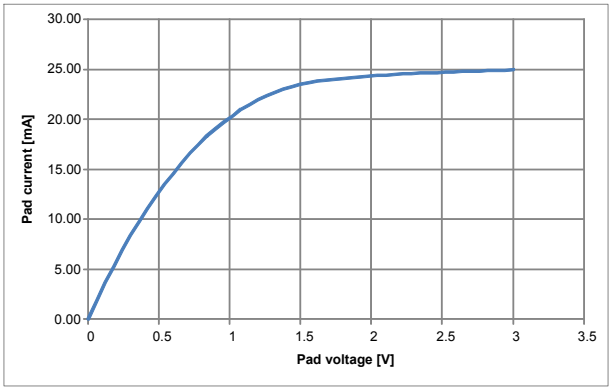



**Figure 25: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V**

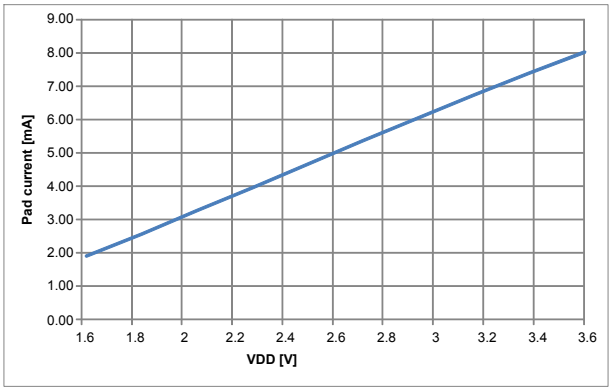



**Figure 26: Max sink current vs Voltage, standard drive**

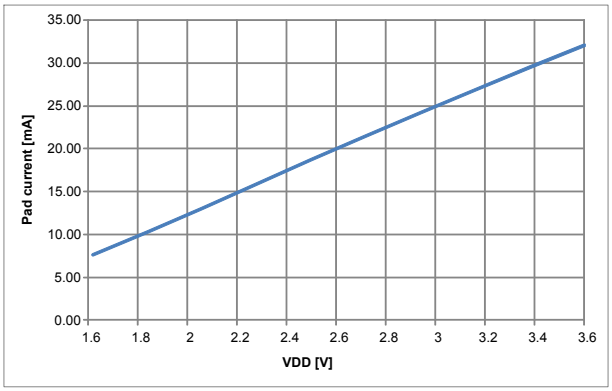



**Figure 27: Max sink current vs Voltage, high drive**

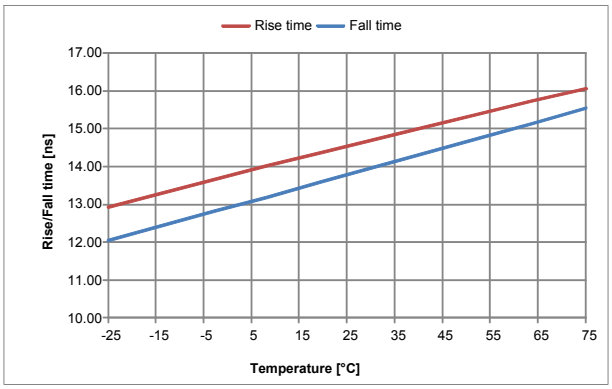



**Figure 28: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V**

# 20 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

**Table 23: GPIOTE properties**

| Instance | Number of GPIOTE channels |
|---|---|
| GPIOTE | 8 |

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change

## 20.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY , and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 24: Task priorities* on page 200.

**Table 24: Task priorities**

| Priority | Task |
|---|---|
| 1 | OUT |
| 2 | CLR |
| 3 | SET |

When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

## 20.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO — General purpose input/output* on page 154 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 154.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

## 20.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

## 20.4 Registers

### Table 25: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40006000 | GPIOTE | GPIOTE | GPIO tasks and events | |

### Table 26: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_OUT[0] | 0x000 | Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in CONFIG[0].POLARITY. |
| TASKS_OUT[1] | 0x004 | Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in CONFIG[1].POLARITY. |

| Register | Offset | Description |
|---|---|---|
| TASKS_OUT[2] | 0x008 | Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in CONFIG[2].POLARITY. |
| TASKS_OUT[3] | 0x00C | Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in CONFIG[3].POLARITY. |
| TASKS_OUT[4] | 0x010 | Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is configured in CONFIG[4].POLARITY. |
| TASKS_OUT[5] | 0x014 | Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is configured in CONFIG[5].POLARITY. |
| TASKS_OUT[6] | 0x018 | Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is configured in CONFIG[6].POLARITY. |
| TASKS_OUT[7] | 0x01C | Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is configured in CONFIG[7].POLARITY. |
| TASKS_SET[0] | 0x030 | Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it high. |
| TASKS_SET[1] | 0x034 | Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it high. |
| TASKS_SET[2] | 0x038 | Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high. |
| TASKS_SET[3] | 0x03C | Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high. |
| TASKS_SET[4] | 0x040 | Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high. |
| TASKS_SET[5] | 0x044 | Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high. |
| TASKS_SET[6] | 0x048 | Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high. |
| TASKS_SET[7] | 0x04C | Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high. |
| TASKS_CLR[0] | 0x060 | Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low. |
| TASKS_CLR[1] | 0x064 | Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low. |
| TASKS_CLR[2] | 0x068 | Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. |
| TASKS_CLR[3] | 0x06C | Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. |
| TASKS_CLR[4] | 0x070 | Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. |
| TASKS_CLR[5] | 0x074 | Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. |
| TASKS_CLR[6] | 0x078 | Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. |
| TASKS_CLR[7] | 0x07C | Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. |
| EVENTS_IN[0] | 0x100 | Event generated from pin specified in CONFIG[0].PSEL |
| EVENTS_IN[1] | 0x104 | Event generated from pin specified in CONFIG[1].PSEL |
| EVENTS_IN[2] | 0x108 | Event generated from pin specified in CONFIG[2].PSEL |
| EVENTS_IN[3] | 0x10C | Event generated from pin specified in CONFIG[3].PSEL |
| EVENTS_IN[4] | 0x110 | Event generated from pin specified in CONFIG[4].PSEL |
| EVENTS_IN[5] | 0x114 | Event generated from pin specified in CONFIG[5].PSEL |
| EVENTS_IN[6] | 0x118 | Event generated from pin specified in CONFIG[6].PSEL |
| EVENTS_IN[7] | 0x11C | Event generated from pin specified in CONFIG[7].PSEL |
| EVENTS_PORT | 0x17C | Event generated from multiple input GPIO pins with SENSE mechanism enabled |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *CONFIG[0]* | 0x510 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[1]* | 0x514 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[2]* | 0x518 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[3]* | 0x51C | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[4]* | 0x520 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[5]* | 0x524 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[6]* | 0x528 | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |
| *CONFIG[7]* | 0x52C | Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event |

## 20.4.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | IN0 | | | Write '1' to Enable interrupt for IN[0] event |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | I | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_IN[0]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | IN1 | | | Write '1' to Enable interrupt for IN[1] event |
| | | | | | See *EVENTS_IN[1]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | IN2 | | | Write '1' to Enable interrupt for IN[2] event |
| | | | | | See *EVENTS_IN[2]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | IN3 | | | Write '1' to Enable interrupt for IN[3] event |
| | | | | | See *EVENTS_IN[3]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | IN4 | | | Write '1' to Enable interrupt for IN[4] event |
| | | | | | See *EVENTS_IN[4]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | IN5 | | | Write '1' to Enable interrupt for IN[5] event |
| | | | | | See *EVENTS_IN[5]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | IN6 | | | Write '1' to Enable interrupt for IN[6] event |
| | | | | | See *EVENTS_IN[6]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | IN7 | | | Write '1' to Enable interrupt for IN[7] event |
| | | | | | See *EVENTS_IN[7]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | PORT | | | Write '1' to Enable interrupt for PORT event |
| | | | | | See *EVENTS_PORT* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 20.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | I | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | IN0 | | | Write '1' to Disable interrupt for IN[0] event<br><br>See *EVENTS_IN[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | IN1 | | | Write '1' to Disable interrupt for IN[1] event<br><br>See *EVENTS_IN[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | IN2 | | | Write '1' to Disable interrupt for IN[2] event<br><br>See *EVENTS_IN[2]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | IN3 | | | Write '1' to Disable interrupt for IN[3] event<br><br>See *EVENTS_IN[3]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | IN4 | | | Write '1' to Disable interrupt for IN[4] event<br><br>See *EVENTS_IN[4]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | IN5 | | | Write '1' to Disable interrupt for IN[5] event<br><br>See *EVENTS_IN[5]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | IN6 | | | Write '1' to Disable interrupt for IN[6] event<br><br>See *EVENTS_IN[6]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | IN7 | | | Write '1' to Disable interrupt for IN[7] event<br><br>See *EVENTS_IN[7]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | PORT | | | Write '1' to Disable interrupt for PORT event<br><br>See *EVENTS_PORT* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 20.4.3 CONFIG[0]

Address offset: 0x510

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.4 CONFIG[1]

Address offset: 0x514

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.5 CONFIG[2]

Address offset: 0x518

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Event mode<br><br>The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode<br><br>The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Event mode<br><br>The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode<br><br>The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.7 CONFIG[4]

Address offset: 0x520

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.8 CONFIG[5]

Address offset: 0x524

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.9 CONFIG[6]

Address offset: 0x528

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Event mode<br><br>The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode<br><br>The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | D | D | | | C | B | B | B | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Event | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Event mode<br><br>The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode<br><br>The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PSEL | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | POLARITY | | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | None | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LoToHi | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HiToLo | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Toggle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUTINIT | | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Task mode: Initial value of pin before task triggering is high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 20.5 Electrical specification

### 20.5.1 GPIOTE Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{GPIOTE,IN}$ | Run current with 1 or more GPIOTE active channels in Input mode, System On Idle | | | | µA |
| $I_{GPIOTE,OUT}$ | Run current with 1 or more GPIOTE active channels in Output mode, System On Idle | | | | µA |
| $I_{GPIOTE,IDLE}$ | Run current when all channels in Idle mode. | | | | µA |

# 21 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

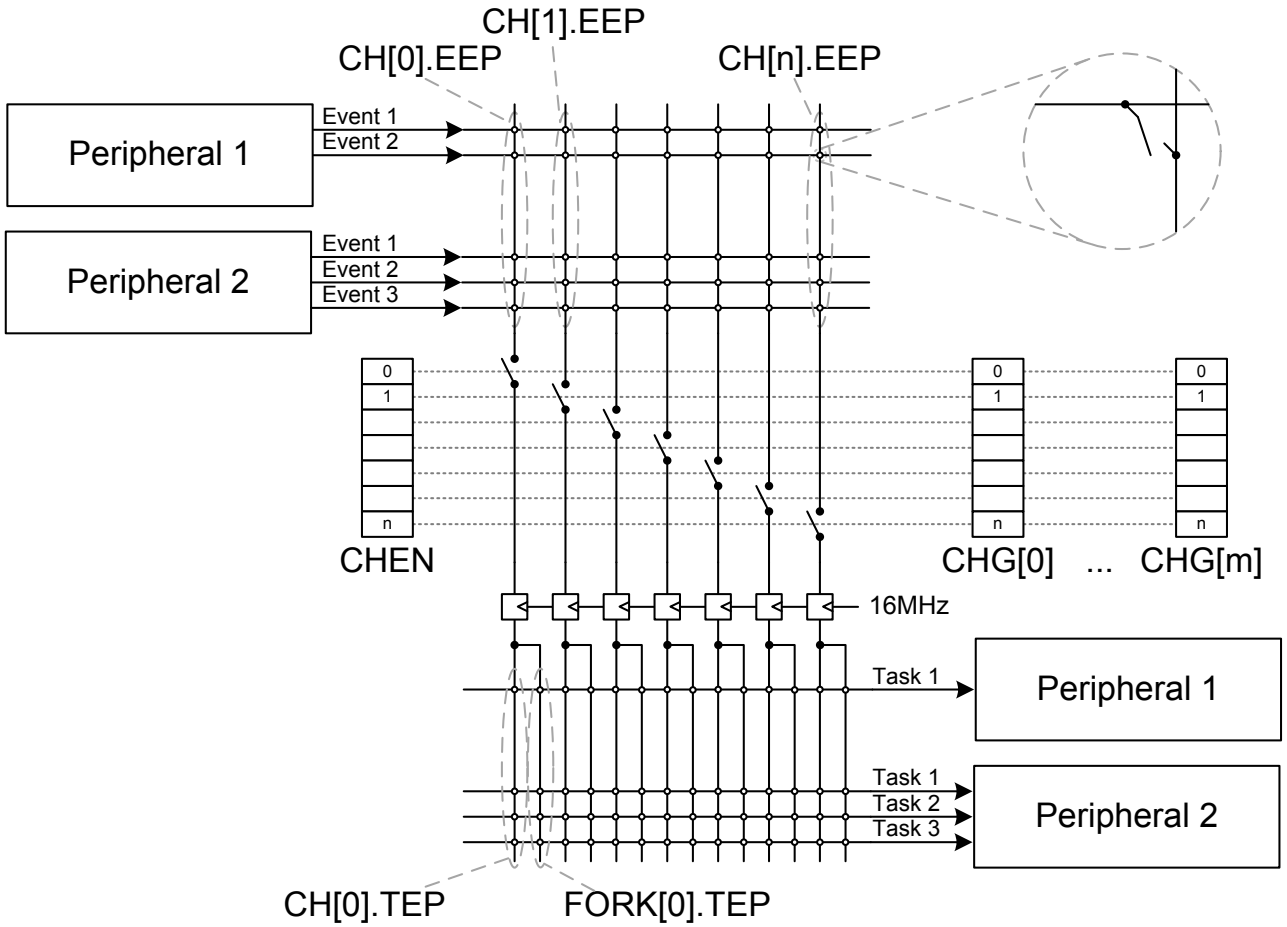



**Figure 29: PPI block diagram**

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

**Table 27: Configurable and fixed PPI channels**

| Instance | Channel | Number of channels | Number of groups |
|---|---|---|---|
| PPI | 0-19 | 20 | 6 |
| PPI (fixed) | 20-31 | 12 | |

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.

Note that shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks. Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

## 21.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

**Table 28: Pre-programmed channels**

| Channel | EEP | TEP |
|---|---|---|
| 20 | TIMER0->EVENTS_COMPARE[0] | RADIO->TASKS_TXEN |
| 21 | TIMER0->EVENTS_COMPARE[0] | RADIO->TASKS_RXEN |
| 22 | TIMER0->EVENTS_COMPARE[1] | RADIO->TASKS_DISABLE |
| 23 | RADIO->EVENTS_BCMATCH | AAR->TASKS_START |
| 24 | RADIO->EVENTS_READY | CCM->TASKS_KSGEN |
| 25 | RADIO->EVENTS_ADDRESS | CCM->TASKS_CRYPT |
| 26 | RADIO->EVENTS_ADDRESS | TIMER0->TASKS_CAPTURE[1] |
| 27 | RADIO->EVENTS_END | TIMER0->TASKS_CAPTURE[2] |
| 28 | RTC0->EVENTS_COMPARE[0] | RADIO->TASKS_TXEN |
| 29 | RTC0->EVENTS_COMPARE[0] | RADIO->TASKS_RXEN |
| 30 | RTC0->EVENTS_COMPARE[0] | TIMER0->TASKS_CLEAR |
| 31 | RTC0->EVENTS_COMPARE[0] | TIMER0->TASKS_START |

## 21.2 Registers

**Table 29: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4001F000 | PPI | PPI | Programmable peripheral interconnect | |

**Table 30: Register Overview**

| Register | Offset | Description |
|---|---|---|
| TASKS_CHG[0].EN | 0x000 | Enable channel group 0 |
| TASKS_CHG[0].DIS | 0x004 | Disable channel group 0 |
| TASKS_CHG[1].EN | 0x008 | Enable channel group 1 |
| TASKS_CHG[1].DIS | 0x00C | Disable channel group 1 |
| TASKS_CHG[2].EN | 0x010 | Enable channel group 2 |
| TASKS_CHG[2].DIS | 0x014 | Disable channel group 2 |
| TASKS_CHG[3].EN | 0x018 | Enable channel group 3 |
| TASKS_CHG[3].DIS | 0x01C | Disable channel group 3 |
| TASKS_CHG[4].EN | 0x020 | Enable channel group 4 |

| Register | Offset | Description |
|---|---|---|
| TASKS_CHG[4].DIS | 0x024 | Disable channel group 4 |
| TASKS_CHG[5].EN | 0x028 | Enable channel group 5 |
| TASKS_CHG[5].DIS | 0x02C | Disable channel group 5 |
| *CHEN* | 0x500 | Channel enable register |
| *CHENSET* | 0x504 | Channel enable set register |
| *CHENCLR* | 0x508 | Channel enable clear register |
| *CH[0].EEP* | 0x510 | Channel 0 event end-point |
| *CH[0].TEP* | 0x514 | Channel 0 task end-point |
| *CH[1].EEP* | 0x518 | Channel 1 event end-point |
| *CH[1].TEP* | 0x51C | Channel 1 task end-point |
| *CH[2].EEP* | 0x520 | Channel 2 event end-point |
| *CH[2].TEP* | 0x524 | Channel 2 task end-point |
| *CH[3].EEP* | 0x528 | Channel 3 event end-point |
| *CH[3].TEP* | 0x52C | Channel 3 task end-point |
| *CH[4].EEP* | 0x530 | Channel 4 event end-point |
| *CH[4].TEP* | 0x534 | Channel 4 task end-point |
| *CH[5].EEP* | 0x538 | Channel 5 event end-point |
| *CH[5].TEP* | 0x53C | Channel 5 task end-point |
| *CH[6].EEP* | 0x540 | Channel 6 event end-point |
| *CH[6].TEP* | 0x544 | Channel 6 task end-point |
| *CH[7].EEP* | 0x548 | Channel 7 event end-point |
| *CH[7].TEP* | 0x54C | Channel 7 task end-point |
| *CH[8].EEP* | 0x550 | Channel 8 event end-point |
| *CH[8].TEP* | 0x554 | Channel 8 task end-point |
| *CH[9].EEP* | 0x558 | Channel 9 event end-point |
| *CH[9].TEP* | 0x55C | Channel 9 task end-point |
| *CH[10].EEP* | 0x560 | Channel 10 event end-point |
| *CH[10].TEP* | 0x564 | Channel 10 task end-point |
| *CH[11].EEP* | 0x568 | Channel 11 event end-point |
| *CH[11].TEP* | 0x56C | Channel 11 task end-point |
| *CH[12].EEP* | 0x570 | Channel 12 event end-point |
| *CH[12].TEP* | 0x574 | Channel 12 task end-point |
| *CH[13].EEP* | 0x578 | Channel 13 event end-point |
| *CH[13].TEP* | 0x57C | Channel 13 task end-point |
| *CH[14].EEP* | 0x580 | Channel 14 event end-point |
| *CH[14].TEP* | 0x584 | Channel 14 task end-point |
| *CH[15].EEP* | 0x588 | Channel 15 event end-point |
| *CH[15].TEP* | 0x58C | Channel 15 task end-point |
| *CH[16].EEP* | 0x590 | Channel 16 event end-point |
| *CH[16].TEP* | 0x594 | Channel 16 task end-point |
| *CH[17].EEP* | 0x598 | Channel 17 event end-point |
| *CH[17].TEP* | 0x59C | Channel 17 task end-point |
| *CH[18].EEP* | 0x5A0 | Channel 18 event end-point |
| *CH[18].TEP* | 0x5A4 | Channel 18 task end-point |
| *CH[19].EEP* | 0x5A8 | Channel 19 event end-point |
| *CH[19].TEP* | 0x5AC | Channel 19 task end-point |
| *CHG[0]* | 0x800 | Channel group 0 |
| *CHG[1]* | 0x804 | Channel group 1 |
| *CHG[2]* | 0x808 | Channel group 2 |
| *CHG[3]* | 0x80C | Channel group 3 |
| *CHG[4]* | 0x810 | Channel group 4 |
| *CHG[5]* | 0x814 | Channel group 5 |
| *FORK[0].TEP* | 0x910 | Channel 0 task end-point |
| *FORK[1].TEP* | 0x914 | Channel 1 task end-point |
| *FORK[2].TEP* | 0x918 | Channel 2 task end-point |
| *FORK[3].TEP* | 0x91C | Channel 3 task end-point |
| *FORK[4].TEP* | 0x920 | Channel 4 task end-point |
| *FORK[5].TEP* | 0x924 | Channel 5 task end-point |

| Register | Offset | Description |
|---|---|---|
| FORK[6].TEP | 0x928 | Channel 6 task end-point |
| FORK[7].TEP | 0x92C | Channel 7 task end-point |
| FORK[8].TEP | 0x930 | Channel 8 task end-point |
| FORK[9].TEP | 0x934 | Channel 9 task end-point |
| FORK[10].TEP | 0x938 | Channel 10 task end-point |
| FORK[11].TEP | 0x93C | Channel 11 task end-point |
| FORK[12].TEP | 0x940 | Channel 12 task end-point |
| FORK[13].TEP | 0x944 | Channel 13 task end-point |
| FORK[14].TEP | 0x948 | Channel 14 task end-point |
| FORK[15].TEP | 0x94C | Channel 15 task end-point |
| FORK[16].TEP | 0x950 | Channel 16 task end-point |
| FORK[17].TEP | 0x954 | Channel 17 task end-point |
| FORK[18].TEP | 0x958 | Channel 18 task end-point |
| FORK[19].TEP | 0x95C | Channel 19 task end-point |
| FORK[20].TEP | 0x960 | Channel 20 task end-point |
| FORK[21].TEP | 0x964 | Channel 21 task end-point |
| FORK[22].TEP | 0x968 | Channel 22 task end-point |
| FORK[23].TEP | 0x96C | Channel 23 task end-point |
| FORK[24].TEP | 0x970 | Channel 24 task end-point |
| FORK[25].TEP | 0x974 | Channel 25 task end-point |
| FORK[26].TEP | 0x978 | Channel 26 task end-point |
| FORK[27].TEP | 0x97C | Channel 27 task end-point |
| FORK[28].TEP | 0x980 | Channel 28 task end-point |
| FORK[29].TEP | 0x984 | Channel 29 task end-point |
| FORK[30].TEP | 0x988 | Channel 30 task end-point |
| FORK[31].TEP | 0x98C | Channel 31 task end-point |

### 21.2.1 CHEN

Address offset: 0x500

Channel enable register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CH0 | | | Enable or disable channel 0 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| B | RW | CH1 | | | Enable or disable channel 1 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| C | RW | CH2 | | | Enable or disable channel 2 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| D | RW | CH3 | | | Enable or disable channel 3 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| E | RW | CH4 | | | Enable or disable channel 4 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| F | RW | CH5 | | | Enable or disable channel 5 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| G | RW | CH6 | | | Enable or disable channel 6 |
| | | | Disabled | 0 | Disable channel |
| | | | Enabled | 1 | Enable channel |
| H | RW | CH7 | | | Enable or disable channel 7 |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register

Read: reads value of CH{i} field in CHEN register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pointer to event register. Accepts only addresses to registers from the Event group.

## 21.2.5 CH[0].TEP

Address offset: 0x514

Channel 0 task end-point

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pointer to task register. Accepts only addresses to registers from the Task group.

## 21.2.6 CH[1].EEP

Address offset: 0x518

Channel 1 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.7 CH[1].TEP

Address offset: 0x51C

Channel 1 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.9 CH[2].TEP

Address offset: 0x524

Channel 2 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.11 CH[3].TEP

Address offset: 0x52C

Channel 3 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.13 CH[4].TEP

Address offset: 0x534

Channel 4 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.15 CH[5].TEP

Address offset: 0x53C

Channel 5 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.17 CH[6].TEP

Address offset: 0x544

Channel 6 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.19 CH[7].TEP

Address offset: 0x54C

Channel 7 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.21 CH[8].TEP

Address offset: 0x554

Channel 8 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.23 CH[9].TEP

Address offset: 0x55C

Channel 9 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register. Accepts only addresses to registers from the Task group. |

## 21.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | EEP | | | Pointer to event register. Accepts only addresses to registers from the Event group. |

## 21.2.41 CH[18].TEP

Address offset: 0x5A4

Channel 18 task end-point

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pointer to task register. Accepts only addresses to registers from the Task group.

## 21.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pointer to event register. Accepts only addresses to registers from the Event group.

## 21.2.43 CH[19].TEP

Address offset: 0x5AC

Channel 19 task end-point

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pointer to task register. Accepts only addresses to registers from the Task group.

## 21.2.44 CHG[0]

Address offset: 0x800

Channel group 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Include or exclude channel 0

Include or exclude channel 1

Include or exclude channel 2

Include or exclude channel 3

Include or exclude channel 4

Include or exclude channel 5

Include or exclude channel 6

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.45 CHG[1]

Address offset: 0x804

Channel group 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | Included | 1 | Include |
| I | RW | CH8 | | | Include or exclude channel 8 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| J | RW | CH9 | | | Include or exclude channel 9 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| K | RW | CH10 | | | Include or exclude channel 10 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| L | RW | CH11 | | | Include or exclude channel 11 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| M | RW | CH12 | | | Include or exclude channel 12 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| N | RW | CH13 | | | Include or exclude channel 13 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| O | RW | CH14 | | | Include or exclude channel 14 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| P | RW | CH15 | | | Include or exclude channel 15 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Q | RW | CH16 | | | Include or exclude channel 16 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| R | RW | CH17 | | | Include or exclude channel 17 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| S | RW | CH18 | | | Include or exclude channel 18 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| T | RW | CH19 | | | Include or exclude channel 19 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| U | RW | CH20 | | | Include or exclude channel 20 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| V | RW | CH21 | | | Include or exclude channel 21 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| W | RW | CH22 | | | Include or exclude channel 22 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| X | RW | CH23 | | | Include or exclude channel 23 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Y | RW | CH24 | | | Include or exclude channel 24 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Z | RW | CH25 | | | Include or exclude channel 25 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| a | RW | CH26 | | | Include or exclude channel 26 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| b | RW | CH27 | | | Include or exclude channel 27 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| c | RW | CH28 | | | Include or exclude channel 28 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| d | RW | CH29 | | | Include or exclude channel 29 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| e | RW | CH30 | | | Include or exclude channel 30 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| f | RW | CH31 | | | Include or exclude channel 31 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

## 21.2.46 CHG[2]

Address offset: 0x808

Channel group 2

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CH0 | | | Include or exclude channel 0 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| B | RW | CH1 | | | Include or exclude channel 1 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| C | RW | CH2 | | | Include or exclude channel 2 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| D | RW | CH3 | | | Include or exclude channel 3 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| E | RW | CH4 | | | Include or exclude channel 4 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| F | RW | CH5 | | | Include or exclude channel 5 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| G | RW | CH6 | | | Include or exclude channel 6 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| H | RW | CH7 | | | Include or exclude channel 7 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| I | RW | CH8 | | | Include or exclude channel 8 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.48 CHG[4]

Address offset: 0x810

Channel group 4

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CH0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CH1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CH3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CH4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | CH5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | Included | 1 | Include |
| M | RW | CH12 | | | Include or exclude channel 12 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| N | RW | CH13 | | | Include or exclude channel 13 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| O | RW | CH14 | | | Include or exclude channel 14 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| P | RW | CH15 | | | Include or exclude channel 15 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Q | RW | CH16 | | | Include or exclude channel 16 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| R | RW | CH17 | | | Include or exclude channel 17 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| S | RW | CH18 | | | Include or exclude channel 18 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| T | RW | CH19 | | | Include or exclude channel 19 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| U | RW | CH20 | | | Include or exclude channel 20 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| V | RW | CH21 | | | Include or exclude channel 21 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| W | RW | CH22 | | | Include or exclude channel 22 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| X | RW | CH23 | | | Include or exclude channel 23 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Y | RW | CH24 | | | Include or exclude channel 24 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| Z | RW | CH25 | | | Include or exclude channel 25 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| a | RW | CH26 | | | Include or exclude channel 26 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| b | RW | CH27 | | | Include or exclude channel 27 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| c | RW | CH28 | | | Include or exclude channel 28 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| d | RW | CH29 | | | Include or exclude channel 29 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| e | RW | CH30 | | | Include or exclude channel 30 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| f | RW | CH31 | | | Include or exclude channel 31 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

## 21.2.49 CHG[5]

Address offset: 0x814

Channel group 5

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CH0 | | | Include or exclude channel 0 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| B | RW | CH1 | | | Include or exclude channel 1 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| C | RW | CH2 | | | Include or exclude channel 2 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| D | RW | CH3 | | | Include or exclude channel 3 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| E | RW | CH4 | | | Include or exclude channel 4 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| F | RW | CH5 | | | Include or exclude channel 5 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| G | RW | CH6 | | | Include or exclude channel 6 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| H | RW | CH7 | | | Include or exclude channel 7 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| I | RW | CH8 | | | Include or exclude channel 8 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| J | RW | CH9 | | | Include or exclude channel 9 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| K | RW | CH10 | | | Include or exclude channel 10 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| L | RW | CH11 | | | Include or exclude channel 11 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |
| M | RW | CH12 | | | Include or exclude channel 12 |
| | | | Excluded | 0 | Exclude |
| | | | Included | 1 | Include |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | CH22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | CH23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | CH24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | CH25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | CH26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | CH27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | CH28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | CH29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | CH30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | CH31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0 | Exclude | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 1 | Include | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.50 FORK[0].TEP

Address offset: 0x910

Channel 0 task end-point

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | Pointer to task register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.51 FORK[1].TEP

Address offset: 0x914

Channel 1 task end-point

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | Pointer to task register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.52 FORK[2].TEP

Address offset: 0x918

Channel 2 task end-point

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | Pointer to task register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.53 FORK[3].TEP

Address offset: 0x91C

Channel 3 task end-point

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TEP | | | Pointer to task register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 21.2.54 FORK[4].TEP

Address offset: 0x920

Channel 4 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.55 FORK[5].TEP

Address offset: 0x924

Channel 5 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.56 FORK[6].TEP

Address offset: 0x928

Channel 6 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.57 FORK[7].TEP

Address offset: 0x92C

Channel 7 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.58 FORK[8].TEP

Address offset: 0x930

Channel 8 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.59 FORK[9].TEP

Address offset: 0x934

Channel 9 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

### 21.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

## 21.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TEP | | | Pointer to task register |

# 22 RADIO — 2.4 GHz Radio

The 2.4 GHz radio transceiver is compatible with multiple radio standards such as 1 Mbps, 2 Mbps and long range *Bluetooth*® low energy. IEEE 802.15.4 250 kbps mode is fully supported as well as Nordic's proprietary 1 Mbps and 2 Mbps modes of operation.

Listed here are main features for the RADIO:

- Multi-domain 2.4 GHz radio transceiver:
  - 1 Mbps, 2Mbps and long range (125kbps and 500kbps mode) *Bluetooth*® low energy modes
  - 250kbps IEEE 802.15.4 mode
  - 1Mbps and 2Mbps Nordic proprietary modes
- Best in class link budget and low power operation
- Efficient data interface with EasyDMA support
- Automatic address filtering and pattern matching

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 30: RADIO block diagram* on page 249 for details.

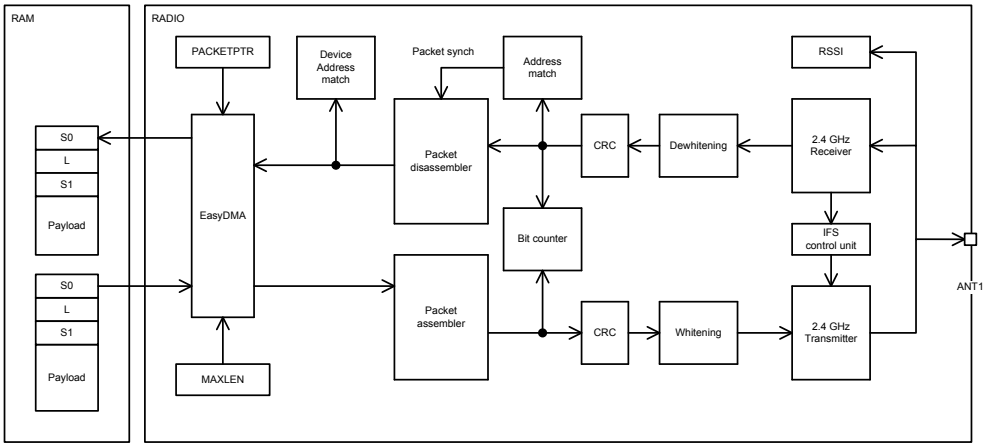



**Figure 30: RADIO block diagram**

The RADIO includes a Device Address match unit and an interframe spacing control unit that can be utilized to simplify address whitelisting and interframe spacing respectively in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

## 22.1 Packet configuration

RADIO packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

The content of a RADIO packet is illustrated in *Figure 31: On-air packet layout* on page 250. The RADIO sends the different fields in the packet in the order they are illustrated below, from left to right:

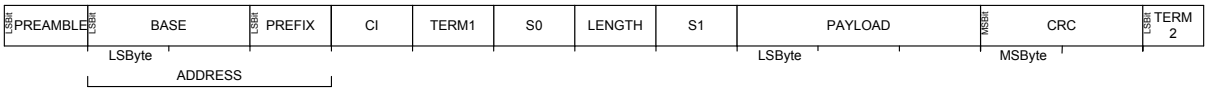



**Figure 31: On-air packet layout**

Not shown in the figure above is the static payload add-on (the length of which is defined in PCNF1.STATLEN, and which is 0 bytes long in a standard BLE packet). The static payload add-on is sent between the PAYLOAD and CRC fields.

PREAMBLE is sent with least significant bit first on-air. The size of the PREAMBLE depends on the mode selected in the MODE register:

- For all Nordic proprietary radio modes (Nrf_1Mbit, Nrf_2Mbit and Nrf_250Kbit) and for the Ble_1Mbit mode, the PREAMBLE is one byte long. The PLEN field in the PCNF0 register has to be set accordingly. If the first bit of the ADDRESS is 0, the PREAMBLE is set to 0xAA. Otherwise the PREAMBLE is set to 0x55.
- For the Ble_2Mbit mode, the PREAMBLE is 2 bytes long. The PLEN field in the PCNF0 register has to be set to 2 bytes accordingly. If the first bit of the ADDRESS is 0, the PREAMBLE is set to 0xAAAA. Otherwise the PREAMBLE is set to 0x5555.
- For the modes Ble_LR125Kbit and Ble_LR500Kbit, the PREAMBLE is 10 repetitions of 0x3C.
- For the Ieee802154_250Kbit mode, the PREAMBLE is 4 bytes long and set to all zeros.

Radio packets are stored in memory, inside instances of a radio packet data structure as illustrated in *Figure 32: In-RAM representation of radio packet - S0, LENGTH and S1 are optional* on page 250. The PREAMBLE, ADDRESS, CI, TERM1, TERM2 and CRC fields are omitted in this data structure.

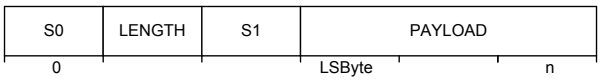



**Figure 32: In-RAM representation of radio packet - S0, LENGTH and S1 are optional**

The byte ordering on the air is always:

- Least significant byte first for the fields ADDRESS and PAYLOAD. The ADDRESS fields are also always transmitted and received least significant bit first on-air.
- Most significant byte first for the CRC field. The CRC field is also always transmitted and received most significant bit first.

The bit endianness, i.e. the order in which the bits are sent and received, is configured in PCNF1.ENDIAN for the fields S0, LENGTH, S1 and PAYLOAD.

The sizes of the fields S0, LENGTH and S1 can be individually configured in the S0LEN, LFLEN and S1LEN fields of the PCNF0 register respectively. If any of these fields are configured to be less than 8 bit long, the least significant bits of the fields are used, as seen from the RAM representation.

If S0, LENGTH or S1 are specified with zero length, their fields will be omitted in memory. Otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

The combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes, independent of the configuration in PCNF1.MAXLEN.

## 22.2 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 31: Definition of logical addresses* on page 251.

**Table 31: Definition of logical addresses**

| Logical address | Base address | Prefix byte |
|---|---|---|
| 0 | BASE0 | PREFIX0.AP0 |
| 1 | BASE1 | PREFIX0.AP1 |
| 2 | BASE1 | PREFIX0.AP2 |
| 3 | BASE1 | PREFIX0.AP3 |
| 4 | BASE1 | PREFIX1.AP4 |
| 5 | BASE1 | PREFIX1.AP5 |
| 6 | BASE1 | PREFIX1.AP6 |
| 7 | BASE1 | PREFIX1.AP7 |

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 31: Definition of logical addresses* on page 251.

## 22.3 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.

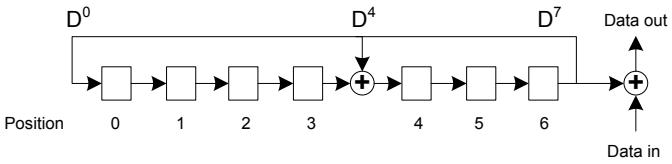



**Figure 33: Data whitening and de-whitening**

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 33: Data whitening and de-whitening* on page 251 can be initialised via the DATAWHITEIV register.

## 22.4 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 34: CRC generation of an n bit CRC* on page 252 where bit 0 in the CRCPOLY register corresponds to $X^0$ and bit 1 corresponds to $X^1$ etc. See CRCPOLY for more information.

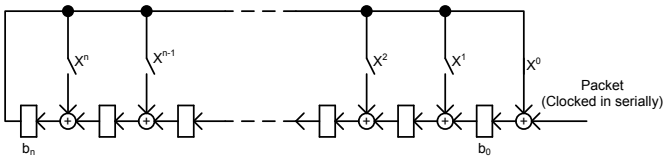



**Figure 34: CRC generation of an n bit CRC**

As illustrated in *Figure 34: CRC generation of an n bit CRC* on page 252, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches $b_0$ through $b_n$ will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches $b_0$ through $b_n$ will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.

The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

## 22.5 Radio states

Tasks and events are used to control the operating state of the RADIO.

The RADIO can enter the states described the table below.

**Table 32: RADIO state diagram**

| State | Description |
|---|---|
| DISABLED | No operations are going on inside the radio and the power consumption is at a minimum |
| RXRU | The radio is ramping up and preparing for reception |
| RXIDLE | The radio is ready for reception to start |
| RX | Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored |
| TXRU | The radio is ramping up and preparing for transmission |
| TXIDLE | The radio is ready for transmission to start |
| TX | The radio is transmitting a packet |
| RXDISABLE | The radio is disabling the receiver |
| TXDISABLE | The radio is disabling the transmitter |

An overview state diagram for the RADIO is illustrated in *Figure 35: Radio states* on page 253.

**Note:** PHYEND is only generated in Ble_LR125Kbit, Ble_LR500Kbit and Ieee802154_250Kbit modes.

**Note:** The END to START shortcut should not be used with Ble_LR125Kbit, Ble_LR500Kbit and Ieee802154_250Kbit modes. Rather the PHYEND to START shortcut.

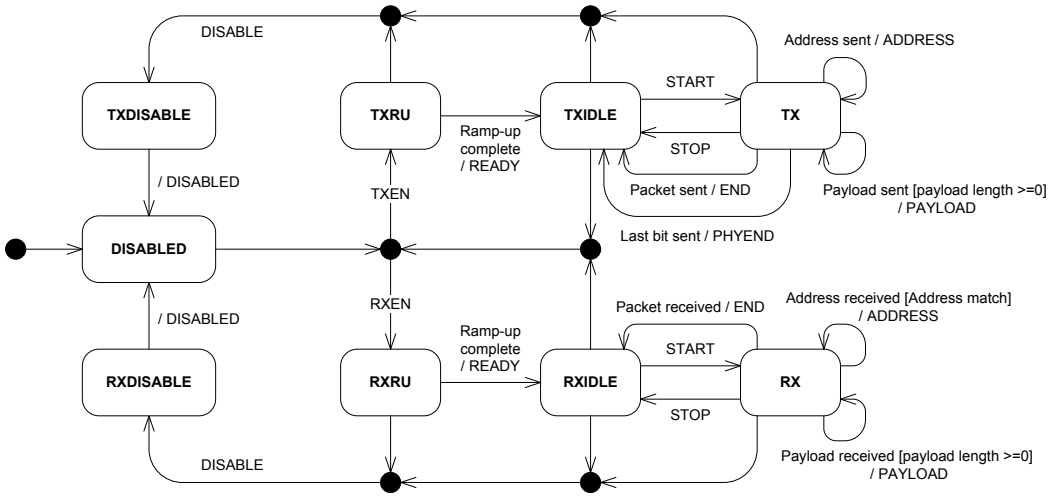



**Figure 35: Radio states**

This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 35: Radio states* on page 253, the PAYLOAD event is always generated even if the payload is zero.

## 22.6 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 35: Radio states* on page 253 and *Figure 36: Transmit sequence* on page 253.
A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 35: Radio states* on page 253 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

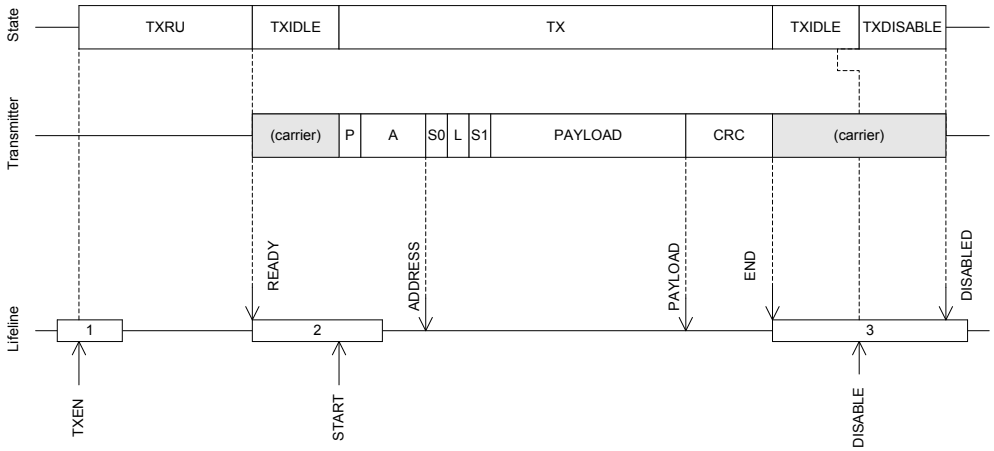



**Figure 36: Transmit sequence**

*Figure 36: Transmit sequence* on page 253 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in *Figure 36: Transmit sequence* on page 253 the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

A slightly modified version of the transmit sequence from *Figure 36: Transmit sequence* on page 253 is illustrated in *Figure 37: Transmit sequence using shortcuts to avoid delays* on page 254 where the RADIO

is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

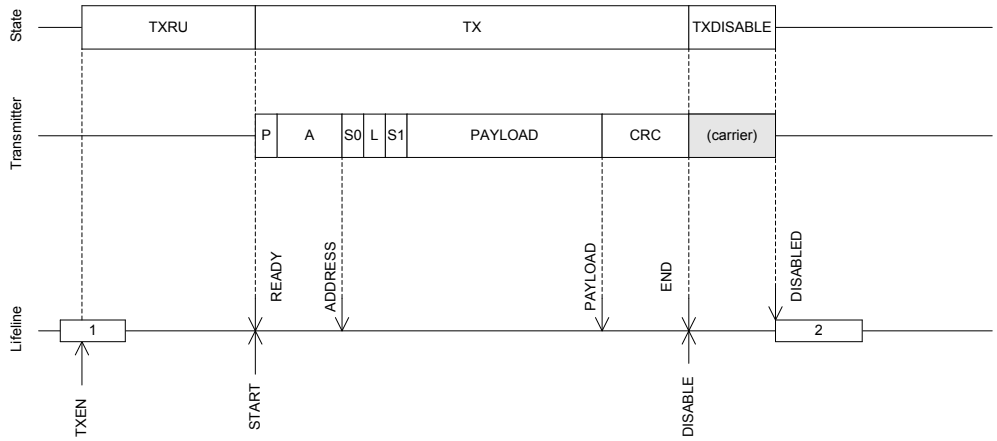



**Figure 37: Transmit sequence using shortcuts to avoid delays**

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 38: Transmission of multiple packets* on page 254.

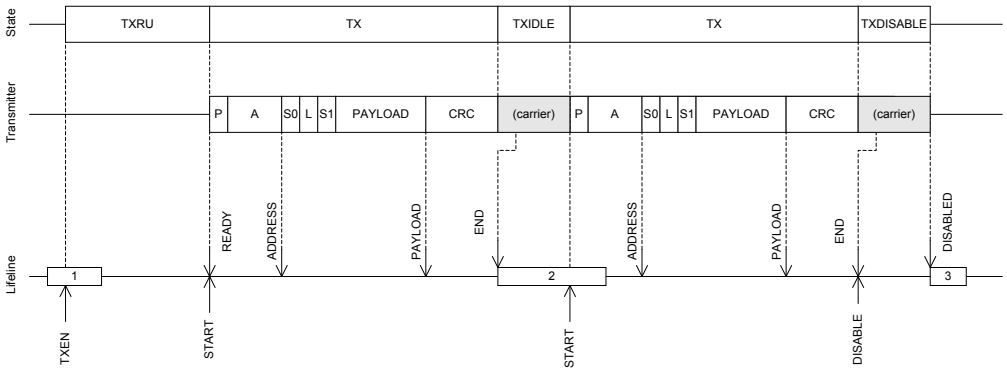



**Figure 38: Transmission of multiple packets**

## 22.7 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in *Figure 35: Radio states* on page 253 and *Figure 39: Receive sequence* on page 255.

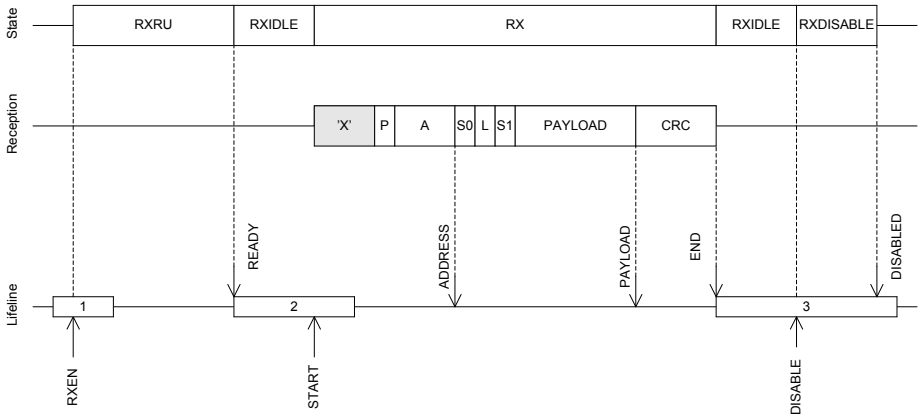



**Figure 39: Receive sequence**

An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 35: Radio states* on page 253 the START task can first be triggered after the RADIO has entered into the RXIDLE state.

*Figure 39: Receive sequence* on page 255 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated *Figure 39: Receive sequence* on page 255 the RADIO will be listening and possibly receiving undefined data, represented with an 'X', from START and until a packet with valid preamble (P) is received.

A slightly modified version of the receive sequence from *Figure 39: Receive sequence* on page 255 is illustrated in *Figure 40: Receive sequence using shortcuts to avoid delays* on page 255 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

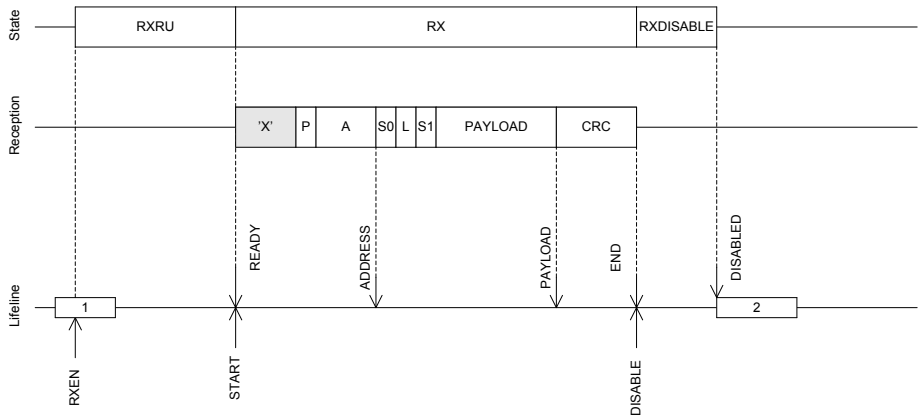



**Figure 40: Receive sequence using shortcuts to avoid delays**

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets as illustrated in *Figure 41: Reception of multiple packets* on page 256.

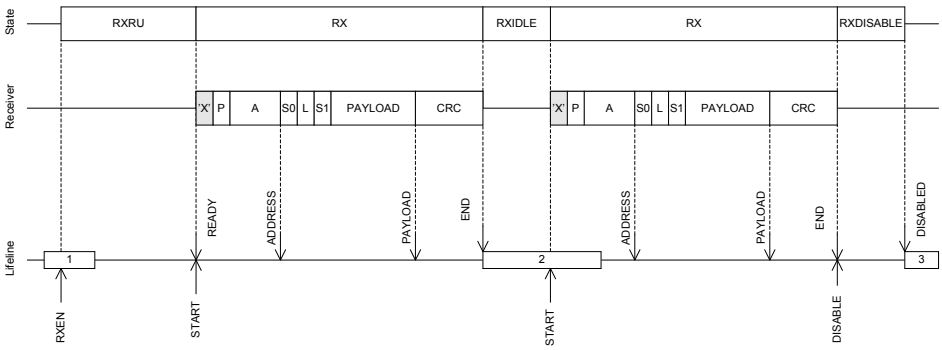



**Figure 41: Reception of multiple packets**

## 22.8 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by $RSSI_{PERIOD}$. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

## 22.9 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turn-around time, i.e. the time needed to switch off the receiver, and switch back on the transmitter. The TIFS register can be written any time before the last bit on air is received.

This timing is illustrated in the *Figure 42: IFS Timing Detail* on page 257. As depicted the TIFS duration starts after the last bit on air, just before the END event, and elapses with first bit being transmitted on air (Just after READY event).

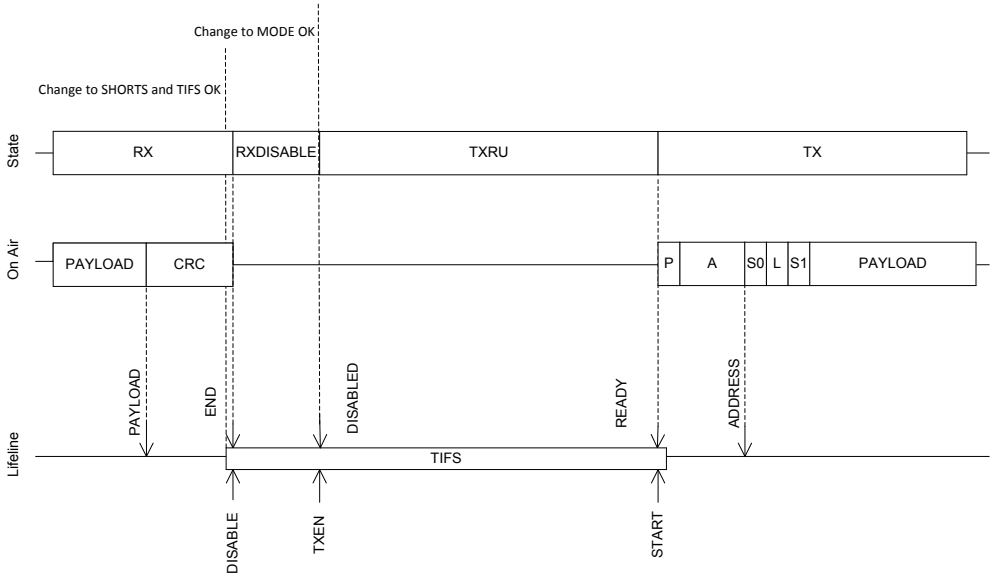



**Figure 42: IFS Timing Detail**

TIFS is only enforced if END_DISABLE and DISABLED_TXEN or END_DISABLE and DISABLED_RXEN shortcuts are enabled. TIFS is qualified for use in BLE_1MBIT, BLE_2MBIT, BLE_LR125KBIT, BLE_LR500KBIT and Ieee802154_250Kbit mode using default ramp-up mode. SHORTS and TIFS are not double buffered and can be updated at any point in time before the last bit on air is received. The MODE register is double buffered and sampled at the TXEN or RXEN task.

## 22.10 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

## 22.11 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.

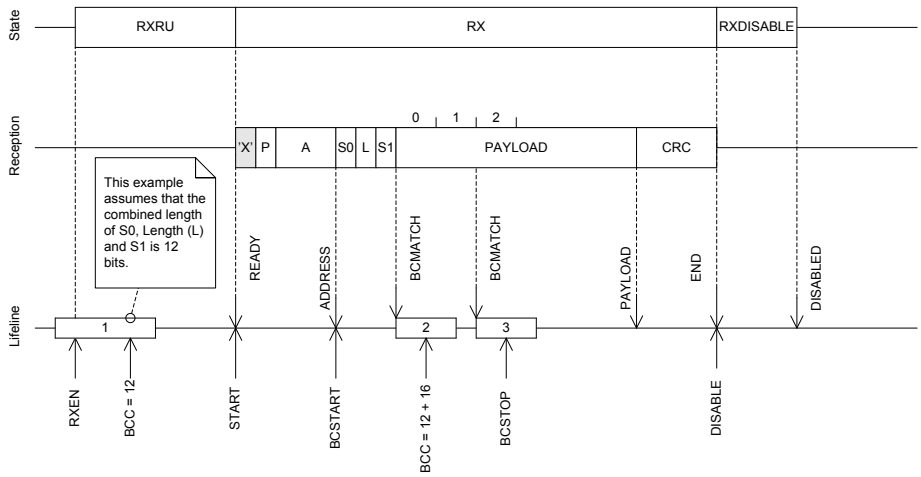



**Figure 43: Bit counter example**

## 22.12 IEEE 802.15.4 Operation

With the MODE=Ieee802154_250kbit the radio module will comply with the IEEE 802.15.4-2006 standard implementing its 250 kbps 2450MHz O-QPSK PHY.

The IEEE 802.15.4 standard differs from Nordic's proprietary and Bluetooth Smart modes. Obvious differences are modulation scheme and channel structure, but also packet structure, security and medium access control.

The main features of the IEEE 802.15.4 mode are:

- Ultra Low power 250 kbps 2450MHz IEEE 802.15.4-2006 compliant link
- Clear Channel Assessment
- Energy detection scan
- CRC Generation

### 22.12.1 Packet Structure

The IEEE 802.15.4 standard defines an on the air frame/packet that is different from what is used in BTLE mode.

*Figure 44: IEEE 802.15.4 Frame Format - PHY-Layer Frame Structure (PPDU)* on page 258 provides an overview of the physical frame structure and its timing.

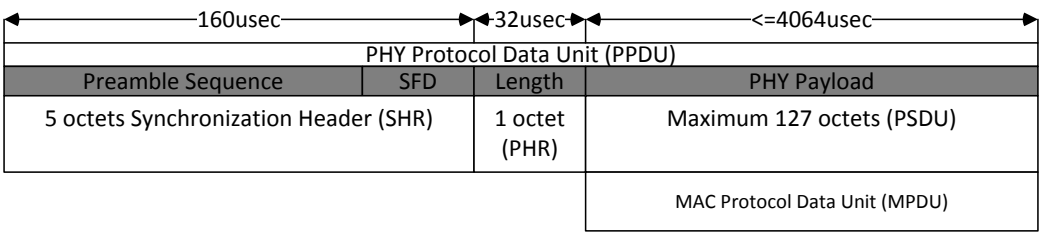



**Figure 44: IEEE 802.15.4 Frame Format - PHY-Layer Frame Structure (PPDU)**

The standard uses the term octet as storage unit for 8-bits within the PPDU. For timing the value symbol is used and it has the duration of 16usec.

The total usable payload (PSDU) is 127 octets - but when CRC is being used this is reduced to 125 octets of usable payload.

The preamble sequence consists of four octets that are all zero. These are used for the radio receiver to synchronize on. Following the four octets is a single octet named start of frame delimiter (SFD) with a fixed value of 0xA7. The user can program an alternative SFD through the SFD register. This feature is provided for an initial level of frame filtering for those who choose non standard compliance. It is a valuable feature when operating in a congested or private network. The preamble sequence and SFD is generated by the radio module and is not programmed by the user into the frame buffer.

The PHY header (PHR) is a single octet following the SHR. The least significant seven bits denote the frame length of the following PSDU. The most significant bit is reserved and shall be set to zero for frames that wishes to be standards compliant. The radio module will report all eight bits and it can potentially be used to carry some information. The PHR is the first byte that will be written to the frame Data Memory pointed to by PACKETPTR. Frames with zero length will be discarded and the FRAMESTART event will not be generated in this case.

The next N octets will carry the data of the PHY packet - where N equals the value of the PHR. For an implementation also using the IEEE 802.15.4 MAC layer, the PHY data will be a MAC frame of N-2 octets since two octets will occupy a CRC field.

An IEEE 802.15.4 MAC frame will always consist of a header (The frame control field (FCF), Sequence Number and Addressing Fields), a payload and the 16-bit Frame Control Sequence (FCS) as seen in *Figure 45: IEEE 802.15.4 Frame Format - MAC-Layer Frame Structure (MPDU)* on page 259.

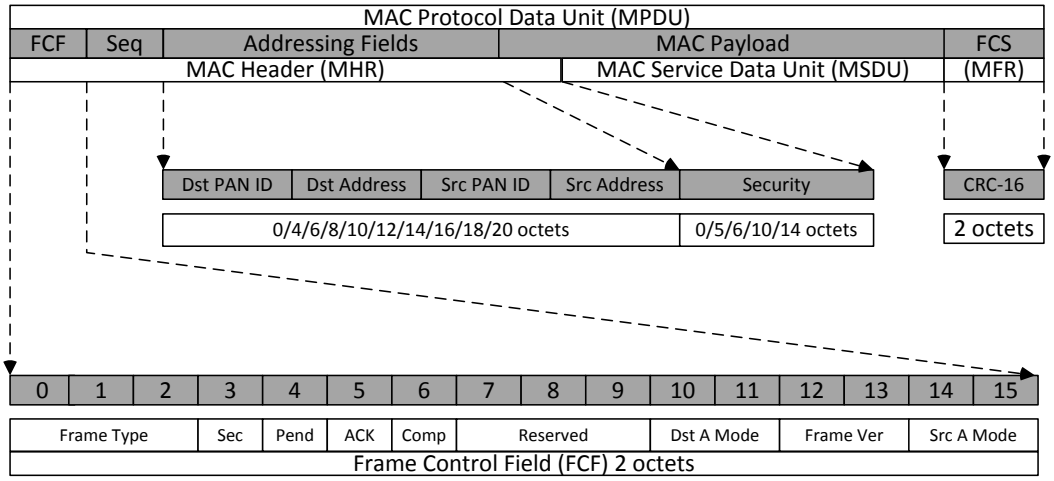



**Figure 45: IEEE 802.15.4 Frame Format - MAC-Layer Frame Structure (MPDU)**

The two FCF octets contains information about what type of frame this is, what addressing it uses and other control flags. This field is decoded when using the assisted operating modes offered by the radio.

The sequence number is a single octet in size and is unique for a frame. It will be used in the associated acknowledgement frame sent upon successful frame reception.

The addressing field can be zero (Acknowledgement Frame) or up to 20 octets in size. The field is used to direct packets to the correct recipient as well as denoting its origin. IEEE 802.15.4 bases it's addressing on networks being organized in PANs with 16-bit identifier and nodes having a 16 or 64-bit address. In the assisted receive mode these parameters are analyzed for address matching and acknowledgement.

The MAC payload carries the data of the next higher layer or in the case of a MAC command frame information used by the MAC layer itself.

The two last octets contain the 16-bit ITU-T CRC. The FCS is calculated over the MAC header (MHR) and MAC payload (MSDU) parts of the frame. This field is calculated automatically when sending a frame - or indicated in the CRCSTATUS register when a frame is received. This feature is taken care of autonomously by the CRC module if configured.

### 22.12.2 Operating Frequencies

The IEEE 802.15.4 standard defines 16 channels [11 - 26] in the 2450MHz frequency band of 5MHz each.

The FREQUENCY register of the radio module must be programmed according to *Table 33: IEEE 802.15.4 Center Frequency Definition* on page 260 for correct operation on the center frequency defined for each channel.

**Table 33: IEEE 802.15.4 Center Frequency Definition**

| IEEE 802.15.4 Channel | Center Frequency (MHz) | FREQUENCY Setting |
|---|---|---|
| Channel 11 | 2405 | 5 |
| Channel 12 | 2410 | 10 |
| Channel 13 | 2415 | 15 |
| Channel 14 | 2420 | 20 |
| Channel 15 | 2425 | 25 |
| Channel 16 | 2430 | 30 |
| Channel 17 | 2435 | 35 |
| Channel 18 | 2440 | 40 |
| Channel 19 | 2445 | 45 |
| Channel 20 | 2450 | 50 |
| Channel 21 | 2455 | 55 |
| Channel 22 | 2460 | 60 |
| Channel 23 | 2465 | 65 |
| Channel 24 | 2470 | 70 |
| Channel 25 | 2475 | 75 |
| Channel 26 | 2480 | 80 |

### 22.12.3 Energy Detection

The IEEE 802.15.4 standard requires that it is possible to sample the received signal power within the bandwidth of a channel for the purpose of determining presence of activity.

There should be no attempt made to decode the signals on the channel, and this is done by disabling the shortcut between READY event and START task before putting the radio in receive mode. The energy detection (ED) measurement time where RSSI samples are averaged over is 8 symbol periods (128 microseconds). The standard further specifies the measurement to be a number between 0 and 0xFF - where 0 shall indicate received power less than 10dB above the selected receiver sensitivity. The power range of the ED values must be at least 40dB with a linear mapping with accuracy of +-6dB. See section 6.9.7 Receiver ED in the standard for further details. An example of an ED scan is given below.

Below is a code snippet showing how to perform a single energy detection measurement.

```
uint8_t sample_ed(void)
{
 NRF_RADIO->TASKS_EDSTART = 1;               //Start
 while (NRF_RADIO->EVENTS_EDEND != 1) {
     //CPU can sleep here or do something else
     //Use of interrupts are encouraged
   }
 return (uint8_t)NRF_RADIO->EDSAMPLE; //Read level
}
```

It is the mlme-scan.req primitive of the MAC layer that is using the ED measurement to detect channels where there might be wireless activity. To assist this primitive a taylored mode of operation is available where the ED measurement runs for a defined number of iterations where it keeps track of the maximum ED level. This is enganged by writing the ED_CNT register to a value different from 0, it will then run the specified number of iterations reporting the maximum energy measurement in the EDSAMPLE register. The scan is started with EDSTART task and its end indicated with the EDEND event. This greatly reduces the interrupt frequency and hence power consumtion. *Figure 46: Energy Detection Measurement Examples* on page 261 shows how the ED measurement will operate depending on the ED_CNT register.

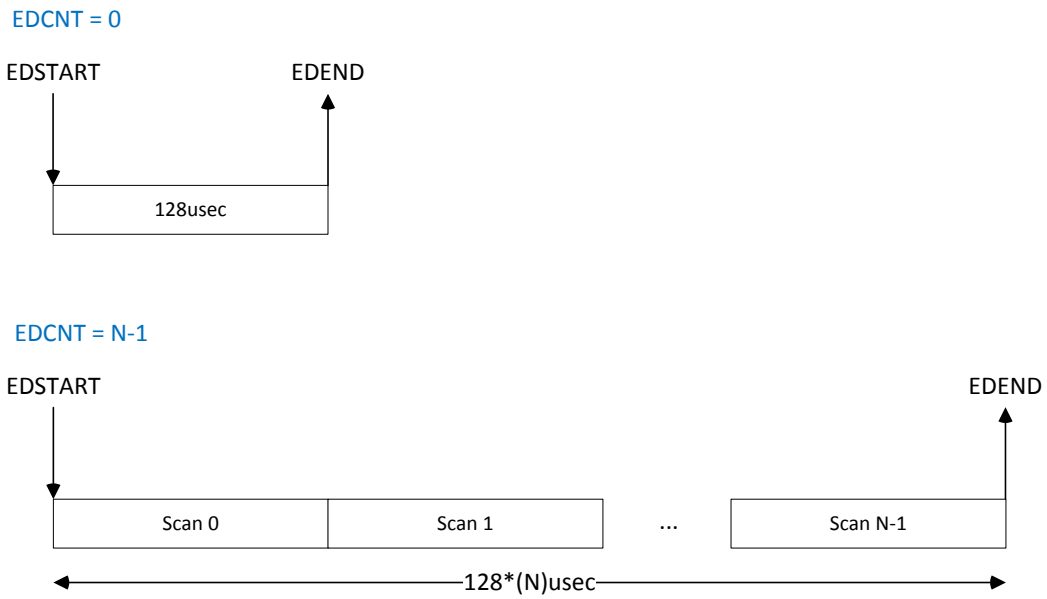



**Figure 46: Energy Detection Measurement Examples**

An ongoing scan can always be stopped by writing the EDSTOP task. It will be followed by the EDSTOPPED event when the module has terminated.

### 22.12.4 Clear Channel Assessment

IEEE 802.15.4 implements a listen-before-talk channel access method to avoid collisions when transmitting - namely Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA). The key part of this is measuring if the wireless medium is busy or not.

At least three methods must be supported:

- Mode 1 (Energy above threshold): The medium is reported busy upon detecting any energy above the ED threshold
- Mode 2 (Carrier sense only): The medium is reported busy upon detection of a signal compliant with the IEEE 802.15.4 standard with the same modulation and spreading characteristics.
- Mode 3 (Carrier sense and threshold): The medium is reported busy by logically ANDing or ORing the results from Mode 1 and Mode 2.

It is furthermore specified that the clear channel assessment should survey a period equal to 8 symbols or 128usec.

The radio module has to be in receive mode and be able to recived correct packets when performing the CCA. The shortcut between READY and START must be disabled if baseband processing is not to be performed while the measurement is running.

Mode 1 is enabled by first configuring the CCA_MODE=EdMode and writing the CCA_EDTHRES to a chosen value. When the CCA_START task is written the radio module will perform a ED measurement for 8 symbols and compare the measured level with that found in the CCA_EDTHRES register. If the measured value is higher than or equal to this threshold the CCABUSY event is generated - the CCAIDLE event is generated if the measured level is less than the threshold.

Mode 2 is enabled by configuring the CCA_MODE=CarrierMode. In carrier mode the module will sample to see if a valid SFD is found during the 8 symbols. If a valid SFD is seen the CCABUSY event is generated and the node should not send any data. The CCABUSY event is also generated if the scan was performed during an ongoing frame reception. In the case where the measurement period completes with no SFD detection the CCAIDLE task is generated. With the CCA_CORR_COUNT unequal to zero the algorithm will look at the correlator output in addition to the SFD detection signal. If a SFD is reported during the scan period it will terminate immidiately indicating busy medium. Similarly, if the number of peaks above CCA_CORRTHRES crosses the CCA_CORR_COUNT the CCABUSY event is generated. If less than

CCA_CORR_COUNT crossings are found and no SFD is reported the CCAIDLE signal will be generated and it is ok for the node to commence sending data.

With the CCA_MODE=CarrierAndEdMode or CCA_MODE=CarrierOrEdMode a logical combination of the result from running both Mode 1 and Mode 2 is performed. The CCABUSY or CCAIDLE signal will be generated based on an ANDing or ORing of the internal signals from performing both the energy detection and carrier detection scans.

An ongoing CCA can always be stopped by issuing the CCASTOP task. This will trigger the associated CCASTOPPED event.

For CCA mode automation there are three shortcuts available. One is between CCAIDLE and TXEN. This short must always be used in conjunction with the short between CCAIDLE and STOP. This automation is provided so that the radio can automatically switch between RX (When performing the CCA) and to TX where the packet is sent. The last shortcut associated with the CCA mode is between CCABUSY and DISABLE. This will cause the radio to be disabled whenever the CCA reports a busy medium.

Another handy shortcut is between RXREADY and CCASTART. When the radio has ramped up into RX mode it can immidiately start a CCA.

### 22.12.5 Cyclic Redundancy Check

IEEE 802.15.4 uses a 16-bit ITU-T cyclic redundancy check (CRC) calculated over the MHR and MSDU.

The standard defines the following generator polynomial:

$G(x) = x^{16} + x^{12} + x^5 + 1$

In receive mode the radio will trigger the CRC module when the first octet after the frame length (PHR) is received. The CRC will then update on each consecutive octet received. When a complete frame is received the CRCSTATUS register will be updated accordingly and the EVENTS_CRCOK or EVENTS_CRCERROR generated. When the CRC module is enabled it will not write the two last octets (CRC) to the frame Data RAM. When transmitting the CRC will be computed on the fly, starting with the first octet after PHR, and inserted as the two last octets in the frame. The EasyDMA will fetch frame length - 2 octets from DataRAM and insert the CRC octets insitu.

Below is a code snippet for configuring the CRC module for correct operation when in IEEE 802.15.4 mode. The CRCCNF is written to 16-bit CRC and the CRCPOLY is written to 0x121. The start value used by IEEE 802.15.4 is zero and CRCINIT is configured to reflect this.

```
/* 16-bit CRC with ITU-T polynomial with 0 as start condition*/
write_reg(NRFRADIO_REG(CRCCNF), 0x202);
write_reg(NRFRADIO_REG(CRCPOLY), 0x11021);
write_reg(NRFRADIO_REG(CRCINIT), 0);
```

The ENDIANESS subregister must be set to LittleEndian since the FCS field is transmitted leftmost bit first.

### 22.12.6 Transmit Sequence

The transmission is started by first putting the radio in receive mode sending the RXEN task.

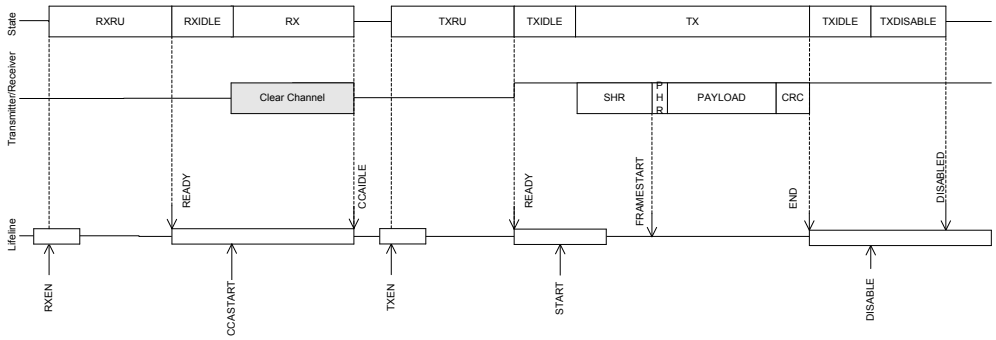



**Figure 47: IEEE 802.15.4 Transmit Sequence**

The receiver will ramp up and enter the RXIDLE state where the READY event is generated. Upon receiving the ready event the CCA is started by writing to the CCASTART task register. The chosen mode of assessment (CCA_MODE register) will be performed and signal the CCAIDLE or CCABUSY event 128usec later. If the CCABUSY is received the radio will have to retry the CCA after a specific back off period as outlined in the IEEE 802.15.4 standard (See Figure 69 in section 7.5.1.4 The CSMA-CA algorithm of the standard). An outline of the IEEE 802.15.4 transmission can be found in the figure below.

When the CCAIDLE event on the other hand is generated the user shall write to the TXEN task register to enter the TXRU state. The READY event will be generated when the radio is in TXIDLE state and ready to transmit. With the PACKETPTR pointing to the length (PHR) field of the frame the START task can be written. The radio will send the four octet preamble sequence followed by the start of frame delimiter (SFD register). The first byte read from the DataRAM is the length field (PHR) followed by the transmission of the number of bytes indicated as the frame length. If the CRC module is configured it will run for PHR-2 octets. The last two octets will be substituted with the results from running the CRC. The necessary CRC parameters are sampled on the START task. The FCS field of the frame is little endian.

In addition to the already available shortcuts, one is provided between READY event and CCASTART task so that a CCA can automatically start when the receiver is ready. And a second shortcut has been added between CCAIDLE event and the TXEN task so that upon detecting a clear channel the radio can immediately enter transmit mode.

## 22.12.7 Receive Sequence

The reception is started by first putting the radio in receive mode. Writing to the RXEN task the radio will start ramping up and enter the RXRU state.

When the READY event is generated the radio has entered the RXIDLE mode. For the baseband processing to be enabled the START task must be written. An outline of the IEEE 802.15.4 reception can be found in *Figure 48: IEEE 802.15.4 Receive Sequence* on page 263

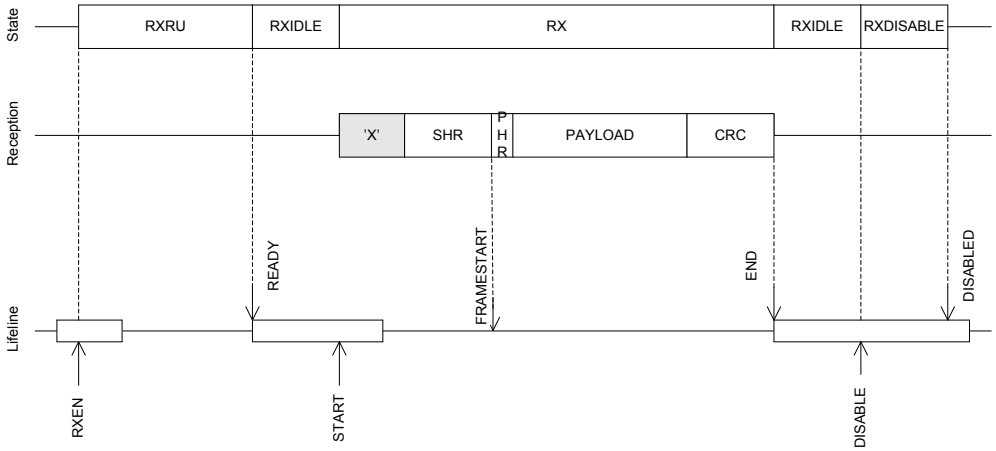



**Figure 48: IEEE 802.15.4 Receive Sequence**

When a valid SHR is received the radio will start storing future octets (Starting with PHR) to the DataMemory pointed to by PACKETPTR. After the SFD octet is received the FRAMESTART event is generated. If the CRC module is enabled it will start updating with the second byte received (First byte in payload) and run for the full frame length. The two last bytes in the frame is not written to DataRAM when CRC is configured. However, if the result of the CRC after running the full frame is zero the CRCOK event will be generated. The END event is generated when the last octet has been received and is available in DataRAM.

When a packet is received a link quality indicator (LQI) is also generated and appended immediately after the last received octet. When using IEEE 802.15.4 compliant frame this will be just after the MSDU since the FCS is not reported. In the case of a non-complient frame it will be appended after the full frame. The LQI is a number ranging from 0 (lowest link quality) to 255 (highest link quality). The LQI is only valid for frames equal to or longer than three octets. When receiving a frame the RSSI (Reported as negative dB) will be measured at three points during the reception. These three values will be sorted and the middle one selected (Median 3) for then to be remapped within the LQI range. See *Figure 49: IEEE 802.15.4 Frame In DataRAM* on page 264 for further detail on the LQI measurement and how the data is arranged in the DataRAM.

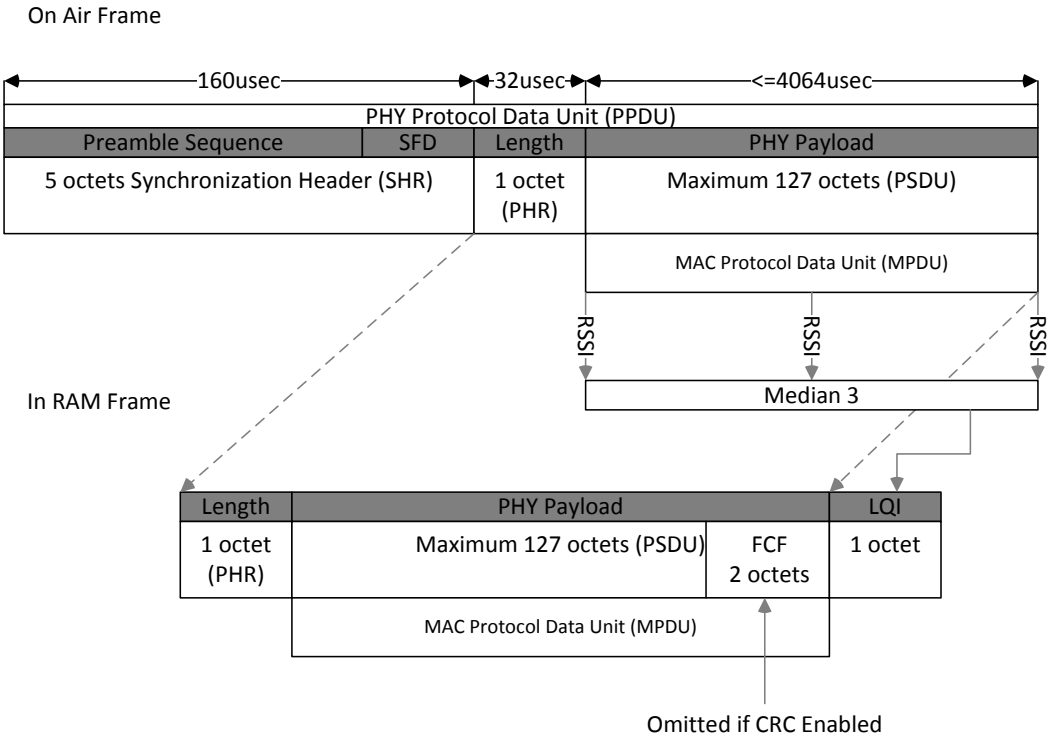



**Figure 49: IEEE 802.15.4 Frame In DataRAM**

A shortcut has been added between FRAMESTART event and the BCSTART task. This can be used to trig a BCMATCH event after N bits - such as when inspecting the MAC addressing fields.

## 22.12.8 Interframe Spacing

The IEEE 802.15.4 standard defines a specific time that is alotted for the MAC sublayer to process received data. Usage of this interframe spacing (IFS) comes into play to avoid that two frames are transmitted too close to eachother in time. If the a transmission is requesting an acknowledgement, the speration to the second frame shall be at least an IFS period.

The IFS is determined to be:

- IFS equals macMinSIFSPeriod (12 symbols) if the MPDU is less than or equal to aMaxSIFSFrameSize (18 octets) octets
- IFS equals macMinLIFSPeriod (40 symbols) if the MPDU is larger than aMaxSIFSFrameSize

The TIFS register must be manually updated by the user based upon the above mentioned length rules. *Figure 50: Interframe Spacing Examples* on page 265 provides further detail on what IFS period is valid in both acknowledged and unacknowledged transmissions.

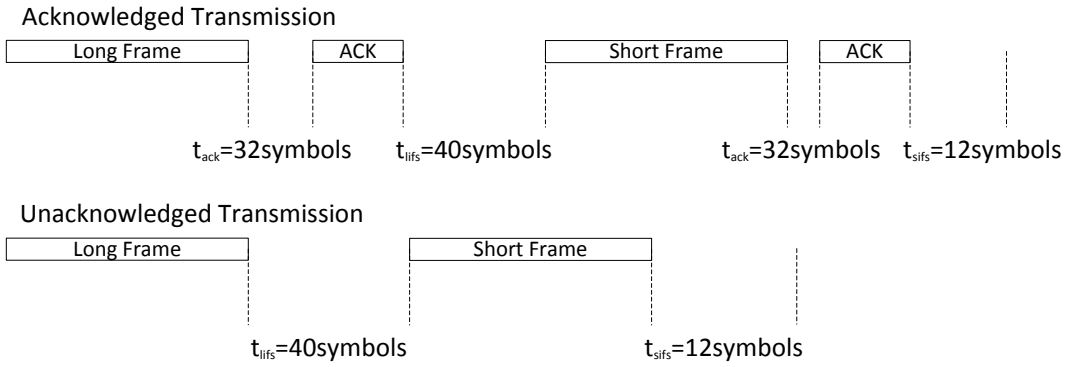



**Figure 50: Interframe Spacing Examples**

## 22.13 EasyDMA

The RADIO peripheral uses EasyDMA for reading of data packets from and writing to RAM, without CPU involvement.

As illustrated in *Figure 30: RADIO block diagram* on page 249, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. This pointer should be reconfigured by the CPU each time before RADIO is started by the START task. Both the PACKETPTR and MAXLEN registers are double-buffered, meaning that they can be updated and prepared for the next transmission.

> **Important:** If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The END event indicates that the last bit has been processed by the radio. The DISABLED event is issued to acknowledge that a DISABLE task is done.

The structure of a radio packet is described in detail in *Packet configuration* on page 249. The data that is stored in Data RAM and transported by EasyDMA consists of the following fields:

- S0
- LENGTH
- S1
- PAYLOAD

In addition, a static add-on is sent immediately after the payload.

The size of each of the above fields in the frame is configurable, and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen. All fields are extended in size to align with a byte boundary in RAM. For instance a 3 bit long field on air will occupy 1 byte in RAM while a 9 bit long field will be extended to 2 bytes.

The radio packet fields can be configured as follows:

- The fields CI, TERM1 and TERM2 are only present in Bluetooth Smart Long Range mode
- S0 is configured in the S0LEN field of the PCNF0 register
- LENGTH is configured in the LFLEN field of the PCNF0 register
- S1 is configured in the S1LEN field of the PCNF0 register
- The size of the payload is configured by the value in RAM corresponding to the LENGTH field
- The size of the static add-on to the payload is configured in the STATLEN field of the PCNF1 register

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by the PCNF1.STATLEN and the LENGTH field in the packet specify a packet larger than MAXLEN, the payload will be truncated at MAXLEN. The packet's LENGTH field will not

be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

> **Important:** The MAXLEN includes the size of the payload and the add-on, but excludes the size occupied by the fields S0, LENGTH and S1. This has to be taken into account when allocating RAM.

## 22.14 Registers

### Table 34: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40001000 | RADIO | RADIO | 2.4 GHz radio | |

### Table 35: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_TXEN | 0x000 | Enable RADIO in TX mode |
| TASKS_RXEN | 0x004 | Enable RADIO in RX mode |
| TASKS_START | 0x008 | Start RADIO |
| TASKS_STOP | 0x00C | Stop RADIO |
| TASKS_DISABLE | 0x010 | Disable RADIO |
| TASKS_RSSISTART | 0x014 | Start the RSSI and take one single sample of the receive signal strength. |
| TASKS_RSSISTOP | 0x018 | Stop the RSSI measurement |
| TASKS_BCSTART | 0x01C | Start the bit counter |
| TASKS_BCSTOP | 0x020 | Stop the bit counter |
| TASKS_EDSTART | 0x024 | Start the Energy Detect measurement used in IEEE 802.15.4 mode |
| TASKS_EDSTOP | 0x028 | Stop the Energy Detect measurement |
| TASKS_CCASTART | 0x02C | Start the Clear Channel Assessment used in IEEE 802.15.4 mode |
| TASKS_CCASTOP | 0x030 | Stop the Clear Channel Assessment |
| EVENTS_READY | 0x100 | RADIO has ramped up and is ready to be started |
| EVENTS_ADDRESS | 0x104 | Address sent or received |
| EVENTS_PAYLOAD | 0x108 | Packet payload sent or received |
| EVENTS_END | 0x10C | Packet sent or received |
| EVENTS_DISABLED | 0x110 | RADIO has been disabled |
| EVENTS_DEVMATCH | 0x114 | A device address match occurred on the last received packet |
| EVENTS_DEVMISS | 0x118 | No device address match occurred on the last received packet |
| EVENTS_RSSIEND | 0x11C | Sampling of receive signal strength complete. |
| EVENTS_BCMATCH | 0x128 | Bit counter reached bit count value. |
| EVENTS_CRCOK | 0x130 | Packet received with CRC ok |
| EVENTS_CRCERROR | 0x134 | Packet received with CRC error |
| EVENTS_FRAMESTART | 0x138 | IEEE 802.15.4 length field received |
| EVENTS_EDEND | 0x13C | Sampling of Energy Detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register |
| EVENTS_EDSTOPPED | 0x140 | The sampling of Energy Detection has stopped |
| EVENTS_CCAIDLE | 0x144 | Wireless medium in idle - clear to send |
| EVENTS_CCABUSY | 0x148 | Wireless medium busy - do not send |
| EVENTS_CCASTOPPED | 0x14C | The CCA has stopped |
| EVENTS_RATEBOOST | 0x150 | Ble_LR CI field received, receive mode is changed from Ble_LR125Kbit to Ble_LR500Kbit. |
| EVENTS_TXREADY | 0x154 | RADIO has ramped up and is ready to be started TX path |
| EVENTS_RXREADY | 0x158 | RADIO has ramped up and is ready to be started RX path |
| EVENTS_MHRMATCH | 0x15C | MAC Header match found. |
| EVENTS_PHYEND | 0x16C | Generated in Ble_LR125Kbit, Ble_LR500Kbit and BleIeee802154_250Kbit modes when last bit is sent on air. |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *CRCSTATUS* | 0x400 | CRC status |
| *RXMATCH* | 0x408 | Received address |

| Register | Offset | Description |
|---|---|---|
| RXCRC | 0x40C | CRC field of previously received packet |
| DAI | 0x410 | Device address match index |
| PDUSTAT | 0x414 | Payload status |
| PACKETPTR | 0x504 | Packet pointer |
| FREQUENCY | 0x508 | Frequency |
| TXPOWER | 0x50C | Output power |
| MODE | 0x510 | Data rate and modulation |
| PCNF0 | 0x514 | Packet configuration register 0 |
| PCNF1 | 0x518 | Packet configuration register 1 |
| BASE0 | 0x51C | Base address 0 |
| BASE1 | 0x520 | Base address 1 |
| PREFIX0 | 0x524 | Prefixes bytes for logical addresses 0-3 |
| PREFIX1 | 0x528 | Prefixes bytes for logical addresses 4-7 |
| TXADDRESS | 0x52C | Transmit address select |
| RXADDRESSES | 0x530 | Receive address select |
| CRCCNF | 0x534 | CRC configuration |
| CRCPOLY | 0x538 | CRC polynomial |
| CRCINIT | 0x53C | CRC initial value |
| TIFS | 0x544 | Inter Frame Spacing in us |
| RSSISAMPLE | 0x548 | RSSI sample |
| STATE | 0x550 | Current radio state |
| DATAWHITEIV | 0x554 | Data whitening initial value |
| BCC | 0x560 | Bit counter compare |
| DAB[0] | 0x600 | Device address base segment 0 |
| DAB[1] | 0x604 | Device address base segment 1 |
| DAB[2] | 0x608 | Device address base segment 2 |
| DAB[3] | 0x60C | Device address base segment 3 |
| DAB[4] | 0x610 | Device address base segment 4 |
| DAB[5] | 0x614 | Device address base segment 5 |
| DAB[6] | 0x618 | Device address base segment 6 |
| DAB[7] | 0x61C | Device address base segment 7 |
| DAP[0] | 0x620 | Device address prefix 0 |
| DAP[1] | 0x624 | Device address prefix 1 |
| DAP[2] | 0x628 | Device address prefix 2 |
| DAP[3] | 0x62C | Device address prefix 3 |
| DAP[4] | 0x630 | Device address prefix 4 |
| DAP[5] | 0x634 | Device address prefix 5 |
| DAP[6] | 0x638 | Device address prefix 6 |
| DAP[7] | 0x63C | Device address prefix 7 |
| DACNF | 0x640 | Device address match configuration |
| MHRMATCHCONF | 0x644 | Search Pattern Configuration |
| MHRMATCHMAS | 0x648 | Pattern mask |
| MODECNF0 | 0x650 | Radio mode configuration register 0 |
| SFD | 0x660 | IEEE 802.15.4 Start of Frame Delimiter |
| EDCNT | 0x664 | IEEE 802.15.4 Energy Detect Loop Count |
| EDSAMPLE | 0x668 | IEEE 802.15.4 Energy Detect Level |
| CCACTRL | 0x66C | IEEE 802.15.4 Clear Channel Assessment Control |
| POWER | 0xFFC | Peripheral power control |

### 22.14.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | U | T | S | R | Q | P | O | N | M | L | K | | | H | | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | END_DISABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DISABLED_TXEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DISABLED_RXEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ADDRESS_RSSISTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | END_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | ADDRESS_BCSTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | DISABLED_RSSISTOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | RXREADY_CCASTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CCAIDLE_TXEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CCABUSY_DISABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | FRAMESTART_BCSTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | READY_EDSTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | U | T | S | R | Q | P | O | N | M | L | K | | | H | | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | EDEND_DISABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EDEND* and *TASKS_DISABLE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CCAIDLE_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CCAIDLE* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | TXREADY_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXREADY* and *TASKS_START* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | RXREADY_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXREADY* and *TASKS_START* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | PHYEND_DISABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_PHYEND* and *TASKS_DISABLE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | PHYEND_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_PHYEND* and *TASKS_START* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | ADDRESS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ADDRESS* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PAYLOAD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_PAYLOAD* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_END* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | DISABLED | | | | | | | | | | Write '1' to Enable interrupt for DISABLED event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_DISABLED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | DEVMATCH | | | | | | | | | | Write '1' to Enable interrupt for DEVMATCH event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_DEVMATCH* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | DEVMISS | | | | | | | | | | Write '1' to Enable interrupt for DEVMISS event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_DEVMISS* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RSSIEND | | | | | | | | | | Write '1' to Enable interrupt for RSSIEND event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_RSSIEND* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | BCMATCH | | | | | | | | | | Write '1' to Enable interrupt for BCMATCH event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_BCMATCH* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CRCOK | | | | | | | | | | Write '1' to Enable interrupt for CRCOK event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_CRCOK* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CRCERROR | | | | | | | | | | Write '1' to Enable interrupt for CRCERROR event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_CRCERROR* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | FRAMESTART | | | | | | | | | | Write '1' to Enable interrupt for FRAMESTART event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_FRAMESTART* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | EDEND | | | | | | | | | | Write '1' to Enable interrupt for EDEND event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_EDEND* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | EDSTOPPED | | | | | | | | | | Write '1' to Enable interrupt for EDSTOPPED event | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_EDSTOPPED* | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CCAIDLE | | | | | | | | | | Write '1' to Enable interrupt for CCAIDLE event<br>See *EVENTS_CCAIDLE* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CCABUSY | | | | | | | | | | Write '1' to Enable interrupt for CCABUSY event<br>See *EVENTS_CCABUSY* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CCASTOPPED | | | | | | | | | | Write '1' to Enable interrupt for CCASTOPPED event<br>See *EVENTS_CCASTOPPED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | RATEBOOST | | | | | | | | | | Write '1' to Enable interrupt for RATEBOOST event<br>See *EVENTS_RATEBOOST* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | TXREADY | | | | | | | | | | Write '1' to Enable interrupt for TXREADY event<br>See *EVENTS_TXREADY* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | RXREADY | | | | | | | | | | Write '1' to Enable interrupt for RXREADY event<br>See *EVENTS_RXREADY* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | MHRMATCH | | | | | | | | | | Write '1' to Enable interrupt for MHRMATCH event<br>See *EVENTS_MHRMATCH* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PHYEND | | | | | | | | | | Write '1' to Enable interrupt for PHYEND event<br>See *EVENTS_PHYEND* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | ADDRESS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | PAYLOAD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | DISABLED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | DEVMATCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | DEVMISS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RSSIEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | BCMATCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CRCOK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CRCERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_CRCERROR* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| M | RW | FRAMESTART | | | Write '1' to Disable interrupt for FRAMESTART event<br><br>See *EVENTS_FRAMESTART* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| N | RW | EDEND | | | Write '1' to Disable interrupt for EDEND event<br><br>See *EVENTS_EDEND* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| O | RW | EDSTOPPED | | | Write '1' to Disable interrupt for EDSTOPPED event<br><br>See *EVENTS_EDSTOPPED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| P | RW | CCAIDLE | | | Write '1' to Disable interrupt for CCAIDLE event<br><br>See *EVENTS_CCAIDLE* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| Q | RW | CCABUSY | | | Write '1' to Disable interrupt for CCABUSY event<br><br>See *EVENTS_CCABUSY* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| R | RW | CCASTOPPED | | | Write '1' to Disable interrupt for CCASTOPPED event<br><br>See *EVENTS_CCASTOPPED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| S | RW | RATEBOOST | | | Write '1' to Disable interrupt for RATEBOOST event<br><br>See *EVENTS_RATEBOOST* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| T | RW | TXREADY | | | Write '1' to Disable interrupt for TXREADY event<br><br>See *EVENTS_TXREADY* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| U | RW | RXREADY | | | Write '1' to Disable interrupt for RXREADY event<br><br>See *EVENTS_RXREADY* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| V | RW | MHRMATCH | | | Write '1' to Disable interrupt for MHRMATCH event<br><br>See *EVENTS_MHRMATCH* |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | Z | | | | V | U | T | S | R | Q | P | O | N | M | L | K | | I | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | PHYEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_PHYEND* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.4 CRCSTATUS

Address offset: 0x400

CRC status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | CRCSTATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CRCError | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CRCOk | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.5 RXMATCH

Address offset: 0x408

Received address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXMATCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Logical address of which previous packet was received | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXCRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | CRC field of previously received packet | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.7 DAI

Address offset: 0x410

Device address match index

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | DAI | | | Device address match index<br><br>Index (n) of device address, see DAB[n] and DAP[n], that got an address match. |

## 22.14.8 PDUSTAT

Address offset: 0x414

Payload status

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | B B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | PDUSTAT | | | Status on payload length vs. PCNF1.MAXLEN |
| | | | LessThan | 0 | Payload less than PCNF1.MAXLEN |
| | | | GreaterThan | 1 | Payload greater than PCNF1.MAXLEN |
| B | R | CISTAT | | | Status on what rate packet is received with in Long Range |
| | | | LR125kbit | 0 | Frame is received at 125kbps |
| | | | LR500kbit | 1 | Frame is received at 500kbps |

## 22.14.9 PACKETPTR

Address offset: 0x504

Packet pointer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PACKETPTR | | | Packet pointer<br><br>Packet address to be used for the next transmission or reception. When transmitting, the packet pointed to by this address will be transmitted and when receiving, the received packet will be written to this address. This address is a byte aligned ram address. |

## 22.14.10 FREQUENCY

Address offset: 0x508

Frequency

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | B A A A A A A A |
| **Reset 0x00000002** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | FREQUENCY | | [0..100] | Radio channel frequency<br><br>Frequency = 2400 + FREQUENCY (MHz). |
| B | RW | MAP | | | Channel map selection. |
| | | | Default | 0 | Channel map between 2400 MHZ .. 2500 MHz<br><br>Frequency = 2400 + FREQUENCY (MHz) |
| | | | Low | 1 | Channel map between 2360 MHZ .. 2460 MHz<br><br>Frequency = 2360 + FREQUENCY (MHz) |

## 22.14.11 TXPOWER

Address offset: 0x50C

Output power

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TXPOWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos8dBm | 0x8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos7dBm | 0x7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos6dBm | 0x6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos5dBm | 0x5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos4dBm | 0x4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos3dBm | 0x3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pos2dBm | 0x2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0dBm | 0x0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg4dBm | 0xFC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg8dBm | 0xF8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg12dBm | 0xF4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg16dBm | 0xF0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg20dBm | 0xEC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Neg30dBm | 0xD8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Deprecated |
| | | | Neg40dBm | 0xD8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.12 MODE

Address offset: 0x510

Data rate and modulation

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Nrf_1Mbit | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Nrf_2Mbit | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ble_1Mbit | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ble_2Mbit | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ble_LR125Kbit | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ble_LR500Kbit | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ieee802154_250Kbit | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.13 PCNF0

Address offset: 0x514

Packet configuration register 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | J | J | | | I | H | H | G | G | | F | E | E | E | E | | | | | | | | C | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LFLEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | S0LEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | S1LEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | J | J | | | I | H | H | G | G | | F | E | E | E | E | | | | | | | | C | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | S1INCL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Automatic | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CILEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | PLEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 8bit | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 16bit | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 32bitZero | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LongRange | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CRCINC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | TERMLEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.14 PCNF1

Address offset: 0x518

Packet configuration register 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | E | D | | | | | | C | C | C | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MAXLEN | | [0..255] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Maximum length of packet payload. If the packet payload is larger than MAXLEN, the radio will truncate the payload to MAXLEN. |
| B | RW | STATLEN | | [0..255] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Static length in number of bytes<br><br>The static length parameter is added to the total length of the payload when sending and receiving packets, e.g. if the static length is set to N the radio will receive or send N bytes more than what is defined in the LENGTH field of the packet. |
| C | RW | BALEN | | [2..4] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Base address length in number of bytes<br><br>The address field is composed of the base address and the one byte long address prefix, e.g. set BALEN=2 to get a total address of 3 bytes. |
| D | RW | ENDIAN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | On air endianness of packet, this applies to the S0, LENGTH, S1 and the PAYLOAD fields. |
| | | | Little | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Big | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | WHITEEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.15 BASE0

Address offset: 0x51C

Base address 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BASE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Base address 0<br><br>Radio base address 0. |

## 22.14.16 BASE1

Address offset: 0x520

Base address 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | BASE1 | | | Base address 1<br><br>Radio base address 1. |

## 22.14.17 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | AP0 | | | Address prefix 0. |
| B | RW | AP1 | | | Address prefix 1. |
| C | RW | AP2 | | | Address prefix 2. |
| D | RW | AP3 | | | Address prefix 3. |

## 22.14.18 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | AP4 | | | Address prefix 4. |
| B | RW | AP5 | | | Address prefix 5. |
| C | RW | AP6 | | | Address prefix 6. |
| D | RW | AP7 | | | Address prefix 7. |

## 22.14.19 TXADDRESS

Address offset: 0x52C

Transmit address select

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TXADDRESS | | | Transmit address select<br><br>Logical address to be used when transmitting a packet. |

## 22.14.20 RXADDRESSES

Address offset: 0x530

Receive address select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | ADDR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ADDR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ADDR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ADDR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | ADDR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | ADDR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ADDR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.21 CRCCNF

Address offset: 0x534

CRC configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | B | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LEN | | [1..3] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | One | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Two | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Three | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SKIPADDR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Skip | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ieee802154 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Note:** For MODE Ble_LR125Kbit and Ble_LR500Kbit, only LEN set to 3 is supported

CRC length is zero and CRC calculation is disabled

CRC length is one byte and CRC calculation is enabled

CRC length is two bytes and CRC calculation is enabled

CRC length is three bytes and CRC calculation is enabled

Include or exclude packet address field out of CRC calculation.

CRC calculation includes address field

CRC calculation does not include address field. The CRC calculation will start at the first byte after the address.

CRC calculation as per 802.15.4 standard. Starting at first byte after length field.

## 22.14.22 CRCPOLY

Address offset: 0x538

CRC polynomial

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CRCPOLY | | | CRC polynomial<br><br>Each term in the CRC polynomial is mapped to a bit in this register which index corresponds to the term's exponent. The least significant term/bit is hard-wired internally to 1, and bit number 0 of the register content is ignored by the hardware. The following example is for an 8 bit CRC polynomial: x8 + x7 + x3 + x2 + 1 = 1 1000 1101 . |

## 22.14.23 CRCINIT

Address offset: 0x53C

CRC initial value

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CRCINIT | | | CRC initial value<br><br>Initial value for CRC calculation. |

## 22.14.24 TIFS

Address offset: 0x544

Inter Frame Spacing in us

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TIFS | | | Inter Frame Spacing in us<br><br>Inter frame space is the time interval between two consecutive packets. It is defined as the time, in micro seconds, from the end of the last bit of the previous packet to the start of the first bit of the subsequent packet. |

## 22.14.25 RSSISAMPLE

Address offset: 0x548

RSSI sample

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | RSSISAMPLE | | [0..127] | RSSI sample<br><br>RSSI sample result. The value of this register is read as a positive value while the actual received signal strength is a negative value. Actual received signal strength is therefore as follows: received signal strength = -A dBm |

## 22.14.26 STATE

Address offset: 0x550

Current radio state

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | STATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RxRu | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RxIdle | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Rx | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RxDisable | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | TxRu | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | TxIdle | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Tx | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | TxDisable | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.27 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000040** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DATAWHITEIV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Data whitening initial value. Bit 6 is hard-wired to '1', writing '0' to it has no effect, and it will always be read back and used by the device as '1'.

Bit 0 corresponds to Position 6 of the LSFR, Bit 1 to Position 5, etc.

## 22.14.28 BCC

Address offset: 0x560

Bit counter compare

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Bit counter compare

Bit counter compare register

## 22.14.29 DAB[0]

Address offset: 0x600

Device address base segment 0

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DAB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Device address base segment 0

## 22.14.30 DAB[1]

Address offset: 0x604

Device address base segment 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 1 |

## 22.14.31 DAB[2]

Address offset: 0x608

Device address base segment 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 2 |

## 22.14.32 DAB[3]

Address offset: 0x60C

Device address base segment 3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 3 |

## 22.14.33 DAB[4]

Address offset: 0x610

Device address base segment 4

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 4 |

## 22.14.34 DAB[5]

Address offset: 0x614

Device address base segment 5

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 5 |

## 22.14.35 DAB[6]

Address offset: 0x618

Device address base segment 6

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 6 |

## 22.14.36 DAB[7]

Address offset: 0x61C

Device address base segment 7

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAB | | | Device address base segment 7 |

## 22.14.37 DAP[0]

Address offset: 0x620

Device address prefix 0

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAP | | | Device address prefix 0 |

## 22.14.38 DAP[1]

Address offset: 0x624

Device address prefix 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAP | | | Device address prefix 1 |

## 22.14.39 DAP[2]

Address offset: 0x628

Device address prefix 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAP | | | Device address prefix 2 |

## 22.14.40 DAP[3]

Address offset: 0x62C

Device address prefix 3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DAP | | | Device address prefix 3 |

## 22.14.41 DAP[4]

Address offset: 0x630

Device address prefix 4

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DAP | | | Device address prefix 4 |

## 22.14.42 DAP[5]

Address offset: 0x634

Device address prefix 5

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DAP | | | Device address prefix 5 |

## 22.14.43 DAP[6]

Address offset: 0x638

Device address prefix 6

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DAP | | | Device address prefix 6 |

## 22.14.44 DAP[7]

Address offset: 0x63C

Device address prefix 7

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DAP | | | Device address prefix 7 |

## 22.14.45 DACNF

Address offset: 0x640

Device address match configuration

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENA0 | | | Enable or disable device address matching using device address 0 |
| | | | Disabled | 0 | Disabled |
| | | | Enabled | 1 | Enabled |
| B | RW | ENA1 | | | Enable or disable device address matching using device address 1 |
| | | | Disabled | 0 | Disabled |
| | | | Enabled | 1 | Enabled |
| C | RW | ENA2 | | | Enable or disable device address matching using device address 2 |
| | | | Disabled | 0 | Disabled |
| | | | Enabled | 1 | Enabled |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| D | RW | ENA3 | | | | | | | | | | | | | | | | | | Enable or disable device address matching using device address 3 | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | Enabled | | | | | | | | | | | | | | | |
| E | RW | ENA4 | | | | | | | | | | | | | | | | | | Enable or disable device address matching using device address 4 | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | Enabled | | | | | | | | | | | | | | | |
| F | RW | ENA5 | | | | | | | | | | | | | | | | | | Enable or disable device address matching using device address 5 | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | Enabled | | | | | | | | | | | | | | | |
| G | RW | ENA6 | | | | | | | | | | | | | | | | | | Enable or disable device address matching using device address 6 | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | Enabled | | | | | | | | | | | | | | | |
| H | RW | ENA7 | | | | | | | | | | | | | | | | | | Enable or disable device address matching using device address 7 | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | Disabled | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | Enabled | | | | | | | | | | | | | | | |
| I | RW | TXADD0 | | | | | | | | | | | | | | | | | | TxAdd for device address 0 | | | | | | | | | | | | | | | |
| J | RW | TXADD1 | | | | | | | | | | | | | | | | | | TxAdd for device address 1 | | | | | | | | | | | | | | | |
| K | RW | TXADD2 | | | | | | | | | | | | | | | | | | TxAdd for device address 2 | | | | | | | | | | | | | | | |
| L | RW | TXADD3 | | | | | | | | | | | | | | | | | | TxAdd for device address 3 | | | | | | | | | | | | | | | |
| M | RW | TXADD4 | | | | | | | | | | | | | | | | | | TxAdd for device address 4 | | | | | | | | | | | | | | | |
| N | RW | TXADD5 | | | | | | | | | | | | | | | | | | TxAdd for device address 5 | | | | | | | | | | | | | | | |
| O | RW | TXADD6 | | | | | | | | | | | | | | | | | | TxAdd for device address 6 | | | | | | | | | | | | | | | |
| P | RW | TXADD7 | | | | | | | | | | | | | | | | | | TxAdd for device address 7 | | | | | | | | | | | | | | | |

## 22.14.46 MHRMATCHCONF

Address offset: 0x644

Search Pattern Configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |

## 22.14.47 MHRMATCHMAS

Address offset: 0x648

Pattern mask

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |

## 22.14.48 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | C | C | | | | | | | | A |
| **Reset 0x00000200** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | RU | | | | | | | | | | | | | | | | | | | | | | | Radio ramp-up time | | | | | | | | | |
| | | | Default | | | | | | | | 0 | | | | | | | | | | | | | | Default ramp-up time (tRXEN), compatible with firmware written for nRF51 | | | | | | | | | |
| | | | Fast | | | | | | | | 1 | | | | | | | | | | | | | | Fast ramp-up (tRXEN,FAST), see electrical specification for more information | | | | | | | | | |
| C | RW | DTX | | | | | | | | | | | | | | | | | | | | | | | Default TX value<br>Specifies what the RADIO will transmit when it is not started, i.e. between:<br>RADIO.EVENTS_READY and RADIO.TASKS_START<br>RADIO.EVENTS_END and RADIO.TASKS_START<br>RADIO.EVENTS_END and RADIO.EVENTS_DISABLED | | | | | | | | | |
| | | | B1 | | | | | | | | 0 | | | | | | | | | | | | | | Transmit '1' | | | | | | | | | |
| | | | B0 | | | | | | | | 1 | | | | | | | | | | | | | | Transmit '0' | | | | | | | | | |
| | | | Center | | | | | | | | 2 | | | | | | | | | | | | | | Transmit center frequency<br>When tuning the crystal for centre frequency, the RADIO must be set in DTX = Center mode to be able to achieve the expected accuracy. This is only a valid setting for Nrf_1Mbit, Nrf_2Mbit, Ble_1Mbit and Ble_2Mbit. | | | | | | | | | |

## 22.14.49 SFD

Address offset: 0x660

IEEE 802.15.4 Start of Frame Delimiter

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x000000A7** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | SFD | | | | | | | | | | | | | | | | | | | | | | | IEEE 802.15.4 Start of Frame Delimiter. Note, the least significant 4-bits of the SFD cannot all be zeros. | | | | | | | | | |

## 22.14.50 EDCNT

Address offset: 0x664

IEEE 802.15.4 Energy Detect Loop Count

Number of iterations to perform an ED scan. If set to 0 one scan is performed, otherwise the specified number + 1 of ED scans will be performed and the max ED value tracked in EDSAMPLE

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | EDCNT | | | | | | | | | | | | | | | | | | | | | | | IEEE 802.15.4 Energy Detect Loop Count | | | | | | | | | |

## 22.14.51 EDSAMPLE

Address offset: 0x668

IEEE 802.15.4 Energy Detect Level

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EDLVL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | IEEE 802.15.4 Energy Detect Level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.52 CCACTRL

Address offset: 0x66C

IEEE 802.15.4 Clear Channel Assessment Control

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CCAMODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | CCA Mode Of Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EdMode | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Energy Above Threshold<br>Will report busy whenever energy is detected above CCAEDTHRES | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CarrierMode | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Carrier Seen<br>Will report busy whenever compliant IEEE 802.15.4 signal is seen | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CarrierAndEdMode | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Energy Above Threshold AND Carrier Seen | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CarrierOrEdMode | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Energy Above Threshold OR Carrier Seen | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EdModeTest1 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Energy Above Threshold test mode that will abort when first ED measurement over threshold is seen. No averaging. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CCAEDTHRES | | CCA Energy Busy Threshold. Used in all the CCA modes except CarrierMode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CCACORRTHRES | | CCA Correlator Busy Threshold. Only relevant to CarrierMode, CarrierAndEdMode and CarrierOrEdMode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CCACORRCNT | | Limit for occurances above CCACORRTHRES. When not equal to zero the corrolator based signal detect is enabled. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 22.14.53 POWER

Address offset: 0xFFC

Peripheral power control

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Peripheral power control. The peripheral and its registers will be reset to its initial state by switching the peripheral off and then back on again. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Peripheral is powered off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Peripheral is powered on | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 22.15 Electrical specification

## 22.15.1 General Radio Characteristics

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{OP}$ | Operating frequencies | 2360 | | 2500 | MHz |
| $f_{PLL,CH,SP}$ | PLL channel spacing | | 1 | | MHz |
| $f_{DELTA,1M}$ | Frequency deviation @ 1 Mbps | | ±170 | | kHz |
| $f_{DELTA,BLE,1M}$ | Frequency deviation @ BLE 1Mbps | | ±250 | | kHz |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{DELTA,2M}$ | Frequency deviation @ 2 Mbps | | ±320 | | kHz |
| $fsk_{BPS}$ | On-the-air data rate | 125 | | 2000 | kbps |
| $f_{chip,\ IEEE\ 802.15.4}$ | Chip rate in IEEE 802.15.4 mode | | 2000 | | kchip/s |

## 22.15.2 Radio current consumption (Transmitter)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{TX,PLUS8dBM,DCDC}$ | TX only run current (DCDC, 3V) $P_{RF}$ =+8 dBm | | 14.1 | | mA |
| $I_{TX,PLUS8dBM}$ | TX only run current $P_{RF}$ = +8 dBm | | 30.4 | | mA |
| $I_{TX,PLUS4dBM,DCDC}$ | TX only run current (DCDC, 3V) $P_{RF}$ =+4 dBm | | 9.3 | | mA |
| $I_{TX,PLUS4dBM}$ | TX only run current $P_{RF}$ = +4 dBm | | 18.9 | | mA |
| $I_{TX,0dBM,DCDC,5V,REG0HI}$ | TX only run current (DCDC, 5V, REG0 out = 3.3 V)$P_{RF}$ = 0dBm | | 6.0 | | mA |
| $I_{TX,0dBM,DCDC,5V,REG0LO}$ | TX only run current (DCDC, 5V, REG0 out = 1.8 V)$P_{RF}$ = 0dBm | | 5.2 | | mA |
| $I_{TX,0dBM,DCDC}$ | TX only run current (DCDC, 3V)$P_{RF}$ = 0dBm | | 4.9 | | mA |
| $I_{TX,0dBM}$ | TX only run current $P_{RF}$ = 0dBm | | 10.2 | | mA |
| $I_{TX,MINUS4dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -4dBm | | 3.4 | | mA |
| $I_{TX,MINUS4dBM}$ | TX only run current $P_{RF}$ = -4 dBm | | 7.3 | | mA |
| $I_{TX,MINUS8dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -8 dBm | | 3.0 | | mA |
| $I_{TX,MINUS8dBM}$ | TX only run current $P_{RF}$ = -8 dBm | | 6.4 | | mA |
| $I_{TX,MINUS12dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -12 dBm | | 2.7 | | mA |
| $I_{TX,MINUS12dBM}$ | TX only run current $P_{RF}$ = -12 dBm | | 5.7 | | mA |
| $I_{TX,MINUS16dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -16 dBm | | 2.5 | | mA |
| $I_{TX,MINUS16dBM}$ | TX only run current $P_{RF}$ = -16 dBm | | 5.3 | | mA |
| $I_{TX,MINUS20dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -20 dBm | | 2.3 | | mA |
| $I_{TX,MINUS20dBM}$ | TX only run current $P_{RF}$ = -20 dBm | | 5.0 | | mA |
| $I_{TX,MINUS40dBM,DCDC}$ | TX only run current DCDC, 3V $P_{RF}$ = -40 dBm | | 2.0 | | mA |
| $I_{TX,MINUS40dBM}$ | TX only run current $P_{RF}$ = -40 dBm | | 4.0 | | mA |
| $I_{START,TX,DCDC}$ | TX start-up current DCDC, 3V, $P_{RF}$ = 4 dBm | | 5.2 | | mA |
| $I_{START,TX}$ | TX start-up current, $P_{RF}$ = 4 dBm | | 11.0 | | mA |
| $I_{0dBm\ (DCDC,\ 3V)}$ | TX current (DCDC 3V) 1Mbps BLE measured from VBAT with $P_{RF}$=0dBm | | 6.4 | | mA |
| $I_{2dBm\ (DCDC,\ 3V)}$ | TX current (DCDC 3V) 1Mbps BLE measured from VBAT with $P_{RF}$=2dBm | | 8.9 | | mA |
| $I_{4dBm\ (DCDC,\ 3V)}$ | TX current (DCDC 3V) 1Mbps BLE measured from VBAT with $P_{RF}$=4dBm | | 10.6 | | mA |
| $I_{9dBm\ (DCDC,\ 3V)}$ | TX current (DCDC 3V) 1Mbps BLE measured from VBAT with $P_{RF}$=9dBm | | 15.5 | | mA |
| $I_{0dBm\ (3V)}$ | TX current (3V) 1Mbps BLE measured from VBAT with $P_{RF}$=0dBm | | 11.2 | | mA |
| $I_{9dBm\ (3V)}$ | TX current (3V) 1Mbps BLE measured from VBAT with $P_{RF}$=9dBm | | 30.7 | | mA |

## 22.15.3 Radio current consumption (Receiver)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{RX,1M,DCDC}$ | RX only run current (DCDC, 3V) 1Mbps / 1Mbps BLE | | 4.8 | | mA |
| $I_{RX,1M}$ | RX only run current (LDO, 3V) 1Mbps / 1Mbps BLE | | 10.3 | | mA |
| $I_{RX,2M,DCDC}$ | RX only run current (DCDC, 3V) 2Mbps / 2Mbps BLE | | 5.4 | | mA |
| $I_{RX,2M}$ | RX only run current (LDO, 3V) 2Mbps / 2Mbps BLE | | 11.6 | | mA |
| $I_{START,RX,1M,DCDC}$ | RX start-up current (DCDC 3V) 1Mbps / 1Mbps BLE | | 3.7 | | mA |
| $I_{START,RX,1M}$ | RX start-up current 1Mbps / 1Mbps BLE | | 6.7 | | mA |

## 22.15.4 Transmitter specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $P_{RF}$ | Maximum output power | | 8 | | dBm |
| $P_{RFC}$ | RF power control range | | 28 | | dB |
| $P_{RFCR}$ | RF power accuracy | | | ±4 | dB |
| $P_{RF1,1}$ | 1st Adjacent Channel Transmit Power 1 MHz (1 Mbps) | | -23 | | dBc |

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $P_{RF2,1}$ | 2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps) | | -50 | | dBc |
| $P_{RF1,2}$ | 1st Adjacent Channel Transmit Power 2 MHz (2 Mbps) | | -24 | | dBc |
| $P_{RF2,2}$ | 2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps) | | -50 | | dBc |
| $E_{vm}$ | Error Vector Magnitude IEEE 802.15.4 | | | | %rms |
| $P_{harm2nd, IEEE 802.15.4}$ | 2nd Harmonics in IEEE 802.15.4 mode | | | | dBm |
| $P_{harm3rd, IEEE 802.15.4}$ | 3rd Harmonics in IEEE 802.15.4 | | | | dBm |

## 22.15.5 Receiver operation

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $P_{RX,MAX}$ | Maximum received signal strength at < 0.1% PER | | 0 | | dBm |
| $P_{SENS,IT,1M}$ | Sensitivity, 1Mbps nRF mode[13] | | -93 | | dBm |
| $P_{SENS,IT,SP,1M,BLE}$ | Sensitivity, 1Mbps BLE ideal transmitter, <=37 bytes BER=1E-3[14] | | -95 | | dBm |
| $P_{SENS,IT,LP,1M,BLE}$ | Sensitivity, 1Mbps BLE ideal transmitter >=128 bytes BER=1E-4 [15] | | -95 | | dBm |
| $P_{SENS,IT,2M}$ | Sensitivity, 2Mbps nRF mode[16] | | -89 | | dBm |
| $P_{SENS,IT,SP,2M,BLE}$ | Sensitivity, 2Mbps BLE ideal transmitter, Packet length <=37bytes | | -92 | | dBm |
| $P_{SENS,IT,BLE LE125k}$ | Sensitivity, 125kbps BLE mode | | -103 | | dBm |
| $P_{SENS,IT,BLE LE500k}$ | Sensitivity, 500kbps BLE mode | | -99 | | dBm |
| $P_{sense, IEEE 802.15.4}$ | Sensitivity in IEEE 802.15.4 mode | | -100 | | dBm |

## 22.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal[17]

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C/I_{1M,co-channel}$ | 1Mbps mode, Co-Channel interference | | 9 | | dB |
| $C/I_{1M,-1MHz}$ | 1 Mbps mode, Adjacent (-1 MHz) interference | | -2 | | dB |
| $C/I_{1M,+1MHz}$ | 1 Mbps mode, Adjacent (+1 MHz) interference | | -10 | | dB |
| $C/I_{1M,-2MHz}$ | 1 Mbps mode, Adjacent (-2 MHz) interference | | -19 | | dB |
| $C/I_{1M,+2MHz}$ | 1 Mbps mode, Adjacent (+2 MHz) interference | | -42 | | dB |
| $C/I_{1M,-3MHz}$ | 1 Mbps mode, Adjacent (-3 MHz) interference | | -38 | | dB |
| $C/I_{1M,+3MHz}$ | 1 Mbps mode, Adjacent (+3 MHz) interference | | -48 | | dB |
| $C/I_{1M,\pm6MHz}$ | 1 Mbps mode, Adjacent (≥6 MHz) interference | | -50 | | dB |
| $C/I_{1MBLE,co-channel}$ | 1 Mbps BLE mode, Co-Channel interference | | 6 | | dB |
| $C/I_{1MBLE,-1MHz}$ | 1 Mbps BLE mode, Adjacent (-1 MHz) interference | | -2 | | dB |
| $C/I_{1MBLE,+1MHz}$ | 1 Mbps BLE mode, Adjacent (+1 MHz) interference | | -9 | | dB |
| $C/I_{1MBLE,-2MHz}$ | 1 Mbps BLE mode, Adjacent (-2 MHz) interference | | -22 | | dB |
| $C/I_{1MBLE,+2MHz}$ | 1 Mbps BLE mode, Adjacent (+2 MHz) interference | | -46 | | dB |
| $C/I_{1MBLE,>3MHz}$ | 1 Mbps BLE mode, Adjacent (≥3 MHz) interference | | -50 | | dB |
| $C/I_{1MBLE,image}$ | Image frequency Interference | | -22 | | dB |
| $C/I_{1MBLE,image,1MHz}$ | Adjacent (1 MHz) interference to in-band image frequency | | -35 | | dB |
| $C/I_{2M,co-channel}$ | 2Mbps mode, Co-Channel interference | | 10 | | dB |
| $C/I_{2M,-2MHz}$ | 2 Mbps mode, Adjacent (-2 MHz) interference | | 6 | | dB |
| $C/I_{2M,+2MHz}$ | 2 Mbps mode, Adjacent (+2 MHz) interference | | -19 | | dB |
| $C/I_{2M,-4MHz}$ | 2 Mbps mode, Adjacent (-4 MHz) interference | | -20 | | dB |
| $C/I_{2M,+4MHz}$ | 2 Mbps mode, Adjacent (+4 MHz) interference | | -44 | | dB |
| $C/I_{2M,-6MHz}$ | 2 Mbps mode, Adjacent (-6 MHz) interference | | -42 | | dB |

[13] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

[14] As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

[15] Equivalent BER limit < 10E-04

[16] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

[17] Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C/I_{2M,+6MHz}$ | 2 Mbps mode, Adjacent (+6 MHz) interference | | -42 | | dB |
| $C/I_{2M,\geq 12MHz}$ | 2 Mbps mode, Adjacent (≥12 MHz) interference | | -52 | | dB |
| $C/I_{125k\ BLE\ LR,co\text{-}channel}$ | 125 kbps BLE LR mode, Co-Channel interference | | | | dB |
| $C/I_{125k\ BLE\ LR,-1MHz}$ | 125 kbps BLE LR mode, Adjacent (-1 MHz) interference | | | | dB |
| $C/I_{125k\ BLE\ LR,+1MHz}$ | 125 kbps BLE LR mode, Adjacent (+1 MHz) interference | | | | dB |
| $C/I_{125k\ BLE\ LR,-2MHz}$ | 125 kbps BLE LR mode, Adjacent (-2 MHz) interference | | | | dB |
| $C/I_{125k\ BLE\ LR,+2MHz}$ | 125 kbps BLE LR mode, Adjacent (+2 MHz) interference | | | | dB |
| $C/I_{125k\ BLE\ LR,>3MHz}$ | 125 kbps BLE LR mode, Adjacent (≥3 MHz) interference | | | | dB |
| $C/I_{125k\ BLE\ LR,image}$ | Image frequency Interference | | | | dB |
| $C/I_{500k\ BLE\ LR,co\text{-}channel}$ | 500 kbps BLE LR mode, Co-Channel interference | | | | dB |
| $C/I_{500k\ BLE\ LR,-1MHz}$ | 500 kbps BLE LR mode, Adjacent (-1 MHz) interference | | | | dB |
| $C/I_{500k\ BLE\ LR,+1MHz}$ | 500 kbps BLE LR mode, Adjacent (+1 MHz) interference | | | | dB |
| $C/I_{500k\ BLE\ LR,-2MHz}$ | 500 kbps BLE LR mode, Adjacent (-2 MHz) interference | | | | dB |
| $C/I_{500k\ BLE\ LR,+2MHz}$ | 500 kbps BLE LR mode, Adjacent (+2 MHz) interference | | | | dB |
| $C/I_{500k\ BLE\ LR,>3MHz}$ | 500 kbps BLE LR mode, Adjacent (≥3 MHz) interference | | | | dB |
| $C/I_{500k\ BLE\ LR,image}$ | Image frequency Interference | | | | dB |

## 22.15.7 RX intermodulation

RX intermodulation[18]

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $P_{IMD,1M}$ | IMD performance, 1 Mbps, 3rd, 4th, and 5th offset channel | | -29 | | dBm |
| $P_{IMD,1M,BLE}$ | IMD performance, BLE 1 Mbps, 3rd, 4th, and 5th offset channel | | -30 | | dBm |
| $P_{IMD,2M}$ | IMD performance, 2 Mbps, 3rd, 4th, and 5th offset channel | | -30 | | dBm |

## 22.15.8 Radio timing

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TXEN}$ | Time between TXEN task and READY event after channel FREQUENCY configured | | 140 | | us |
| $t_{TXEN,FAST}$ | Time between TXEN task and READY event after channel FREQUENCY configured (Fast Mode) | | 40 | | us |
| $t_{TXDISABLE}$ | Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 1Mbps | | 6 | | us |
| $t_{TXDISABLE,2M}$ | Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 2Mbps | .. | .. | .. | us |
| $t_{RXEN}$ | Time between the RXEN task and READY event after channel FREQUENCY configured in default mode | | 140 | | us |
| $t_{RXEN,FAST}$ | Time between the RXEN task and READY event after channel FREQUENCY configured in fast mode | | 40 | | us |
| $t_{RXDISABLE}$ | Time between DISABLE task and DISABLED event when the radio was in RX | | 0 | | us |
| $t_{TXCHAIN}$ | TX chain delay | | 0.6 | | us |
| $t_{RXCHAIN}$ | RX chain delay | | 9.4 | | us |
| $t_{RXCHAIN,2M}$ | RX chain delay in 2Mbps mode | | 5 | | us |
| $t_{RXCHAIN,LR\ 125k}$ | RX chain delay in BLE LR125kbps mode | .. | .. | .. | us |
| $t_{RXCHAIN,LR\ 500k}$ | RX chain delay in BLE LR500kbps mode | .. | .. | .. | us |
| $t_{RX\text{-}to\text{-}TX\ turnaround}$ | Maximum TX-to-RX or RX-to-TX turnaround time in IEEE 802.15.4 mode | .. | .. | .. | us |

## 22.15.9 Received Signal Strength Indicator (RSSI) specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $RSSI_{ACC}$ | RSSI Accuracy Valid range -90 to -20 dBm | | -2 | | dB |

[18] Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $RSSI_{RESOLUTION}$ | RSSI resolution | | 1 | | dB |
| $RSSI_{PERIOD}$ | Sample period | | 8 | | us |
| $RSSI_{min,\ IEEE\ 802.15.4}$ | Minimum RSSI sensitivity in 802.15.4 mode | | | | dBm |

## 22.15.10 Jitter

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{DISABLEDJITTER}$ | Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled. | | 0.25 | | us |
| $t_{READYJITTER}$ | Jitter on READY event relative to TXEN and RXEN task. | | 0.25 | | us |

## 22.15.11 Delay when disabling the RADIO

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TXDISABLE,1M}$ | Disable delay from TX.<br>Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit | | 6 | | us |
| $t_{RXDISABLE,1M}$ | Disable delay from RX.<br>Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit | | 0 | | us |

# 23 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

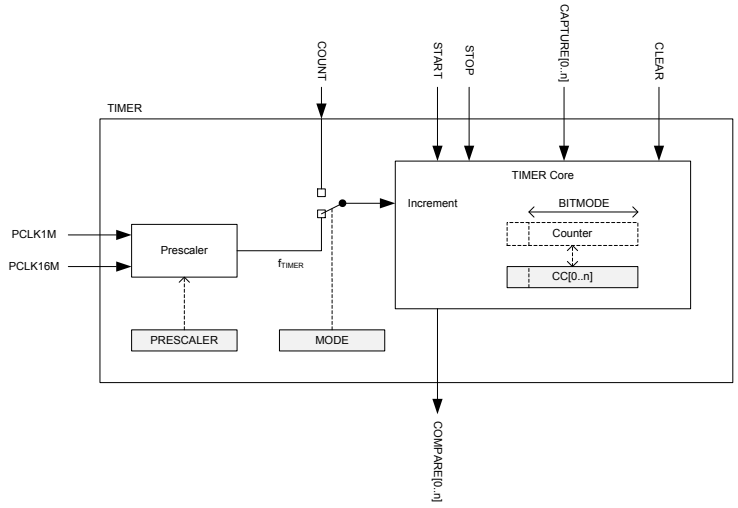



**Figure 51: Block schematic for timer/counter**

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

The status (Started or Stopped) of each TIMER instance can be checked by reading its STATUS register.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency $f_{TIMER}$ as illustrated in *Figure 51: Block schematic for timer/counter* on page 292. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

$$f_{TIMER} = 16\ MHz\ /\ (2^{PRESCALER})$$

When $f_{TIMER}$ <= 1 MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 297 register.

*PRESCALER* on page 298 and the *BITMODE* on page 297 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.

When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency $f_{TIMER}$ as illustrated in *Figure 51: Block schematic for timer/counter* on page 292.

## 23.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

## 23.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

*BITMODE* on page 297 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

## 23.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

## 23.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

## 23.5 Registers

**Table 36: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40008000 | TIMER | TIMER0 | Timer 0 | This timer instance has 4 CC registers (CC[0..3]) |
| 0x40009000 | TIMER | TIMER1 | Timer 1 | This timer instance has 4 CC registers (CC[0..3]) |
| 0x4000A000 | TIMER | TIMER2 | Timer 2 | This timer instance has 4 CC registers (CC[0..3]) |
| 0x4001A000 | TIMER | TIMER3 | Timer 3 | This timer instance has 6 CC registers (CC[0..5]) |
| 0x4001B000 | TIMER | TIMER4 | Timer 4 | This timer instance has 6 CC registers (CC[0..5]) |

### Table 37: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| TASKS_START | 0x000 | Start Timer | |
| TASKS_STOP | 0x004 | Stop Timer | |
| TASKS_COUNT | 0x008 | Increment Timer (Counter mode only) | |
| TASKS_CLEAR | 0x00C | Clear time | |
| TASKS_SHUTDOWN | 0x010 | Shut down timer | Deprecated |
| TASKS_CAPTURE[0] | 0x040 | Capture Timer value to CC[0] register | |
| TASKS_CAPTURE[1] | 0x044 | Capture Timer value to CC[1] register | |
| TASKS_CAPTURE[2] | 0x048 | Capture Timer value to CC[2] register | |
| TASKS_CAPTURE[3] | 0x04C | Capture Timer value to CC[3] register | |
| TASKS_CAPTURE[4] | 0x050 | Capture Timer value to CC[4] register | |
| TASKS_CAPTURE[5] | 0x054 | Capture Timer value to CC[5] register | |
| EVENTS_COMPARE[0] | 0x140 | Compare event on CC[0] match | |
| EVENTS_COMPARE[1] | 0x144 | Compare event on CC[1] match | |
| EVENTS_COMPARE[2] | 0x148 | Compare event on CC[2] match | |
| EVENTS_COMPARE[3] | 0x14C | Compare event on CC[3] match | |
| EVENTS_COMPARE[4] | 0x150 | Compare event on CC[4] match | |
| EVENTS_COMPARE[5] | 0x154 | Compare event on CC[5] match | |
| *SHORTS* | 0x200 | Shortcut register | |
| *INTENSET* | 0x304 | Enable interrupt | |
| *INTENCLR* | 0x308 | Disable interrupt | |
| *STATUS* | 0x400 | Timer status | |
| *MODE* | 0x504 | Timer mode selection | |
| *BITMODE* | 0x508 | Configure the number of bits used by the TIMER | |
| *PRESCALER* | 0x510 | Timer prescaler register | |
| *CC[0]* | 0x540 | Capture/Compare register 0 | |
| *CC[1]* | 0x544 | Capture/Compare register 1 | |
| *CC[2]* | 0x548 | Capture/Compare register 2 | |
| *CC[3]* | 0x54C | Capture/Compare register 3 | |
| *CC[4]* | 0x550 | Capture/Compare register 4 | |
| *CC[5]* | 0x554 | Capture/Compare register 5 | |

## 23.5.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | L | K | J | I | H | G | | | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | | | | | | | | | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | COMPARE0_CLEAR | | | Shortcut between COMPARE[0] event and CLEAR task |
| | | | | | See *EVENTS_COMPARE[0]* and *TASKS_CLEAR* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | COMPARE1_CLEAR | | | Shortcut between COMPARE[1] event and CLEAR task |
| | | | | | See *EVENTS_COMPARE[1]* and *TASKS_CLEAR* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| C | RW | COMPARE2_CLEAR | | | Shortcut between COMPARE[2] event and CLEAR task |
| | | | | | See *EVENTS_COMPARE[2]* and *TASKS_CLEAR* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| D | RW | COMPARE3_CLEAR | | | Shortcut between COMPARE[3] event and CLEAR task |
| | | | | | See *EVENTS_COMPARE[3]* and *TASKS_CLEAR* |
| | | | Disabled | 0 | Disable shortcut |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | L | K | J | I | H | G | | | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | COMPARE4_CLEAR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[4]* and *TASKS_CLEAR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE5_CLEAR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[5]* and *TASKS_CLEAR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | COMPARE0_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[0]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | COMPARE1_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[1]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | COMPARE2_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[2]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | COMPARE3_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[3]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | COMPARE4_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[4]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | COMPARE5_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[5]* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 23.5.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | F | E | D | C | B | A | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | COMPARE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[0]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | COMPARE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[1]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | F | E | D | C | B | A | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | COMPARE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[2]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | COMPARE3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[3]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | COMPARE4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[4]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[5]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 23.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | F | E | D | C | B | A | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | COMPARE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[0]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | COMPARE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[1]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | COMPARE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[2]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | COMPARE3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COMPARE[3]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| E | RW | COMPARE4 | | | Write '1' to Disable interrupt for COMPARE[4] event<br><br>See *EVENTS_COMPARE[4]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | COMPARE5 | | | Write '1' to Disable interrupt for COMPARE[5] event<br><br>See *EVENTS_COMPARE[5]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 23.5.4 STATUS

Address offset: 0x400

Timer status

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | STATUS | | | Timer status |
| | | | Stopped | 0 | Timer is stopped |
| | | | Started | 1 | Timer is started |

## 23.5.5 MODE

Address offset: 0x504

Timer mode selection

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | MODE | | | Timer mode |
| | | | Timer | 0 | Select Timer mode |
| | | | Counter | 1 | Select Counter mode Deprecated |
| | | | LowPowerCounter | 2 | Select Low Power Counter mode |

## 23.5.6 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | BITMODE | | | Timer bit width |
| | | | 16Bit | 0 | 16 bit timer bit width |
| | | | 08Bit | 1 | 8 bit timer bit width |
| | | | 24Bit | 2 | 24 bit timer bit width |
| | | | 32Bit | 3 | 32 bit timer bit width |

### 23.5.7 PRESCALER

Address offset: 0x510

Timer prescaler register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000004** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PRESCALER | | [0..9] | Prescaler value |

### 23.5.8 CC[0]

Address offset: 0x540

Capture/Compare register 0

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

### 23.5.9 CC[1]

Address offset: 0x544

Capture/Compare register 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

### 23.5.10 CC[2]

Address offset: 0x548

Capture/Compare register 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

### 23.5.11 CC[3]

Address offset: 0x54C

Capture/Compare register 3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

### 23.5.12 CC[4]

Address offset: 0x550

Capture/Compare register 4

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

### 23.5.13 CC[5]

Address offset: 0x554

Capture/Compare register 5

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CC | | | Capture/Compare value<br><br>Only the number of bits indicated by BITMODE will be used by the TIMER. |

## 23.6 Electrical specification

### 23.6.1 Timers Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{TIMER\_1M}$ | Run current with 1 MHz clock input (PCLK1M) | 3 | 5 | 8 | µA |
| $I_{TIMER\_16M}$ | Run current with 16 MHz clock input (PCLK16M) | 50 | 70 | 120 | µA |
| $t_{TIMER,START}$ | Time from START task is given until timer starts counting | | 0.25 | | µs |

# 24 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

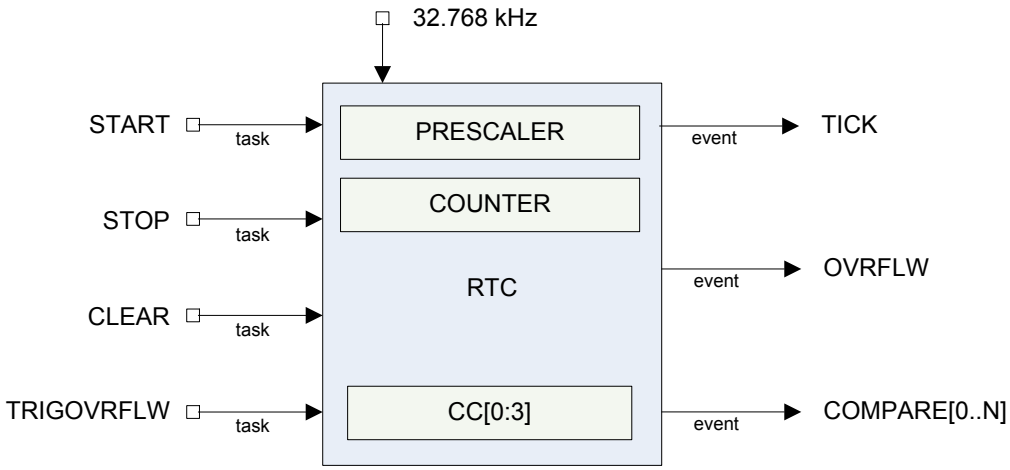



**Figure 52: RTC block schematic**

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

## 24.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be 30.517 µs. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See *CLOCK — Clock control* on page 141 for more information about clock sources.

## 24.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

$$f_{RTC}\ [kHz] = 32.768\ /\ (PRESCALER + 1\ )$$

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

   PRESCALER = round(32.768 kHz / 100 Hz) - 1 = 327

   $f_{RTC}$ = 99.9 Hz

10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

   PRESCALER = round(32.768 kHz / 8 Hz) – 1 = 4095

   $f_{RTC}$ = 8 Hz

   125 ms counter period

**Table 38: RTC resolution versus overflow**

| Prescaler | Counter resolution | Overflow |
|---|---|---|
| 0 | 30.517 µs | 512 seconds |
| $2^8$-1 | 7812.5 µs | 131072 seconds |
| $2^{12}$-1 | 125 ms | 582.542 hours |

## 24.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

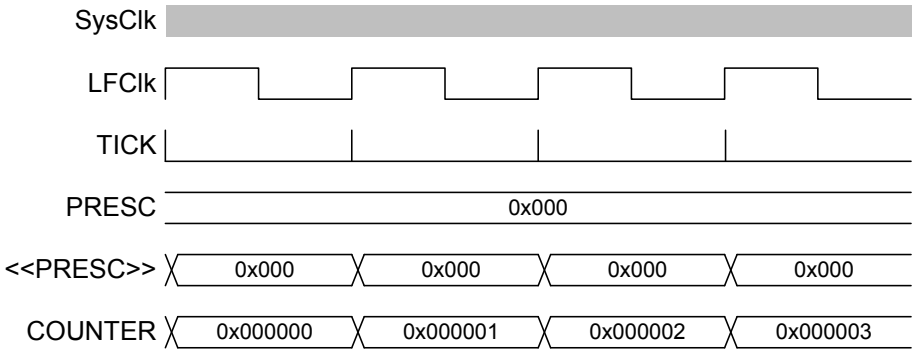



**Figure 53: Timing diagram - COUNTER_PRESCALER_0**

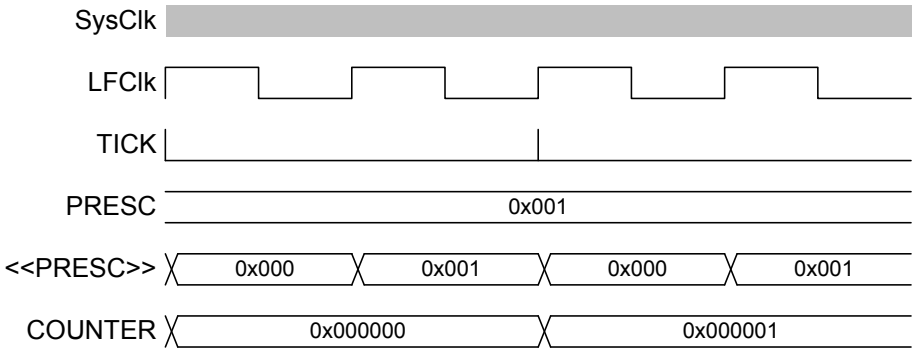



**Figure 54: Timing diagram - COUNTER_PRESCALER_1**

## 24.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

**Important:** The OVRFLW event is disabled by default.

## 24.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.

Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

**Important:** The TICK event is disabled by default.

## 24.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Peripheral interface* on page 59. The RTC task and event system is illustrated in *Figure 55: Tasks, events and interrupts in the RTC* on page 302.

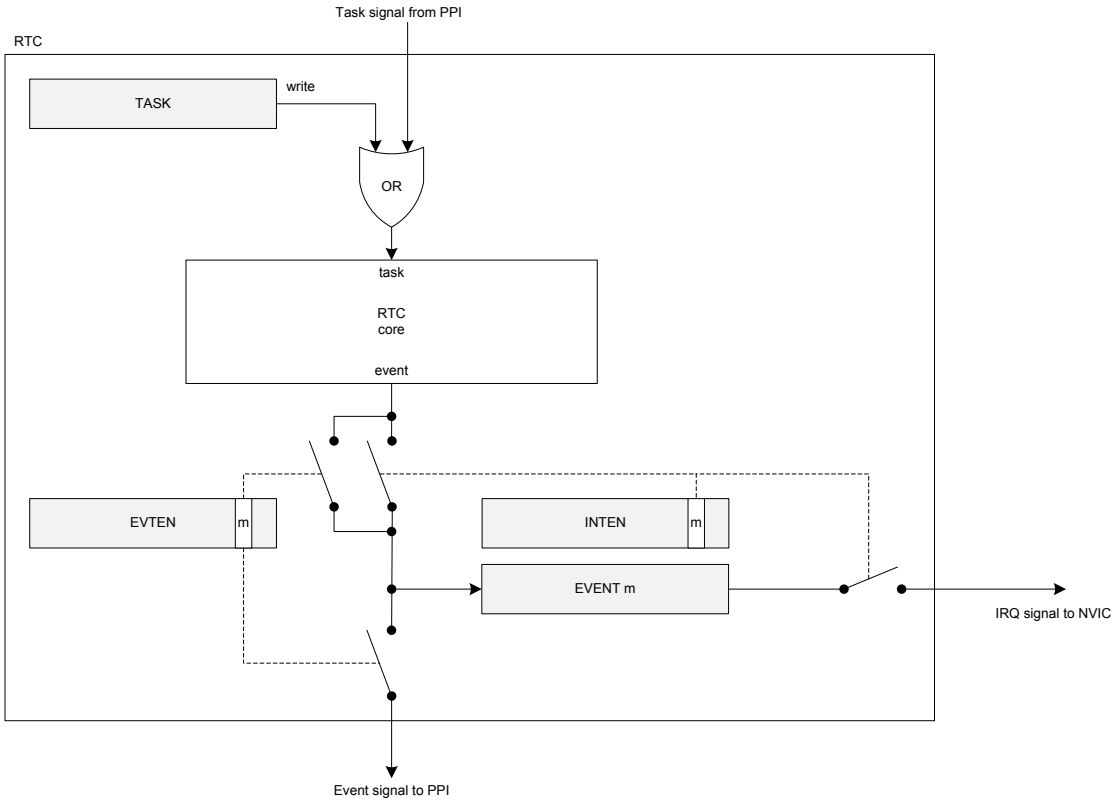



**Figure 55: Tasks, events and interrupts in the RTC**

## 24.7 Compare feature

There are a number of Compare registers.

For more information, see *Registers* on page 306.

When setting a compare register, the following behavior of the RTC compare event should be noted:

- If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.

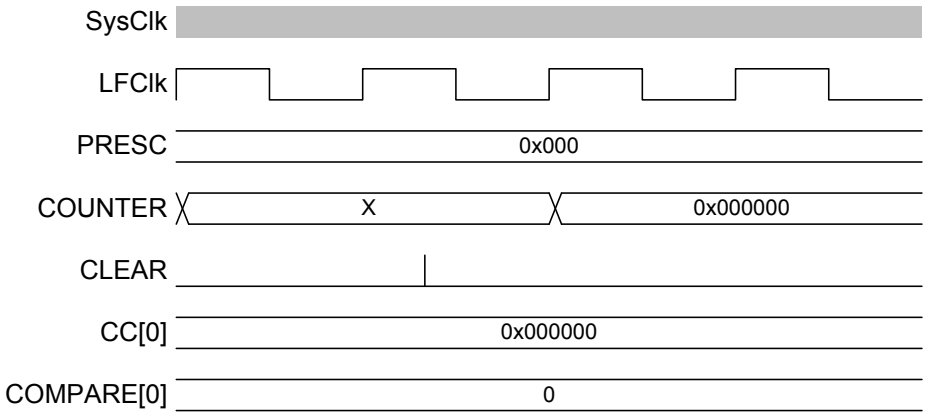



**Figure 56: Timing diagram - COMPARE_CLEAR**

- If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

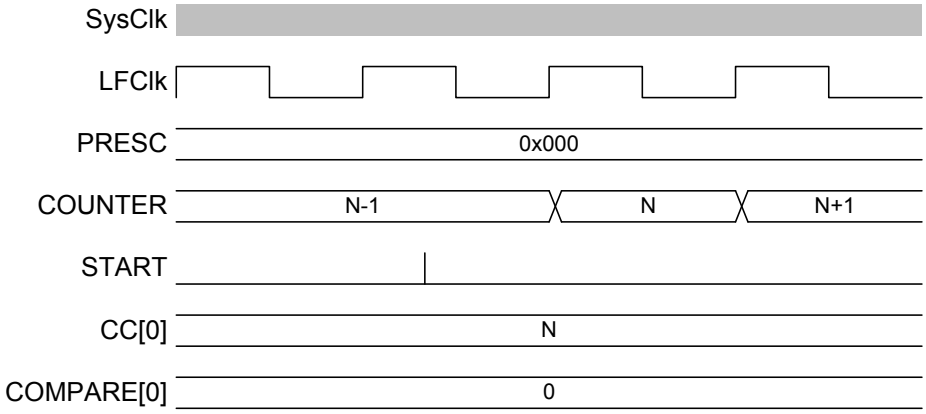



**Figure 57: Timing diagram - COMPARE_START**

- COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

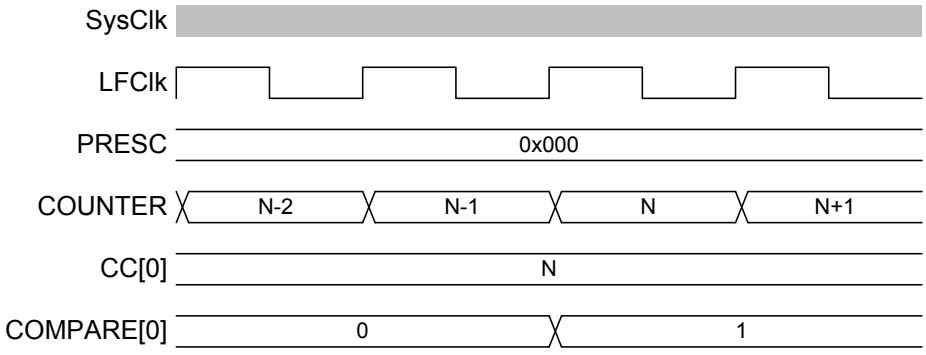



**Figure 58: Timing diagram - COMPARE**

- If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.

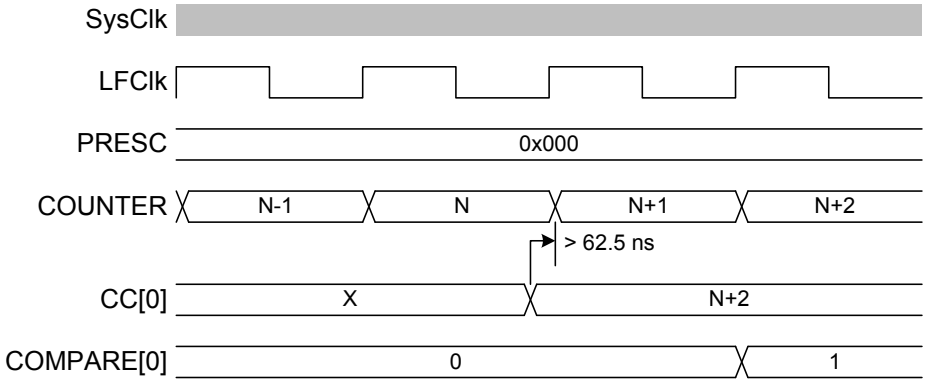



**Figure 59: Timing diagram - COMPARE_N+2**

- If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

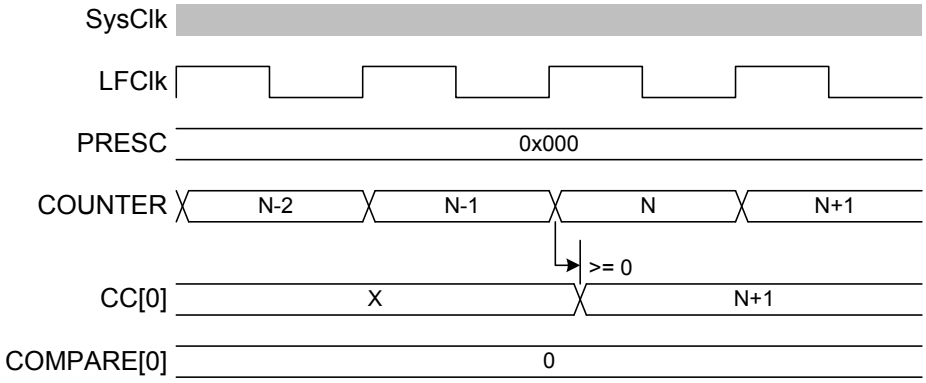



**Figure 60: Timing diagram - COMPARE_N+1**

- If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

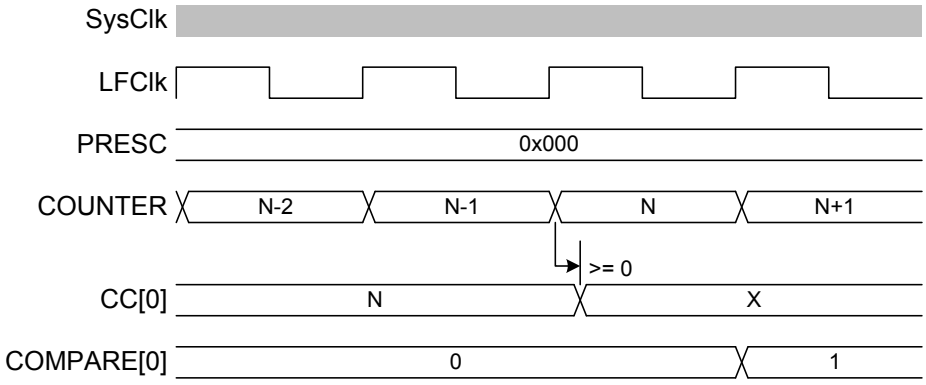



**Figure 61: Timing diagram - COMPARE_N-1**

## 24.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.

**Table 39: RTC jitter magnitudes on tasks**

| Task | Delay |
|---|---|
| CLEAR, STOP, START, TRIGOVRFLOW | +15 to 46 µs |

**Table 40: RTC jitter magnitudes on events**

| Operation/Function | Jitter |
|---|---|
| START to COUNTER increment | +/- 15 µs |
| COMPARE to COMPARE [19] | +/- 62.5 ns |

1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 µs and 45.7755 µs – rounded to 15 µs and 46 µs for the remainder of the section.

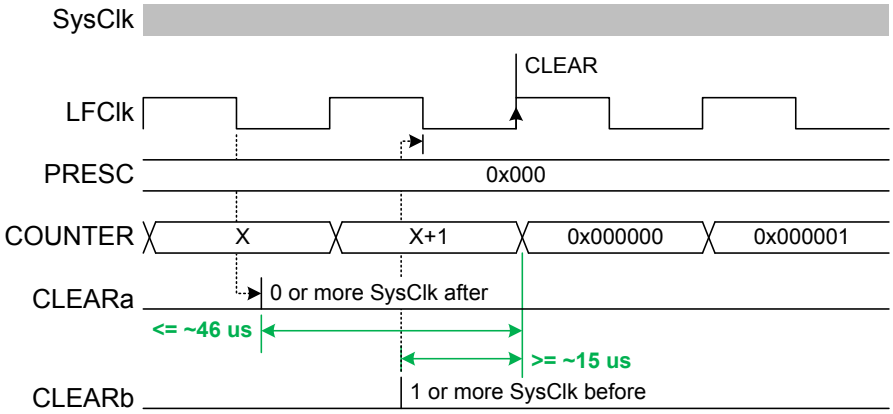



**Figure 62: Timing diagram - DELAY_CLEAR**

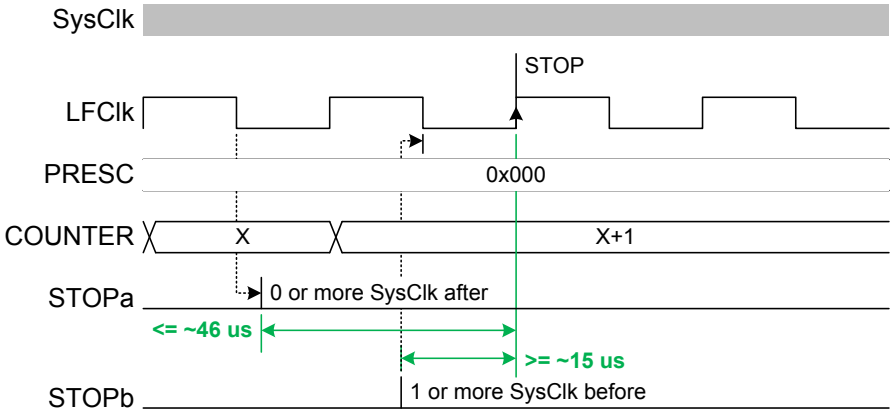



**Figure 63: Timing diagram - DELAY_STOP**

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 µs +/-15 µs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 µs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 µs jitter on the first COUNTER increment.

[19] Assumes RTC runs continuously between these events.

**Note:** 32.768 kHz clock jitter is additional to the numbers provided above.

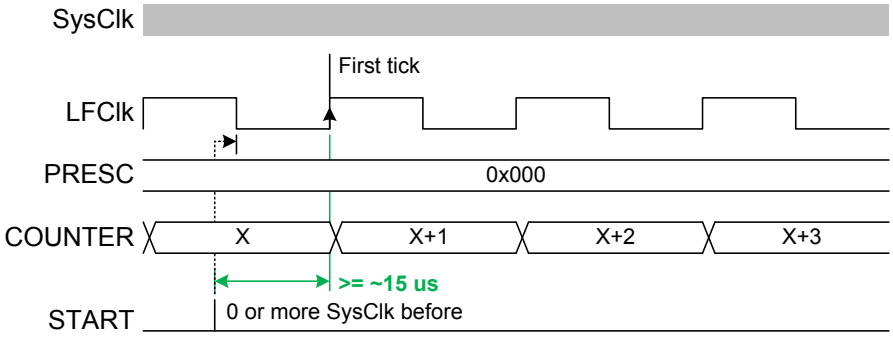



**Figure 64: Timing diagram - JITTER_START-**

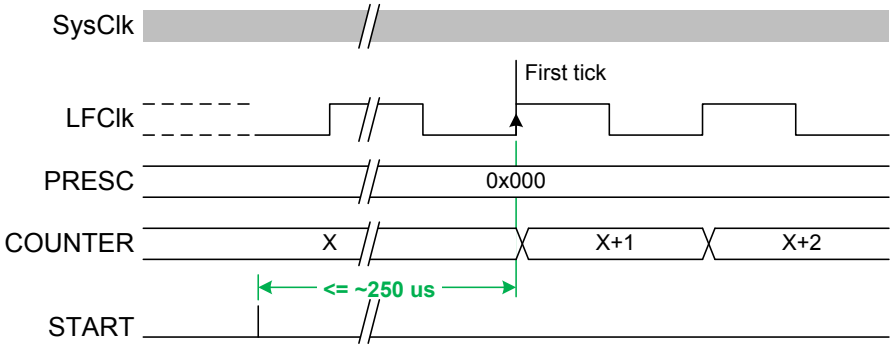



**Figure 65: Timing diagram - JITTER_START+**

## 24.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

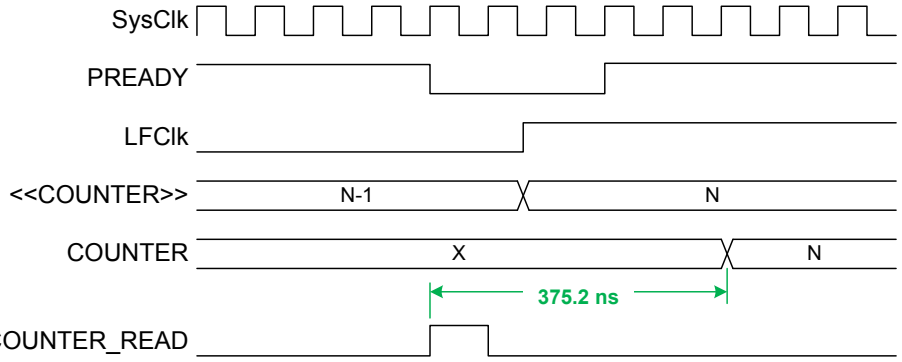



**Figure 66: Timing diagram - COUNTER_READ**

## 24.10 Registers

### Table 41: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000B000 | RTC | RTC0 | Real-time counter 0 | CC[0..2] implemented, CC[3] not implemented |
| 0x40011000 | RTC | RTC1 | Real-time counter 1 | CC[0..3] implemented |

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40024000 | RTC | RTC2 | Real-time counter 2 | CC[0..3] implemented |

### Table 42: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start RTC COUNTER |
| TASKS_STOP | 0x004 | Stop RTC COUNTER |
| TASKS_CLEAR | 0x008 | Clear RTC COUNTER |
| TASKS_TRIGOVRFLW | 0x00C | Set COUNTER to 0xFFFFF0 |
| EVENTS_TICK | 0x100 | Event on COUNTER increment |
| EVENTS_OVRFLW | 0x104 | Event on COUNTER overflow |
| EVENTS_COMPARE[0] | 0x140 | Compare event on CC[0] match |
| EVENTS_COMPARE[1] | 0x144 | Compare event on CC[1] match |
| EVENTS_COMPARE[2] | 0x148 | Compare event on CC[2] match |
| EVENTS_COMPARE[3] | 0x14C | Compare event on CC[3] match |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *EVTEN* | 0x340 | Enable or disable event routing |
| *EVTENSET* | 0x344 | Enable event routing |
| *EVTENCLR* | 0x348 | Disable event routing |
| *COUNTER* | 0x504 | Current COUNTER value |
| *PRESCALER* | 0x508 | 12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)).Must be written when RTC is stopped |
| *CC[0]* | 0x540 | Compare register 0 |
| *CC[1]* | 0x544 | Compare register 1 |
| *CC[2]* | 0x548 | Compare register 2 |
| *CC[3]* | 0x54C | Compare register 3 |

## 24.10.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | | | | | | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TICK | | | Write '1' to Enable interrupt for TICK event<br>See *EVENTS_TICK* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | OVRFLW | | | Write '1' to Enable interrupt for OVRFLW event<br>See *EVENTS_OVRFLW* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | COMPARE0 | | | Write '1' to Enable interrupt for COMPARE[0] event<br>See *EVENTS_COMPARE[0]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | COMPARE1 | | | Write '1' to Enable interrupt for COMPARE[1] event<br>See *EVENTS_COMPARE[1]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | COMPARE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TICK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | OVRFLW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | COMPARE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | COMPARE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | COMPARE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TICK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | OVRFLW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | COMPARE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | COMPARE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | COMPARE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.4 EVTENSET

Address offset: 0x344

Enable event routing

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TICK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | OVRFLW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | COMPARE0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | COMPARE1 | | | Write '1' to Enable event routing for COMPARE[1] event<br><br>See *EVENTS_COMPARE[1]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | COMPARE2 | | | Write '1' to Enable event routing for COMPARE[2] event<br><br>See *EVENTS_COMPARE[2]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | COMPARE3 | | | Write '1' to Enable event routing for COMPARE[3] event<br><br>See *EVENTS_COMPARE[3]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 24.10.5 EVTENCLR

Address offset: 0x348

Disable event routing

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | TICK | | | Write '1' to Disable event routing for TICK event<br><br>See *EVENTS_TICK* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | OVRFLW | | | Write '1' to Disable event routing for OVRFLW event<br><br>See *EVENTS_OVRFLW* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | COMPARE0 | | | Write '1' to Disable event routing for COMPARE[0] event<br><br>See *EVENTS_COMPARE[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | COMPARE1 | | | Write '1' to Disable event routing for COMPARE[1] event<br><br>See *EVENTS_COMPARE[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | COMPARE2 | | | Write '1' to Disable event routing for COMPARE[2] event<br><br>See *EVENTS_COMPARE[2]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | F | E | D | C | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | COMPARE3 | | | | | | | | | | Write '1' to Disable event routing for COMPARE[3] event<br><br>See *EVENTS_COMPARE[3]* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | COUNTER | | | | | | | | | | Counter value | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)).Must be written when RTC is stopped

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PRESCALER | | | | | | | | | | Prescaler value | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.8 CC[0]

Address offset: 0x540

Compare register 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | COMPARE | | | | | | | | | | Compare value | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.9 CC[1]

Address offset: 0x544

Compare register 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | COMPARE | | | | | | | | | | Compare value | | | | | | | | | | | | | | | | | | | | | | | |

## 24.10.10 CC[2]

Address offset: 0x548

Compare register 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | COMPARE | | | Compare value |

### 24.10.11 CC[3]

Address offset: 0x54C

Compare register 3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | COMPARE | | | Compare value |

## 24.11 Electrical specification

### 24.11.1 RTC Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{RTC}$ | Run current Real Time Counter (LFCLK source) | | 0.1 | | µA |

# 25 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

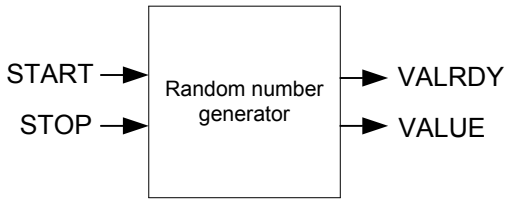



**Figure 67: Random number generator**

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

## 25.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

## 25.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

## 25.3 Registers

**Table 43: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000D000 | RNG | RNG | Random number generator | |

**Table 44: Register Overview**

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Task starting the random number generator |
| TASKS_STOP | 0x004 | Task stopping the random number generator |
| EVENTS_VALRDY | 0x100 | Event being generated for every new random number written to the VALUE register |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *CONFIG* | 0x504 | Configuration register |
| *VALUE* | 0x508 | Output random number |

### 25.3.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | VALRDY_STOP | | | Shortcut between VALRDY event and STOP task |
| | | | | | See *EVENTS_VALRDY* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 25.3.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | VALRDY | | | Write '1' to Enable interrupt for VALRDY event |
| | | | | | See *EVENTS_VALRDY* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 25.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | VALRDY | | | Write '1' to Disable interrupt for VALRDY event |
| | | | | | See *EVENTS_VALRDY* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 25.3.4 CONFIG

Address offset: 0x504

Configuration register

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DERCEN | | | Bias correction |
| | | | Disabled | 0 | Disabled |
| | | | Enabled | 1 | Enabled |

## 25.3.5 VALUE

Address offset: 0x508

Output random number

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | VALUE | | [0..255] | Generated random number |

# 25.4 Electrical specification

## 25.4.1 RNG Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{RNG}$ | Run current, CPU sleeping. | | 500 | | µA |
| $t_{RNG,START}$ | Time from setting the START task to generation begins. This is a one-time delay on START signal and does not apply between samples. | | 128 | | µs |
| $t_{RNG,RAW}$ | Run time per byte without bias correction. Uniform distribution of 0 and 1 is not guaranteed. | | 30 | | µs |
| $t_{RNG,BC}$ | Run time per byte with bias correction. Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed. | | 120 | | µs |

# 26 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK — Clock control* on page 141 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

## 26.1 Registers

### Table 45: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000C000 | TEMP | TEMP | Temperature sensor | |

### Table 46: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start temperature measurement |
| TASKS_STOP | 0x004 | Stop temperature measurement |
| EVENTS_DATARDY | 0x100 | Temperature measurement complete, data ready |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *TEMP* | 0x508 | Temperature in °C (0.25° steps) |
| *A0* | 0x520 | Slope of 1st piece wise linear function |
| *A1* | 0x524 | Slope of 2nd piece wise linear function |
| *A2* | 0x528 | Slope of 3rd piece wise linear function |
| *A3* | 0x52C | Slope of 4th piece wise linear function |
| *A4* | 0x530 | Slope of 5th piece wise linear function |
| *A5* | 0x534 | Slope of 6th piece wise linear function |
| *B0* | 0x540 | y-intercept of 1st piece wise linear function |
| *B1* | 0x544 | y-intercept of 2nd piece wise linear function |
| *B2* | 0x548 | y-intercept of 3rd piece wise linear function |
| *B3* | 0x54C | y-intercept of 4th piece wise linear function |
| *B4* | 0x550 | y-intercept of 5th piece wise linear function |
| *B5* | 0x554 | y-intercept of 6th piece wise linear function |
| *T0* | 0x560 | End point of 1st piece wise linear function |
| *T1* | 0x564 | End point of 2nd piece wise linear function |
| *T2* | 0x568 | End point of 3rd piece wise linear function |
| *T3* | 0x56C | End point of 4th piece wise linear function |
| *T4* | 0x570 | End point of 5th piece wise linear function |

### 26.1.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DATARDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for DATARDY event<br><br>See *EVENTS_DATARDY* |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |

### 26.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DATARDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for DATARDY event<br><br>See *EVENTS_DATARDY* |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |

### 26.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | R | TEMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Temperature in °C (0.25° steps)<br><br>Result of temperature measurement. Die temperature in °C, 2's complement format, 0.25 °C steps<br><br>Decision point: DATARDY |

### 26.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000326** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | A0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Slope of 1st piece wise linear function |

### 26.1.5 A1

Address offset: 0x524

Slope of 2nd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000348** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | A1 | | | Slope of 2nd piece wise linear function |

## 26.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x000003AA** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | A2 | | | Slope of 3rd piece wise linear function |

## 26.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x0000040E** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | A3 | | | Slope of 4th piece wise linear function |

## 26.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x000004BD** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **1** | **1** | **0** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | A4 | | | Slope of 5th piece wise linear function |

## 26.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x000005A3** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | A5 | | | Slope of 6th piece wise linear function |

## 26.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00003FEF** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B0 | | | y-intercept of 1st piece wise linear function |

## 26.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00003FBE** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B1 | | | y-intercept of 2nd piece wise linear function |

## 26.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00003FBE** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B2 | | | y-intercept of 3rd piece wise linear function |

## 26.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000012** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B3 | | | y-intercept of 4th piece wise linear function |

## 26.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000124** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B4 | | | y-intercept of 5th piece wise linear function |

## 26.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x0000027C** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | B5 | | | y-intercept of 6th piece wise linear function |

### 26.1.16 T0

Address offset: 0x560

End point of 1st piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x000000E2** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | T0 | | | End point of 1st piece wise linear function |

### 26.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | T1 | | | End point of 2nd piece wise linear function |

### 26.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000019** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | T2 | | | End point of 3rd piece wise linear function |

### 26.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x0000003C** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | T3 | | | End point of 4th piece wise linear function |

### 26.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000050** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | T4 | | | End point of 5th piece wise linear function |

## 26.2 Electrical specification

### 26.2.1 Temperature Sensor Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TEMP}$ | Time required for temperature measurement | | 36 | | µs |
| $T_{TEMP,RANGE}$ | Temperature sensor range | -40 | | 85 | °C |
| $T_{TEMP,ACC}$ | Temperature sensor accuracy | -5 | | 5 | °C |
| $T_{TEMP,RES}$ | Temperature sensor resolution | | 0.25 | | °C |
| $T_{TEMP,STB}$ | Sample to sample stability at constant device temperature | -0.25 | | 0.25 | °C |
| $T_{TEMP,OFFST}$ | Sample offset at 25°C | -2.5 | | 2.5 | °C |

# 27 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

## 27.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

## 27.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

## 27.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

**Table 47: ECB data structure overview**

| Property | Address offset | Description |
|---|---|---|
| KEY | 0 | 16 byte AES key |
| CLEARTEXT | 16 | 16 byte AES cleartext input block |
| CIPHERTEXT | 32 | 16 byte AES ciphertext output block |

## 27.4 Registers

### Table 48: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000E000 | ECB | ECB | AES electronic code book (ECB) mode block encryption | |

### Table 49: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTECB | 0x000 | Start ECB block encrypt |
| TASKS_STOPECB | 0x004 | Abort a possible executing ECB operation |
| EVENTS_ENDECB | 0x100 | ECB block encrypt complete |
| EVENTS_ERRORECB | 0x104 | ECB block encrypt aborted because of a STOPECB task or due to an error |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ECBDATAPTR* | 0x504 | ECB block encrypt memory pointers |

### 27.4.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENDECB | | | Write '1' to Enable interrupt for ENDECB event<br>See *EVENTS_ENDECB* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | ERRORECB | | | Write '1' to Enable interrupt for ERRORECB event<br>See *EVENTS_ERRORECB* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 27.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENDECB | | | Write '1' to Disable interrupt for ENDECB event<br>See *EVENTS_ENDECB* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | ERRORECB | | | Write '1' to Disable interrupt for ERRORECB event<br>See *EVENTS_ERRORECB* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 27.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ECBDATAPTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pointer to the ECB data structure (see Table 1 ECB data structure overview) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 27.5 Electrical specification

### 27.5.1 ECB Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{ECB}$ | Run time per 16 byte block in all modes | | | 7.2 | µs |

# 28 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in *Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification.[20]

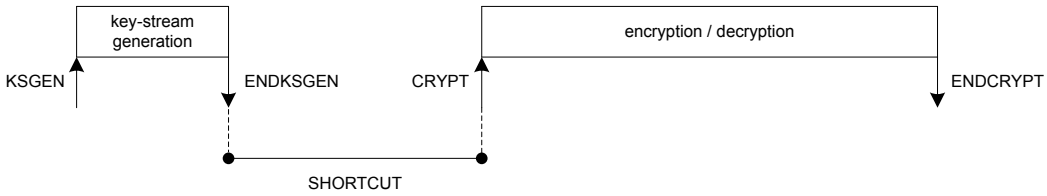



**Figure 68: Key-stream generation followed by encryption or decryption. The shortcut is optional.**

## 28.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

## 28.2 Key-steam generation

A new key-stream needs to be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task and an ENDKSGEN event will be generated when the key-stream has been generated.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by *CNFPTR* on page 333. It is necessary to configure this pointer and its underlying data structure, and the *MODE* on page 332 register before the KSGEN task is triggered.

[20] *Bluetooth* AES CCM 128 bit block encryption, see *Bluetooth* Core specification Version 4.0.

The key-stream will be stored in the AES CCM's temporary memory area, specified by the *SCRATCHPTR* on page 333, where it will be used in subsequent encryption and decryption operations.

For default length packets, that is when MODE.LENGTH is set to Default, the size of the generated key-stream is 27 bytes. When using extended length packets, that is when MODE.LENGTH is set to Extended, The *MAXPACKETSIZE* on page 333 register specifies the length of the key-stream to be generated. The length of the generated key-stream must be greater or equal to the length of the subsequent packet payload to be encrypted or decrypted. The maximum length of the key-stream in extended mode is 251 bytes, which means that the maximum packet payload size is 251.

If a shortcut is used between ENDKSGEN event and CRYPT task, the *INPTR* on page 333 pointer and the *OUTPTR* on page 333 pointers must also be configured before the KSGEN task is triggered.

## 28.3 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

Encryption is started by triggering the CRYPT task with the *MODE* on page 332 register set to ENCRYPTION. An ENDCRYPT event will be generated when packet encryption is completed

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the *OUTPTR* on page 333 pointer, see *Figure 69: Encryption* on page 326.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

The CCM supports different widths of the LENGTH field in the data structure for encrypted packets. This is configured in the *MODE* on page 332 register.

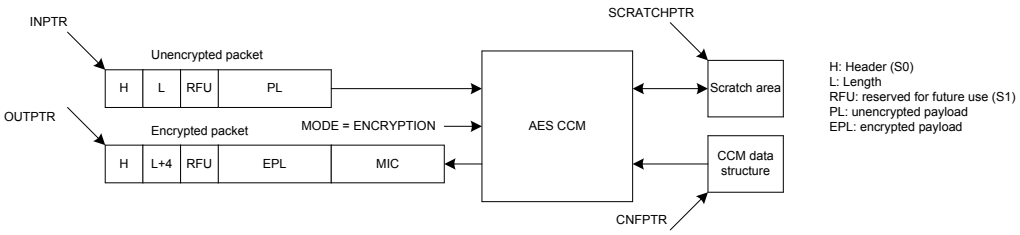



**Figure 69: Encryption**

## 28.4 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

Decryption is started by triggering the CRYPT task with the *MODE* on page 332 register set to DECRYPTION. An ENDCRYPT event will be generated when packet decryption is completed

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 70: Decryption* on page 327.

The CCM is only able to decrypt packet payloads that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.

The CCM supports different widths of the LENGTH field in the data structure for decrypted packets. This is configured in the *MODE* on page 332 register.

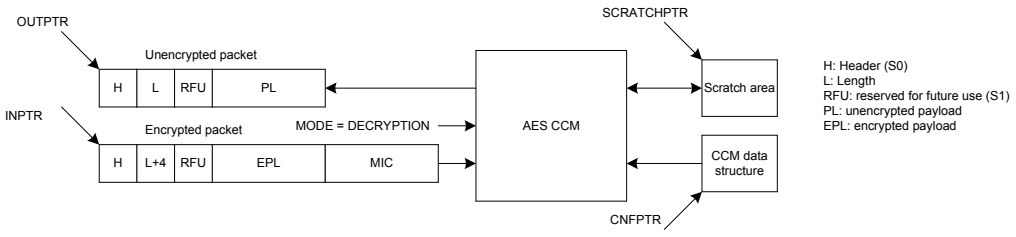



**Figure 70: Decryption**

## 28.5 AES CCM and RADIO concurrent operation

The CCM module is able to encrypt/decrypt data synchronously to data being transmitted or received on the radio.

In order for the CCM module to run synchronously with the radio, the data rate setting in the *MODE* on page 332 register needs to match the radio data rate. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered.

The data rate setting of the *MODE* on page 332 register can also be overridden on-the-fly during an ongoing encrypt/decrypt operation by the contents of the *RATEOVERRIDE* on page 334 register. The data rate setting in this register applies whenever the RATEOVERRIDE task is triggered. This feature can be useful in cases where the radio data rate is changed during an ongoing packet transaction.

## 28.6 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the radio is transmitting it, the radio must read the encrypted packet from the same memory location as the AES CCM is writing to.

The *OUTPTR* on page 333 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the radio, see *Figure 71: Configuration of on-the-fly encryption* on page 327.

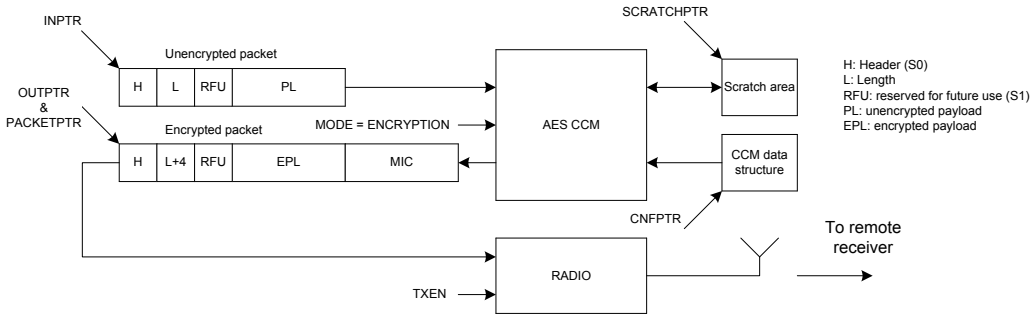



**Figure 71: Configuration of on-the-fly encryption**

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the key-stream generation to complete before the encryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 72: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection* on page 328 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the TXEN task in the RADIO is triggered.

**Important:** Refer to *Timing specification* on page 334 for information about the time needed for generating a key-stream.

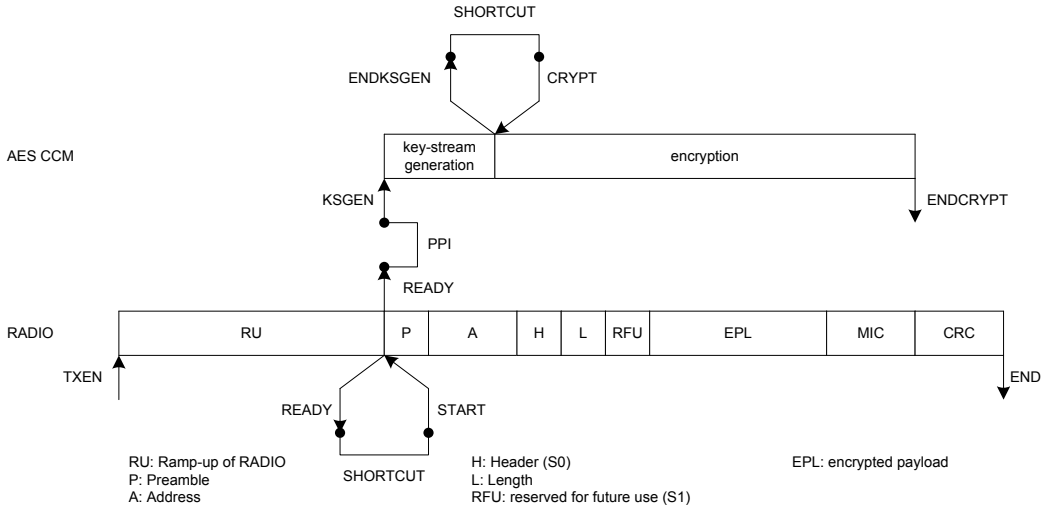



**Figure 72: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection**

## 28.7 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The *INPTR* on page 333 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 73: Configuration of on-the-fly decryption* on page 328.

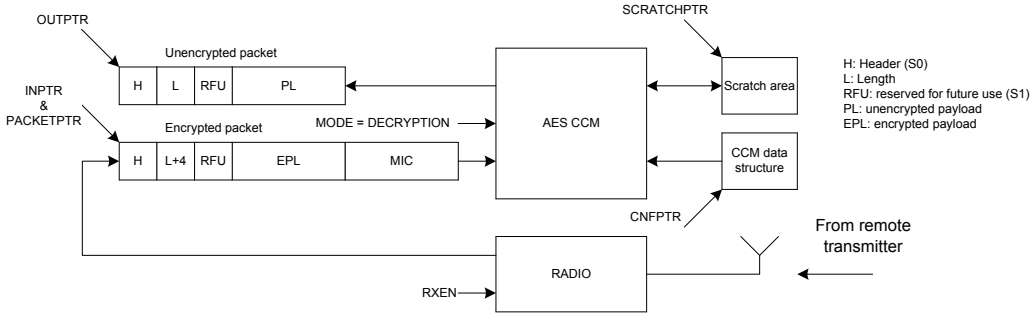



**Figure 73: Configuration of on-the-fly decryption**

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the key-stream generation to complete before the decryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 74: On-the-fly decryption of short packets (MODE.LENGTH = Default) using a PPI connection* on page 329 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the RXEN task in the RADIO is triggered.

**Important:** Refer to *Timing specification* on page 334 for information about the time needed for generating a key-stream.

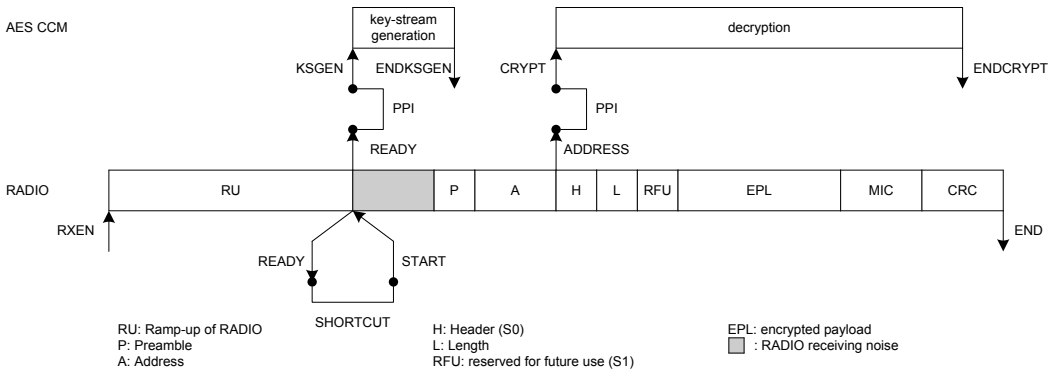



**Figure 74: On-the-fly decryption of short packets (MODE.LENGTH = Default) using a PPI connection**

## 28.8 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

### Table 50: CCM data structure overview

| Property | Address offset | Description |
|---|---|---|
| KEY | 0 | 16 byte AES key |
| PKTCTR | 16 | Octet0 (LSO) of packet counter |
| | 17 | Octet1 of packet counter |
| | 18 | Octet2 of packet counter |
| | 19 | Octet3 of packet counter |
| | 20 | Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant bit) Bit7: Ignored |
| | 21 | Ignored |
| | 22 | Ignored |
| | 23 | Ignored |
| | 24 | Bit 0: Direction bit Bit 7 – Bit 1: Zero padded |
| IV | 25 | 8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV, … , Octet7 (MSO) of IV |

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 50: CCM data structure overview* on page 329 .

### Table 51: Data structure for unencrypted packet

| Property | Address offset | Description |
|---|---|---|
| HEADER | 0 | Packet Header |
| LENGTH | 1 | Number of bytes in unencrypted payload |
| RFU | 2 | Reserved Future Use |
| PAYLOAD | 3 | Unencrypted payload |

### Table 52: Data structure for encrypted packet

| Property | Address offset | Description |
|---|---|---|
| HEADER | 0 | Packet Header |
| LENGTH | 1 | Number of bytes in encrypted payload including length of MIC<br>**Important:** LENGTH will be 0 for empty packets since the MIC is not added to empty packets |
| RFU | 2 | Reserved Future Use |

| Property | Address offset | Description |
|---|---|---|
| PAYLOAD | 3 | Encrypted payload |
| MIC | 3 + payload length | ENCRYPT: 4 bytes encrypted MIC |

**Important:** MIC is not added to empty packets

## 28.9 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In cases where the CPU and other EasyDMA enabled peripherals are accessing the same RAM block at the same time, a high level of bus collisions may cause too slow operation for correct on the fly encryption. In this case the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

## 28.10 Registers

### Table 53: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000F000 | CCM | CCM | AES counter with CBC-MAC (CCM) mode block encryption | |

### Table 54: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| TASKS_KSGEN | 0x000 | Start generation of key-stream. This operation will stop by itself when completed. | |
| TASKS_CRYPT | 0x004 | Start encryption/decryption. This operation will stop by itself when completed. | |
| TASKS_STOP | 0x008 | Stop encryption/decryption | |
| TASKS_RATEOVERRIDE | 0x00C | Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption | |
| EVENTS_ENDKSGEN | 0x100 | Key-stream generation complete | |
| EVENTS_ENDCRYPT | 0x104 | Encrypt/decrypt complete | |
| EVENTS_ERROR | 0x108 | CCM error event | Deprecated |
| *SHORTS* | 0x200 | Shortcut register | |
| *INTENSET* | 0x304 | Enable interrupt | |
| *INTENCLR* | 0x308 | Disable interrupt | |
| *MICSTATUS* | 0x400 | MIC check result | |
| *ENABLE* | 0x500 | Enable | |
| *MODE* | 0x504 | Operation mode | |
| *CNFPTR* | 0x508 | Pointer to data structure holding AES key and NONCE vector | |
| *INPTR* | 0x50C | Input pointer | |
| *OUTPTR* | 0x510 | Output pointer | |
| *SCRATCHPTR* | 0x514 | Pointer to data area used for temporary storage | |
| *MAXPACKETSIZE* | 0x518 | Length of key-stream generated when MODE.LENGTH = Extended. | |
| *RATEOVERRIDE* | 0x51C | Data rate override setting. | |

### 28.10.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ENDKSGEN_CRYPT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Shortcut between ENDKSGEN event and CRYPT task |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDKSGEN* and *TASKS_CRYPT* |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable shortcut |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable shortcut |

## 28.10.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ENDKSGEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for ENDKSGEN event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDKSGEN* |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |
| B | RW | ENDCRYPT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for ENDCRYPT event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDCRYPT* |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |
| C | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for ERROR event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ERROR* |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |

## 28.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ENDKSGEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ENDKSGEN event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDKSGEN* |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |
| B | RW | ENDCRYPT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ENDCRYPT event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDCRYPT* |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled |
| C | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ERROR event |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ERROR* |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | Enabled | 1 | Read: Enabled |

## 28.10.4 MICSTATUS

Address offset: 0x400

MIC check result

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | MICSTATUS | | | The result of the MIC check performed during the previous decryption operation |
| | | | CheckFailed | 0 | MIC check failed |
| | | | CheckPassed | 1 | MIC check passed |

## 28.10.5 ENABLE

Address offset: 0x500

Enable

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENABLE | | | Enable or disable CCM |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 2 | Enable |

## 28.10.6 MODE

Address offset: 0x504

Operation mode

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B B A |
| **Reset 0x00000001** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | MODE | | | The mode of operation to be used. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered. |
| | | | Encryption | 0 | AES CCM packet encryption mode |
| | | | Decryption | 1 | AES CCM packet decryption mode |
| B | RW | DATARATE | | | Radio data rate that the CCM shall run synchronous with |
| | | | 1Mbit | 0 | 1 Mbps |
| | | | 2Mbit | 1 | 2 Mbps |
| | | | 125Kbps | 2 | 125 Kbps |
| | | | 500Kbps | 3 | 500 Kbps |
| C | RW | LENGTH | | | Packet length configuration |
| | | | Default | 0 | Default length. Effective length of LENGTH field in encrypted/ decrypted packet is 5 bits. A key-stream for packet payloads up to 27 bytes will be generated. |
| | | | Extended | 1 | Extended length. Effective length of LENGTH field in encrypted/ decrypted packet is 8 bits. A key-stream for packet payloads up to MAXPACKETSIZE bytes will be generated. |

## 28.10.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CNFPTR | | | Pointer to the data structure holding the AES key and the CCM NONCE vector (see Table 1 CCM data structure overview) |

## 28.10.8 INPTR

Address offset: 0x50C

Input pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | INPTR | | | Input pointer |

## 28.10.9 OUTPTR

Address offset: 0x510

Output pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | OUTPTR | | | Output pointer |

## 28.10.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SCRATCHPTR | | | Pointer to a scratch data area used for temporary storage during key-stream generation, MIC generation and encryption/ decryption.<br><br>The scratch area is used for temporary storage of data during key-stream generation and encryption.<br><br>When MODE.LENGTH = Default, a space of 43 bytes is required for this temporary storage. MODE.LENGTH = Extended (16 + MAXPACKETSIZE) bytes of storage is required. |

## 28.10.11 MAXPACKETSIZE

Address offset: 0x518

Length of key-stream generated when MODE.LENGTH = Extended.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x000000FB** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | MAXPACKETSIZE | | [0x001B..0x00FB] | | | | | | | | | | | | | | | | | | | | | | | | Length of key-stream generated when MODE.LENGTH = Extended. This value must be greater or equal to the subsequent packet payload to be encrypted/decrypted. | | | | | | | |

### 28.10.12 RATEOVERRIDE

Address offset: 0x51C

Data rate override setting.

Override value to be used instead of the setting of MODE.DATARATE. This override value applies when the RATEOVERRIDE task is triggered.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | RATEOVERRIDE | | | | | | | | | | | | | | | | | | | | | | | | | | Data rate override setting. | | | | | | | |
| | | | 1Mbit | 0 | | | | | | | | | | | | | | | | | | | | | | | | 1 Mbps | | | | | | | |
| | | | 2Mbit | 1 | | | | | | | | | | | | | | | | | | | | | | | | 2 Mbps | | | | | | | |
| | | | 125Kbps | 2 | | | | | | | | | | | | | | | | | | | | | | | | 125 Kbps | | | | | | | |
| | | | 500Kbps | 3 | | | | | | | | | | | | | | | | | | | | | | | | 500 Kbps | | | | | | | |

## 28.11 Electrical specification

### 28.11.1 Timing specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{kgen}$ | Time needed for key-stream generation (given priority access to destination RAM block). | | | 50 | µs |

# 29 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

## 29.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

## 29.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

## 29.3 Resolving a resolvable address

As per *Bluetooth* specification, a private resolvable address is composed of six bytes.

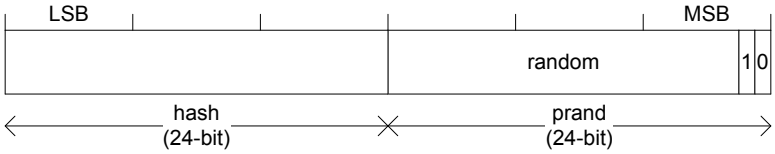



**Figure 75: Resolvable address**

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification[21]. The time it takes to resolve an address may vary depending on where in the list the

[21] *Bluetooth* Specification Version 4.0 [Vol 3] chapter 10.8.2.3.

resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

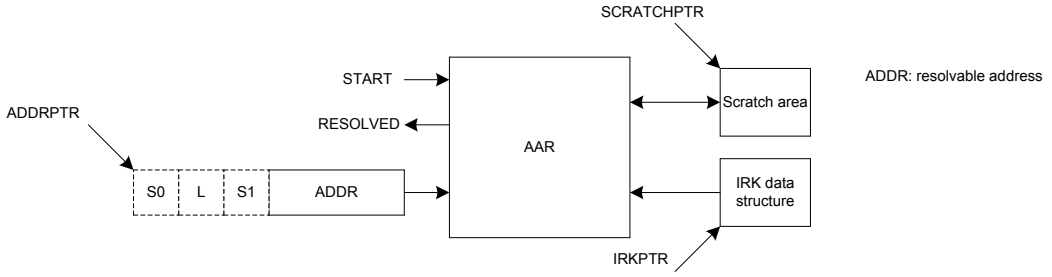



**Figure 76: Address resolution with packet preloaded into RAM**

## 29.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

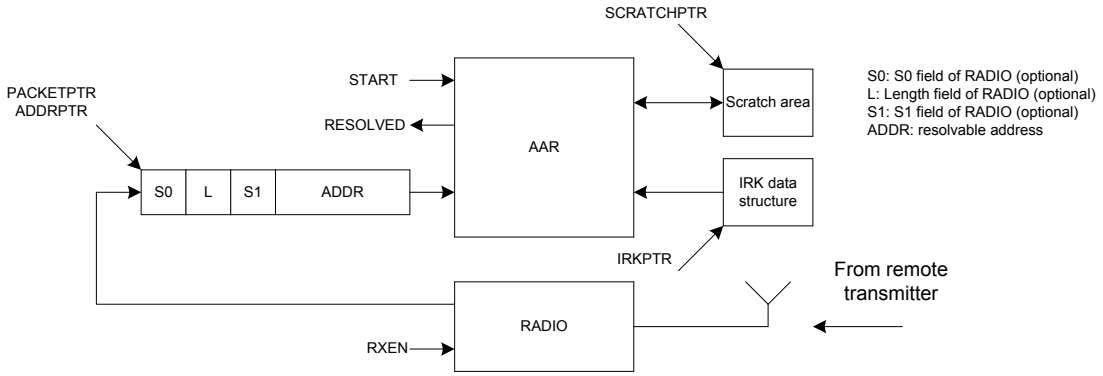



**Figure 77: Address resolution with packet loaded into RAM by the RADIO**

## 29.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

**Table 55: IRK data structure overview**

| Property | Address offset | Description |
|---|---|---|
| IRK0 | 0 | IRK number 0 (16 - byte) |
| IRK1 | 16 | IRK number 1 (16 - byte) |
| .. | .. | .. |
| IRK15 | 240 | IRK number 15 (16 - byte) |

# 29.6 Registers

### Table 56: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4000F000 | AAR | AAR | Accelerated address resolver | |

### Table 57: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start resolving addresses based on IRKs specified in the IRK data structure |
| TASKS_STOP | 0x008 | Stop resolving addresses |
| EVENTS_END | 0x100 | Address resolution procedure complete |
| EVENTS_RESOLVED | 0x104 | Address resolved |
| EVENTS_NOTRESOLVED | 0x108 | Address not resolved |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *STATUS* | 0x400 | Resolution status |
| *ENABLE* | 0x500 | Enable AAR |
| *NIRK* | 0x504 | Number of IRKs |
| *IRKPTR* | 0x508 | Pointer to IRK data structure |
| *ADDRPTR* | 0x510 | Pointer to the resolvable address |
| *SCRATCHPTR* | 0x514 | Pointer to data area used for temporary storage |

## 29.6.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | END | | | Write '1' to Enable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | RESOLVED | | | Write '1' to Enable interrupt for RESOLVED event |
| | | | | | See *EVENTS_RESOLVED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | NOTRESOLVED | | | Write '1' to Enable interrupt for NOTRESOLVED event |
| | | | | | See *EVENTS_NOTRESOLVED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 29.6.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | END | | | Write '1' to Disable interrupt for END event<br><br>See *EVENTS_END* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | RESOLVED | | | Write '1' to Disable interrupt for RESOLVED event<br><br>See *EVENTS_RESOLVED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | NOTRESOLVED | | | Write '1' to Disable interrupt for NOTRESOLVED event<br><br>See *EVENTS_NOTRESOLVED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 29.6.3 STATUS

Address offset: 0x400

Resolution status

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | STATUS | | [0..15] | The IRK that was used last time an address was resolved |

## 29.6.4 ENABLE

Address offset: 0x500

Enable AAR

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENABLE | | | Enable or disable AAR |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 3 | Enable |

## 29.6.5 NIRK

Address offset: 0x504

Number of IRKs

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A |
| **Reset 0x00000001** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | NIRK | | [1..16] | Number of Identity root keys available in the IRK data structure |

## 29.6.6 IRKPTR

Address offset: 0x508

Pointer to IRK data structure

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | IRKPTR | | | | | | | | | | | | | | | | | | | | | | | | Pointer to the IRK data structure | | | | | | | | | |

## 29.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | ADDRPTR | | | | | | | | | | | | | | | | | | | | | | | | Pointer to the resolvable address (6-bytes) | | | | | | | | | |

## 29.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | SCRATCHPTR | | | | | | | | | | | | | | | | | | | | | | | | Pointer to a scratch data area used for temporary storage during resolution.A space of minimum 3 bytes must be reserved. | | | | | | | | | |

# 29.7 Electrical specification

## 29.7.1 AAR Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{AAR}$ | Address resolution time per IRK. Total time for several IRKs is given as (1 µs + n * t_AAR), where n is the number of IRKs. (Given priority to the actual destination RAM block). | | | 6 | µs |
| $t_{AAR,8}$ | Time for address resolution of 8 IRKs. (Given priority to the actual destination RAM block). | | | 49 | µs |

# 30 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple SPI slaves using individual chip select signals for each slave.

Listed here are the main features for the SPIM

- EasyDMA direct transfer to/from RAM
- SPI mode 0-3
- Individual selection of IO pin for each SPI signal
- Optional D/CX output line for distinguishing between command and data bytes

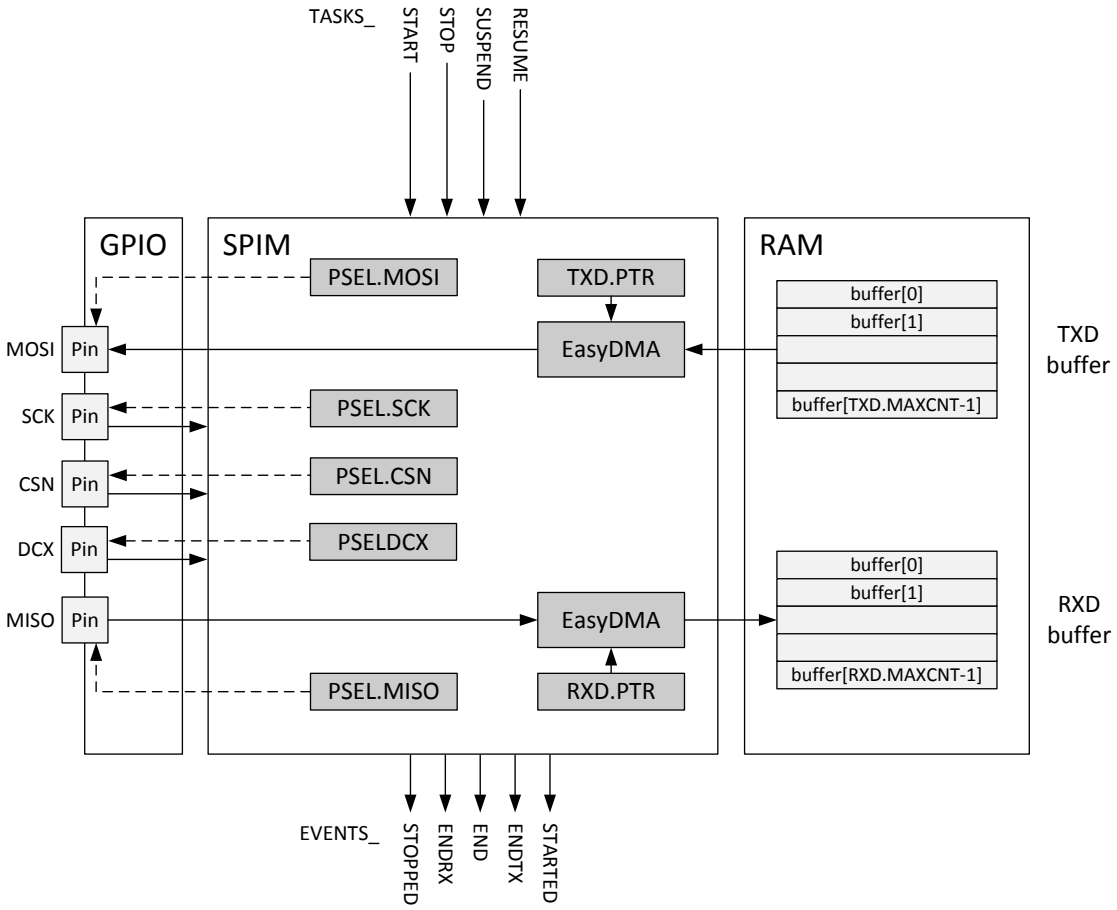



**Figure 78: SPIM — SPI master with EasyDMA**

## 30.1 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of bytes being transmitted/received on MOSI/MISO.

An SPI master transaction is started by triggering the START task. When started, a number of bytes will be transmitted/received on MOSI/MISO. This is illustrated in *Figure 79: SPI master transaction* on page 341.

The ENDTX is generated when all bytes in the *TXD.PTR* on page 349 buffer as specified in the *TXD.MAXCNT* on page 349 register have been transmitted. The ENDRX event will be generated when

the *RXD.PTR* on page 349 buffer is full, that is after the number of bytes specified in the *RXD.MAXCNT* on page 349 register have been received. The transaction stops automatically after MAX( *TXD.MAXCNT* on page 349, *RXD.MAXCNT* on page 349) number of bytes have been transmitted/received. In the case when *RXD.MAXCNT* on page 349 > *TXD.MAXCNT* on page 349 the contents of the *ORC* on page 352 register will be transmitted after the last byte in the *TXD.PTR* on page 349 buffer has been transmitted.

The END event will be generated after both the ENDRX and ENDTX events have been generated.

The SPI master can be stopped in the middle of a transaction by triggering the STOP task. When triggering the STOP task the SPIM will wait for the transmission/reception of the current byte to complete before stopping. A STOPPED event is generated when the SPI master has stopped.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the ENDTX event will be generated even though all bytes in the *TXD.PTR* on page 349 buffer have not been transmitted.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the ENDRX event will be generated even though the *RXD.PTR* on page 349 buffer is not full.

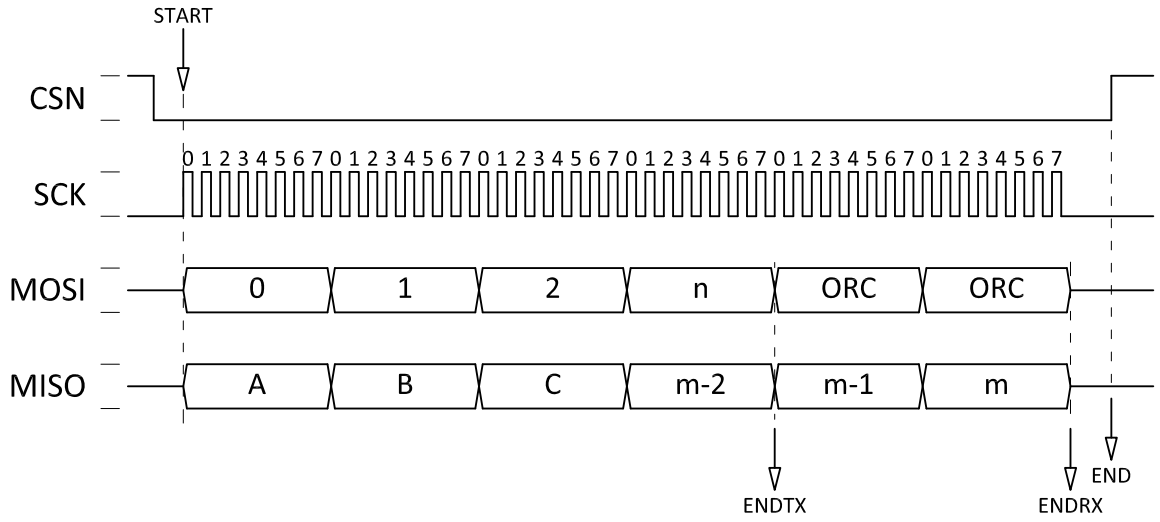



**Figure 79: SPI master transaction**

## 30.2 D/CX functionality

Some SPI slaves, as for example display drivers, require an additional signal from the SPI master to distinguish between command and data bytes. For displays drivers this line is often called D/CX.

The SPIM provides support for such a D/CX output line. The D/CX line is set low during transmission of command bytes and high during transmission of data bytes.

The D/CX pin number is selected using *PSELDCX* on page 351 and the number of command bytes preceding the data bytes is configured using *DCXCNT* on page 351.

It is not allowed to write to the *DCXCNT* on page 351 during an ongoing transmission.

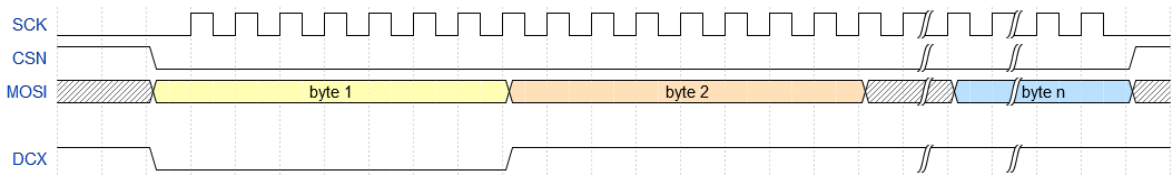



**Figure 80: D/CX example. SPIM.DCXCNT = 1.**

## 30.3 Pin configuration

The SCK, CSN, DCX, MOSI, and MISO signals associated with the SPIM are mapped to physical pins according to the configuration specified in the PSEL.n registers.

The contents of *PSEL.SCK* on page 347, *PSEL.CSN* on page 348, *PSELDCX* on page 351, *PSEL.MOSI* on page 347 and *PSEL.MISO* on page 348 registers are only used when the SPIM is enabled and retained only as long as the device is in System On mode. The PSEL.n registers can only be configured when the SPIM is disabled. Enabling/disabling is done using the *ENABLE* on page 347 register.

To ensure correct behavior the pins used by the SPIM must be configured in the GPIO peripheral as described in *Table 58: GPIO configuration* on page 342 before the SPIM is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

**Table 58: GPIO configuration**

| SPI master signal | SPI master pin | Direction | Output value | Comments |
|---|---|---|---|---|
| SCK | As specified in *PSEL.SCK* on page 347 | Output | Same as CONFIG.CPOL | |
| CSN | As specified in *PSEL.CSN* on page 348 | Output | Same as CONFIG.CPOL | |
| DCX | As specified in *PSELDCX* on page 351 | Output | 1 | |
| MOSI | As specified in *PSEL.MOSI* on page 347 | Output | 0 | |
| MISO | As specified in *PSEL.MISO* on page 348 | Input | Not applicable | |

Some SPIM instances do not have support for controlling CSN automatically. In these cases available GPIO pins needs to be used to control CSN directly. Refer to *Table 60: Instances* on page 344 for information about what features are supported in the various SPIM instances.

The SPIM supports SPI modes 0 through 3. The *CONFIG* on page 350 register allows setting CPOL and CPHA appropriately.

**Table 59: SPI modes**

| Mode | Clock polarity CPOL | Clock phase CPHA |
|---|---|---|
| SPI_MODE0 | 0 (Active High) | 0 (Leading) |
| SPI_MODE1 | 0 (Active High) | 1 (Trailing) |
| SPI_MODE2 | 1 (Active Low) | 0 (Leading) |
| SPI_MODE3 | 1 (Active Low) | 1 (Trailing) |

## 30.4 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

## 30.5 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 78: SPIM — SPI master with EasyDMA* on page 340. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

In the case where several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. The SPIM is such an AHB master, and when congestion occurs the SPIM might have to wait for access to RAM to be granted. If the SPIM has to wait for bus access the transaction will be temporary stalled, but resume once the SPIM is granted access to the bus. See the *AHB multilayer* on page 25 for more information on this subject. Note that some SPIM instances do not support this stalling mechanism. Refer to *Table 60: Instances* on page 344 for information about what features are supported in the various instances.

### 30.5.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

- Array list

#### EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE  4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];

//replace 'Channel' below by the specific data channel you want to use,
//         for instance 'NRF_SPIM->RXD', 'NRF_TWIM->RXD', etc.
Channel.MAXCNT = BUFFER_SIZE;
```

```
Channel.PTR = &MyArrayList;
```

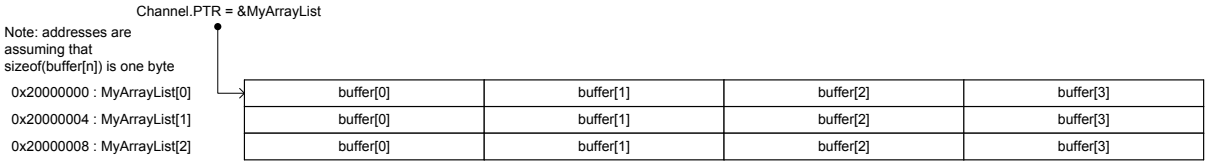



**Figure 81: EasyDMA array list**

## 30.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

## 30.7 Registers

### Table 60: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40003000 | SPIM | SPIM0 | SPI master 0 | Not supported: > 8 Mbps data rate, CSNPOL register, DCX functionality, IFTIMING.x registers, hardware CSN control (PSEL.CSN), stalling mechanism during AHB bus contention. Limitations: TXD.MAXCNT/ RXD.MAXCNT only 8 bits wide. |
| 0x40004000 | SPIM | SPIM1 | SPI master 1 | Not supported: > 8 Mbps data rate, CSNPOL register, DCX functionality, IFTIMING.x registers, hardware CSN control (PSEL.CSN), stalling mechanism during AHB bus contention. Limitations: TXD.MAXCNT/ RXD.MAXCNT only 8 bits wide. |
| 0x40023000 | SPIM | SPIM2 | SPI master 2 | Not supported: > 8 Mbps data rate, CSNPOL register, DCX functionality, IFTIMING.x registers, hardware CSN control (PSEL.CSN), stalling mechanism during AHB bus contention. Limitations: TXD.MAXCNT/ RXD.MAXCNT only 8 bits wide. |
| 0x4002F000 | SPIM | SPIM3 | SPI master 3 | |

### Table 61: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x010 | Start SPI transaction |
| TASKS_STOP | 0x014 | Stop SPI transaction |
| TASKS_SUSPEND | 0x01C | Suspend SPI transaction |
| TASKS_RESUME | 0x020 | Resume SPI transaction |
| EVENTS_STOPPED | 0x104 | SPI transaction has stopped |
| EVENTS_ENDRX | 0x110 | End of RXD buffer reached |
| EVENTS_END | 0x118 | End of RXD buffer and TXD buffer reached |
| EVENTS_ENDTX | 0x120 | End of TXD buffer reached |
| EVENTS_STARTED | 0x14C | Transaction started |
| *SHORTS* | 0x200 | Shortcut register |

| Register | Offset | Description |
|---|---|---|
| INTENSET | 0x304 | Enable interrupt |
| INTENCLR | 0x308 | Disable interrupt |
| STALLSTAT | 0x400 | Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware whenever a stall occurres and can be cleared (set to NOSTALL) by the CPU. |
| ENABLE | 0x500 | Enable SPIM |
| PSEL.SCK | 0x508 | Pin select for SCK |
| PSEL.MOSI | 0x50C | Pin select for MOSI signal |
| PSEL.MISO | 0x510 | Pin select for MISO signal |
| PSEL.CSN | 0x514 | Pin select for CSN |
| FREQUENCY | 0x524 | SPI frequency. Accuracy depends on the HFCLK source selected. |
| RXD.PTR | 0x534 | Data pointer |
| RXD.MAXCNT | 0x538 | Maximum number of bytes in receive buffer |
| RXD.AMOUNT | 0x53C | Number of bytes transferred in the last transaction |
| RXD.LIST | 0x540 | EasyDMA list type |
| TXD.PTR | 0x544 | Data pointer |
| TXD.MAXCNT | 0x548 | Number of bytes in transmit buffer |
| TXD.AMOUNT | 0x54C | Number of bytes transferred in the last transaction |
| TXD.LIST | 0x550 | EasyDMA list type |
| CONFIG | 0x554 | Configuration register |
| IFTIMING.RXDELAY | 0x560 | Sample delay for input serial data on MISO |
| IFTIMING.CSNDUR | 0x564 | Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay high between transactions |
| CSNPOL | 0x568 | Polarity of CSN output |
| PSELDCX | 0x56C | Pin select for DCX signal |
| DCXCNT | 0x570 | DCX configuration |
| ORC | 0x5C0 | Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT |

## 30.7.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | A | | | | | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | END_START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | E | | | | | | | | | | D | | C | | B | | | A | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | E | | | | | | | | | | | D | | C | | B | | | A | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_ENDRX* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | END | | | Write '1' to Enable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | ENDTX | | | Write '1' to Enable interrupt for ENDTX event |
| | | | | | See *EVENTS_ENDTX* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | STARTED | | | Write '1' to Enable interrupt for STARTED event |
| | | | | | See *EVENTS_STARTED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 30.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | E | | | | | | | | | | | D | | C | | B | | | A | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | STOPPED | | | Write '1' to Disable interrupt for STOPPED event |
| | | | | | See *EVENTS_STOPPED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | ENDRX | | | Write '1' to Disable interrupt for ENDRX event |
| | | | | | See *EVENTS_ENDRX* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | END | | | Write '1' to Disable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | ENDTX | | | Write '1' to Disable interrupt for ENDTX event |
| | | | | | See *EVENTS_ENDTX* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | STARTED | | | Write '1' to Disable interrupt for STARTED event |
| | | | | | See *EVENTS_STARTED* |
| | | | Clear | 1 | Disable |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | E | | | | | | | | | | | D | | C | | B | | | A | |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.4 STALLSTAT

Address offset: 0x400

Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware whenever a stall occurres and can be cleared (set to NOSTALL) by the CPU.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TX | | [1..0] | Stall status for EasyDMA RAM reads | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NOSTALL | 0 | No stall | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | STALL | 1 | A stall has occurred | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RX | | [1..0] | Stall status for EasyDMA RAM writes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NOSTALL | 0 | No stall | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | STALL | 1 | A stall has occurred | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.5 ENABLE

Address offset: 0x500

Enable SPIM

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | Enable or disable SPIM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Disable SPIM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 7 | Enable SPIM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.6 PSEL.SCK

Address offset: 0x508

Pin select for SCK

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | Pin number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | Connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | Connect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.7 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.8 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.9 PSEL.CSN

Address offset: 0x514

Pin select for CSN

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.10 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x04000000** | | | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FREQUENCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K125 | 0x02000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K250 | 0x04000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K500 | 0x08000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M1 | 0x10000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M2 | 0x20000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M4 | 0x40000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M8 | 0x80000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M16 | 0x0A000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M32 | 0x14000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 30.7.11 RXD.PTR

Address offset: 0x534

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer |

### 30.7.12 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in receive buffer |

### 30.7.13 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

### 30.7.14 RXD.LIST

Address offset: 0x540

EasyDMA list type

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | LIST | | | List type |
| | | | Disabled | 0 | Disable EasyDMA list |
| | | | ArrayList | 1 | Use array list |

### 30.7.15 TXD.PTR

Address offset: 0x544

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer |

### 30.7.16 TXD.MAXCNT

Address offset: 0x548

Number of bytes in transmit buffer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MAXCNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Maximum number of bytes in transmit buffer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | AMOUNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Number of bytes transferred in the last transaction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.18 TXD.LIST

Address offset: 0x550

EasyDMA list type

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LIST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ArrayList | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Disable EasyDMA list | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Use array list | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.19 CONFIG

Address offset: 0x554

Configuration register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ORDER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | MsbFirst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LsbFirst | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Bit order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Most significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Least significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CPHA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Leading | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Trailing | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) phase | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on leading edge of clock, shift serial data on trailing edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on trailing edge of clock, shift serial data on leading edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CPOL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveHigh | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveLow | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) polarity | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 30.7.20 IFTIMING.RXDELAY

Address offset: 0x560

Sample delay for input serial data on MISO

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | RXDELAY | | [7..0] | Sample delay for input serial data on MISO. The value specifies the number of 64 MHz clock cycles (15.625 ns) delay from the the sampling edge of SCK (leading edge for CONFIG.CPHA = 0, trailing edge for CONFIG.CPHA = 1) until the input serial data is sampled. As en example, if RXDELAY = 0 and CONFIG.CPHA = 0, the input serial data is sampled on the rising edge of SCK. |

## 30.7.21 IFTIMING.CSNDUR

Address offset: 0x564

Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay high between transactions

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | CSNDUR | | [0xFF..0] | Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay high between transactions. The value is specified in number of 64 MHz clock cycles (15.625 ns). |

## 30.7.22 CSNPOL

Address offset: 0x568

Polarity of CSN output

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | CSNPOL | | | Polarity of CSN output |
| | | | LOW | 0 | Active low (idle state high) |
| | | | HIGH | 1 | Active high (idle state low) |

## 30.7.23 PSELDCX

Address offset: 0x56C

Pin select for DCX signal

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 30.7.24 DCXCNT

Address offset: 0x570

DCX configuration

| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|
| Id | A A A A |
| **Reset 0x00000000** | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | DCXCNT | | 0x0..0xF | This register specifies the number of command bytes preceding the data bytes. The PSEL.DCX line will be low during transmission of command bytes and high during transmission of data bytes. Value 0xF indicates that all bytes are command bytes. |

### 30.7.25 ORC

Address offset: 0x5C0

Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT

| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|
| Id | A A A A A A A A |
| **Reset 0x00000000** | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ORC | | | Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT. |

## 30.8 Electrical specification

### 30.8.1 Current consumption

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{SPIM,2Mbps}$ | Run current for SPIM, 2 Mbps | | 50 | | µA |
| $I_{SPIM,8Mbps}$ | Run current for SPIM, 8 Mbps | | 50 | | µA |
| $I_{SPIM,16Mbps}$ | Run current for SPIM, 16 Mbps | .. | .. | .. | µA |
| $I_{SPIM,32Mbps}$ | Run current for SPIM, 32 Mbps | .. | .. | .. | µA |
| $I_{SPIM,IDLE}$ | Idle current for SPIM (STARTed, no CSN activity) | | 1 | | µA |

### 30.8.2 Timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{SPIM}$ | Bit rates for SPIM[22] | | | 8[23] | Mbps |
| $t_{SPIM,START}$ | Time from START task to transmission started | | 1 | | µs |
| $t_{SPIM,CSCK}$ | SCK period | 125 | | | ns |
| $t_{SPIM,RSCK,LD}$ | SCK rise time, standard drive[a] | | | $t_{RF,25pF}$ | |
| $t_{SPIM,RSCK,HD}$ | SCK rise time, high drive[a] | | | $t_{HRF,25pF}$ | |
| $t_{SPIM,FSCK,LD}$ | SCK fall time, standard drive[a] | | | $t_{RF,25pF}$ | |
| $t_{SPIM,FSCK,HD}$ | SCK fall time, high drive[a] | | | $t_{HRF,25pF}$ | |
| $t_{SPIM,WHSCK}$ | SCK high time[a] | $(0.5*t_{CSCK})$ – $t_{RSCK}$ | | | |
| $t_{SPIM,WLSCK}$ | SCK low time[a] | $(0.5*t_{CSCK})$ – $t_{FSCK}$ | | | |
| $t_{SPIM,SUMI}$ | MISO to CLK edge setup time | 19 | | | ns |
| $t_{SPIM,HMI}$ | CLK edge to MISO hold time | 18 | | | ns |
| $t_{SPIM,VMO}$ | CLK edge to MOSI valid | | | 59 | ns |
| $t_{SPIM,HMO}$ | MOSI hold time after CLK edge | 20 | | | ns |

[22] High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
[23] The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.
[a] At 25pF load, including GPIO pin capacitance, see GPIO spec.

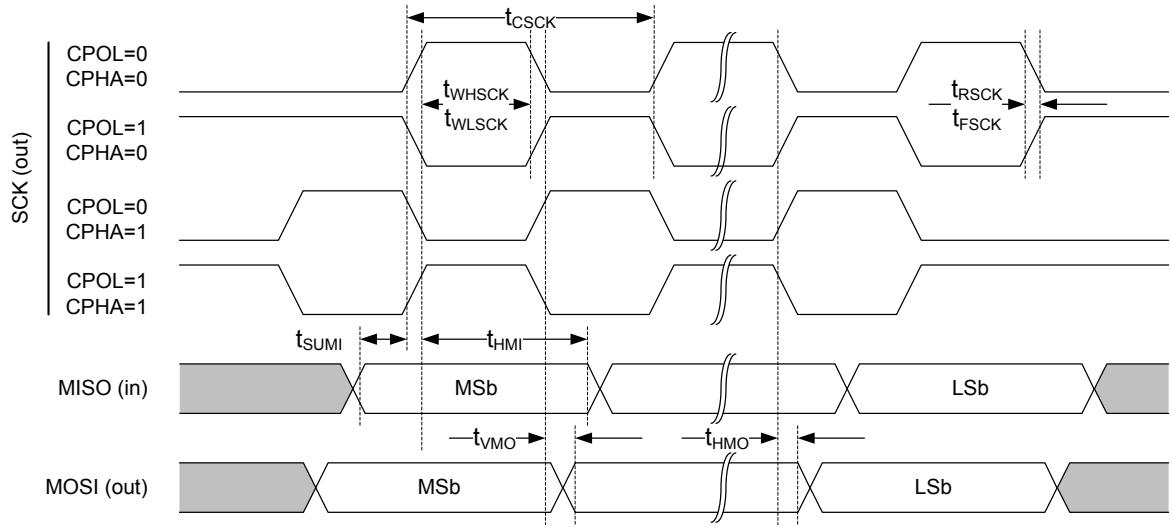



**Figure 82: SPIM timing diagram**

# 31 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

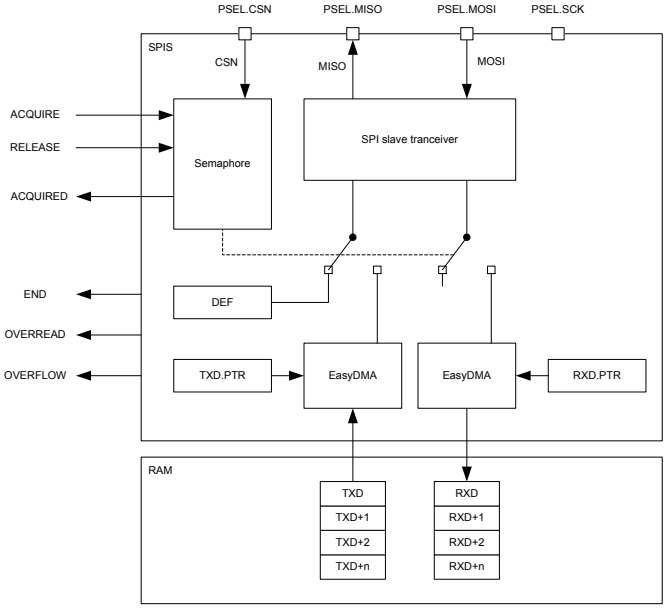



**Figure 83: SPI slave**

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

**Table 62: SPI modes**

| Mode | Clock polarity CPOL | Clock phase CPHA |
|---|---|---|
| SPI_MODE0 | 0 (Leading) | 0 (Active High) |
| SPI_MODE1 | 0 (Leading) | 1 (Active Low) |
| SPI_MODE2 | 1 (Trailing) | 0 (Active High) |
| SPI_MODE3 | 1 (Trailing) | 1 (Active Low) |

## 31.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the SPI slave.

## 31.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

## 31.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See *Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 356.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 356. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 356, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.

The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

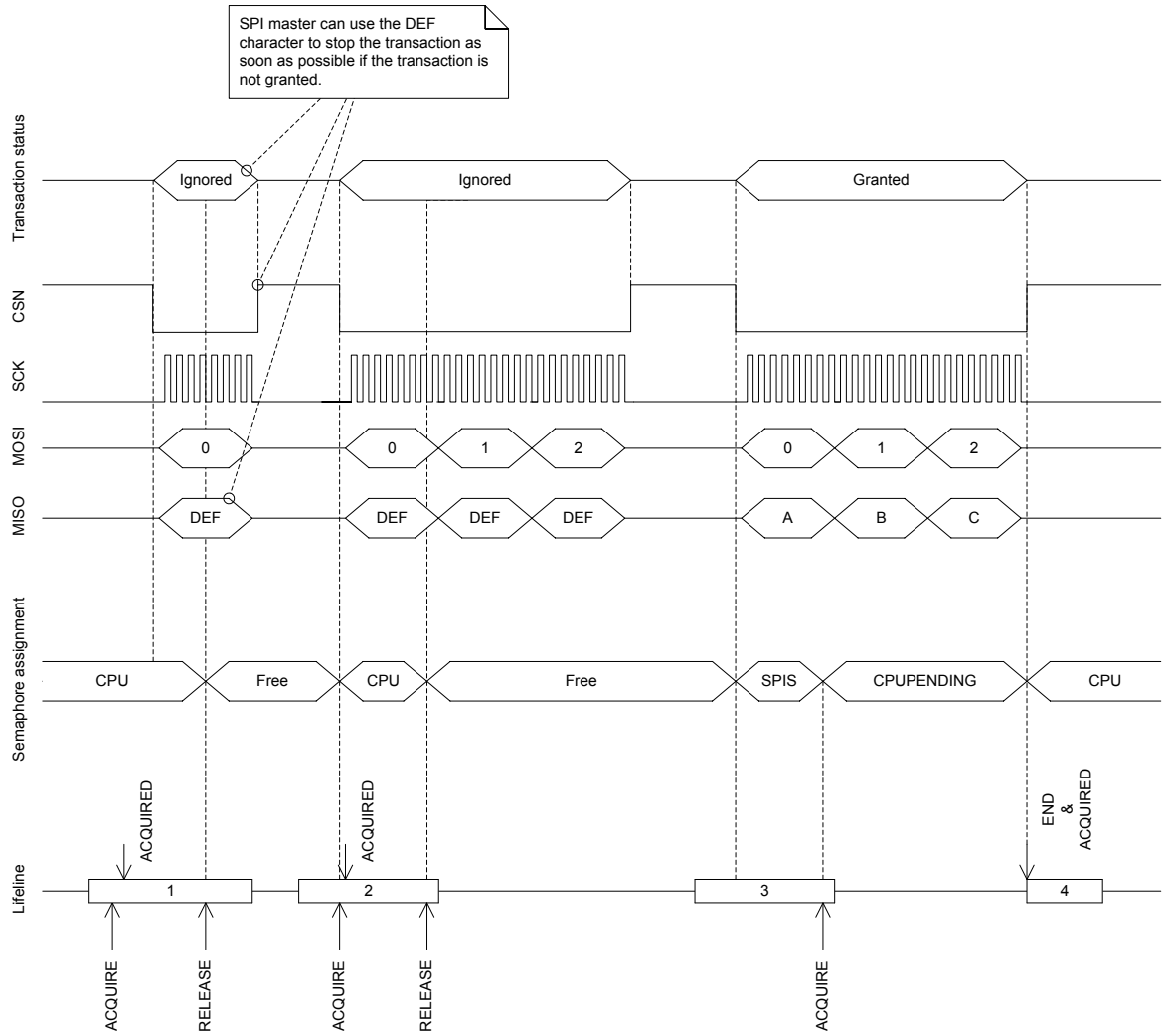



**Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled**

## 31.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER — Power supply* on page 66 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 63: GPIO configuration before enabling peripheral* on page 357 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI

slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

### Table 63: GPIO configuration before enabling peripheral

| SPI signal | SPI pin | Direction | Output value | Comment |
|---|---|---|---|---|
| CSN | As specified in PSEL.CSN | Input | Not applicable | |
| SCK | As specified in PSEL.SCK | Input | Not applicable | |
| MOSI | As specified in PSEL.MOSI | Input | Not applicable | |
| MISO | As specified in PSEL.MISO | Input | Not applicable | Emulates that the SPI slave is not selected. |

## 31.5 Registers

### Table 64: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40003000 | SPIS | SPIS0 | SPI slave 0 | |
| 0x40004000 | SPIS | SPIS1 | SPI slave 1 | |
| 0x40023000 | SPIS | SPIS2 | SPI slave 2 | |

### Table 65: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| TASKS_ACQUIRE | 0x024 | Acquire SPI semaphore | |
| TASKS_RELEASE | 0x028 | Release SPI semaphore, enabling the SPI slave to acquire it | |
| EVENTS_END | 0x104 | Granted transaction completed | |
| EVENTS_ENDRX | 0x110 | End of RXD buffer reached | |
| EVENTS_ACQUIRED | 0x128 | Semaphore acquired | |
| *SHORTS* | 0x200 | Shortcut register | |
| *INTENSET* | 0x304 | Enable interrupt | |
| *INTENCLR* | 0x308 | Disable interrupt | |
| *SEMSTAT* | 0x400 | Semaphore status register | |
| *STATUS* | 0x440 | Status from last transaction | |
| *ENABLE* | 0x500 | Enable SPI slave | |
| *PSELSCK* | 0x508 | Pin select for SCK | Deprecated |
| *PSELMISO* | 0x50C | Pin select for MISO | Deprecated |
| *PSELMOSI* | 0x510 | Pin select for MOSI | Deprecated |
| *PSELCSN* | 0x514 | Pin select for CSN | Deprecated |
| *PSEL.SCK* | 0x508 | Pin select for SCK | |
| *PSEL.MISO* | 0x50C | Pin select for MISO signal | |
| *PSEL.MOSI* | 0x510 | Pin select for MOSI signal | |
| *PSEL.CSN* | 0x514 | Pin select for CSN signal | |
| *RXDPTR* | 0x534 | RXD data pointer | Deprecated |
| *MAXRX* | 0x538 | Maximum number of bytes in receive buffer | Deprecated |
| *AMOUNTRX* | 0x53C | Number of bytes received in last granted transaction | Deprecated |
| *RXD.PTR* | 0x534 | RXD data pointer | |
| *RXD.MAXCNT* | 0x538 | Maximum number of bytes in receive buffer | |
| *RXD.AMOUNT* | 0x53C | Number of bytes received in last granted transaction | |
| *TXDPTR* | 0x544 | TXD data pointer | Deprecated |
| *MAXTX* | 0x548 | Maximum number of bytes in transmit buffer | Deprecated |
| *AMOUNTTX* | 0x54C | Number of bytes transmitted in last granted transaction | Deprecated |
| *TXD.PTR* | 0x544 | TXD data pointer | |
| *TXD.MAXCNT* | 0x548 | Maximum number of bytes in transmit buffer | |
| *TXD.AMOUNT* | 0x54C | Number of bytes transmitted in last granted transaction | |
| *CONFIG* | 0x554 | Configuration register | |

| Register | Offset | Description |
|---|---|---|
| *DEF* | 0x55C | Default character. Character clocked out in case of an ignored transaction. |
| *ORC* | 0x5C0 | Over-read character |

## 31.5.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | END_ACQUIRE | | | Shortcut between END event and ACQUIRE task |
| | | | | | See *EVENTS_END* and *TASKS_ACQUIRE* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 31.5.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | END | | | Write '1' to Enable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | ENDRX | | | Write '1' to Enable interrupt for ENDRX event |
| | | | | | See *EVENTS_ENDRX* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | ACQUIRED | | | Write '1' to Enable interrupt for ACQUIRED event |
| | | | | | See *EVENTS_ACQUIRED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 31.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | END | | | Write '1' to Disable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | ENDRX | | | Write '1' to Disable interrupt for ENDRX event |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | C | | | | | | B | | | A | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_ENDRX* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | ACQUIRED | | | Write '1' to Disable interrupt for ACQUIRED event |
| | | | | | See *EVENTS_ACQUIRED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 31.5.4 SEMSTAT

Address offset: 0x400

Semaphore status register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000001** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | SEMSTAT | | | Semaphore status |
| | | | Free | 0 | Semaphore is free |
| | | | CPU | 1 | Semaphore is assigned to CPU |
| | | | SPIS | 2 | Semaphore is assigned to SPI slave |
| | | | CPUPending | 3 | Semaphore is assigned to SPI but a handover to the CPU is pending |

## 31.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | OVERREAD | | | TX buffer over-read detected, and prevented |
| | | | NotPresent | 0 | Read: error not present |
| | | | Present | 1 | Read: error present |
| | | | Clear | 1 | Write: clear error on writing '1' |
| B | RW | OVERFLOW | | | RX buffer overflow detected, and prevented |
| | | | NotPresent | 0 | Read: error not present |
| | | | Present | 1 | Read: error present |
| | | | Clear | 1 | Write: clear error on writing '1' |

## 31.5.6 ENABLE

Address offset: 0x500

Enable SPI slave

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ENABLE | | | Enable or disable SPI slave |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.7 PSELSCK ( Deprecated )

Address offset: 0x508

Pin select for SCK

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELSCK | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.8 PSELMISO ( Deprecated )

Address offset: 0x50C

Pin select for MISO

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELMISO | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.9 PSELMOSI ( Deprecated )

Address offset: 0x510

Pin select for MOSI

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELMOSI | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.10 PSELCSN ( Deprecated )

Address offset: 0x514

Pin select for CSN

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELCSN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.11 PSEL.SCK

Address offset: 0x508

Pin select for SCK

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | |

## 31.5.12 PSEL.MISO

Address offset: 0x50C

Pin select for MISO signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | |

## 31.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | |

## 31.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | |

## 31.5.15 RXDPTR ( Deprecated )

Address offset: 0x534

RXD data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | RXDPTR | | | RXD data pointer |

## 31.5.16 MAXRX ( Deprecated )

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXRX | | | Maximum number of bytes in receive buffer |

## 31.5.17 AMOUNTRX ( Deprecated )

Address offset: 0x53C

Number of bytes received in last granted transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNTRX | | | Number of bytes received in the last granted transaction |

## 31.5.18 RXD.PTR

Address offset: 0x534

RXD data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | RXD data pointer |

## 31.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in receive buffer |

## 31.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes received in the last granted transaction |

### 31.5.21 TXDPTR ( Deprecated )

Address offset: 0x544

TXD data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TXDPTR | | | TXD data pointer |

### 31.5.22 MAXTX ( Deprecated )

Address offset: 0x548

Maximum number of bytes in transmit buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXTX | | | Maximum number of bytes in transmit buffer |

### 31.5.23 AMOUNTTX ( Deprecated )

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNTTX | | | Number of bytes transmitted in last granted transaction |

### 31.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | TXD data pointer |

### 31.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in transmit buffer |

### 31.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | AMOUNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Number of bytes transmitted in last granted transaction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.27 CONFIG

Address offset: 0x554

Configuration register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ORDER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | MsbFirst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Most significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LsbFirst | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Least significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CPHA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) phase | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Leading | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on leading edge of clock, shift serial data on trailing edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Trailing | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on trailing edge of clock, shift serial data on leading edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CPOL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) polarity | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveHigh | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveLow | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | DEF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Default character. Character clocked out in case of an ignored transaction. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 31.5.29 ORC

Address offset: 0x5C0

Over-read character

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ORC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Over-read character. Character clocked out after an over-read of the transmit buffer. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 31.6 Electrical specification

## 31.6.1 SPIS slave interface electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{SPIS}$ | Bit rates for SPIS[24] | | | 8[25] | Mbps |
| $I_{SPIS,2Mbps}$ | Run current for SPIS, 2 Mbps | | 45 | | µA |
| $I_{SPIS,8Mbps}$ | Run current for SPIS, 8 Mbps | | 45 | | µA |
| $I_{SPIS,IDLE}$ | Idle current for SPIS (STARTed, no CSN activity) | | 1 | | µA |
| $t_{SPIS,START}$ | Time from RELEASE task to receive/transmit (CSN active) | | 0.125 | | µs |

## 31.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{SPIS,CSCKIN}$ | SCK input period | 125 | | | ns |
| $t_{SPIS,RFSCKIN}$ | SCK input rise/fall time | | | 30 | ns |
| $t_{SPIS,WHSCKIN}$ | SCK input high time | 30 | | | ns |
| $t_{SPIS,WLSCKIN}$ | SCK input low time | 30 | | | ns |
| $t_{SPIS,SUCSN}$ | CSN to CLK setup time | 1000 | | | ns |
| $t_{SPIS,HCSN}$ | CLK to CSN hold time | 2000 | | | ns |
| $t_{SPIS,ASA}$ | CSN to MISO driven | 0 | | | ns |
| $t_{SPIS,ASO}$ | CSN to MISO valid[a] | | | 1000 | ns |
| $t_{SPIS,DISSO}$ | CSN to MISO disabled[a] | | | 68 | ns |
| $t_{SPIS,CWH}$ | CSN inactive time | 300 | | | ns |
| $t_{SPIS,VSO}$ | CLK edge to MISO valid | | | 19 | ns |
| $t_{SPIS,HSO}$ | MISO hold time after CLK edge | 18[26] | | | ns |
| $t_{SPIS,SUSI}$ | MOSI to CLK edge setup time | 59 | | | ns |
| $t_{SPIS,HSI}$ | CLK edge to MOSI hold time | 20 | | | ns |

[24] High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

[25] The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

[a] At 25pF load, including GPIO capacitance, see GPIO spec.

[26] This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output

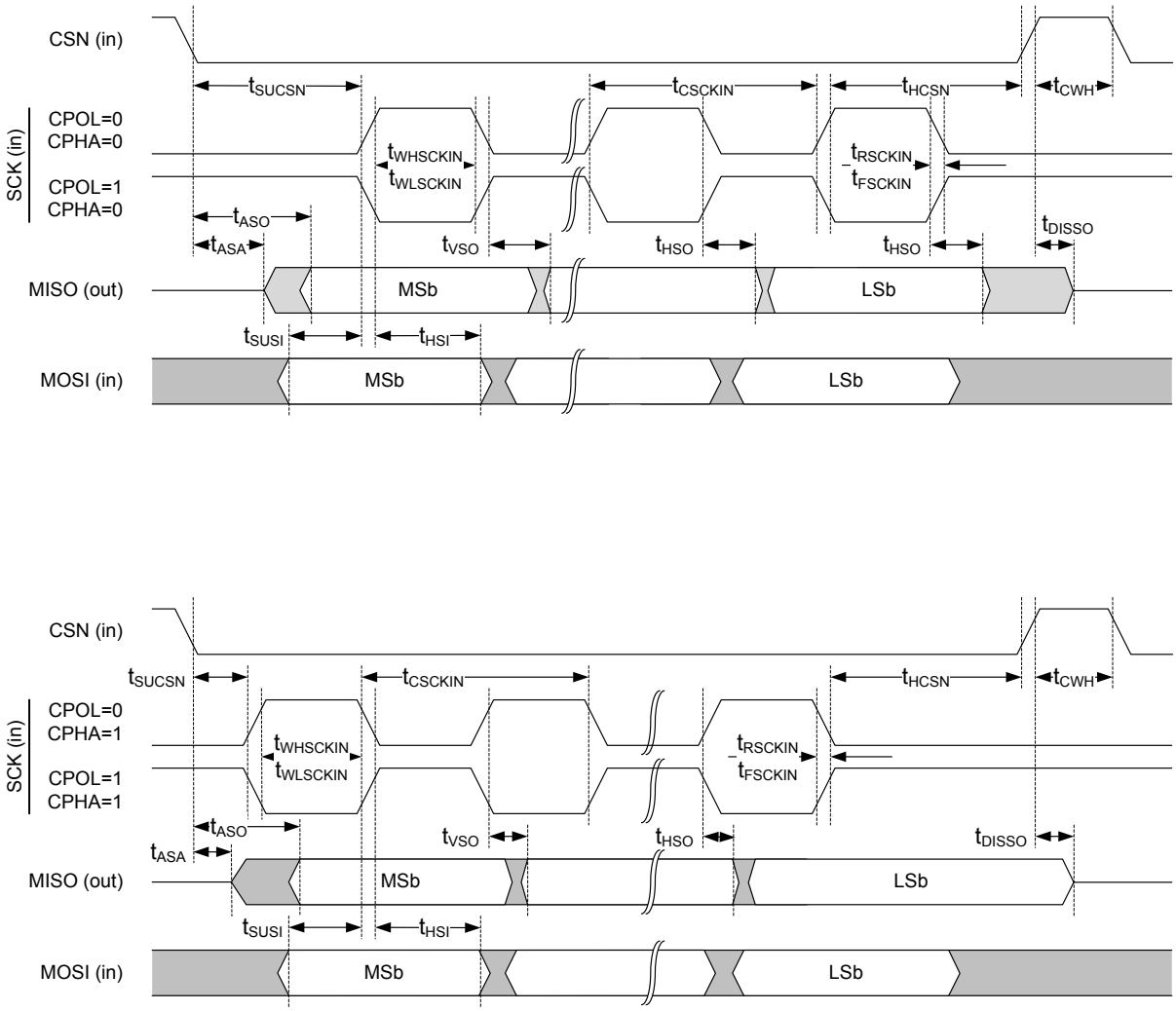



**Figure 85: SPIS timing diagram**

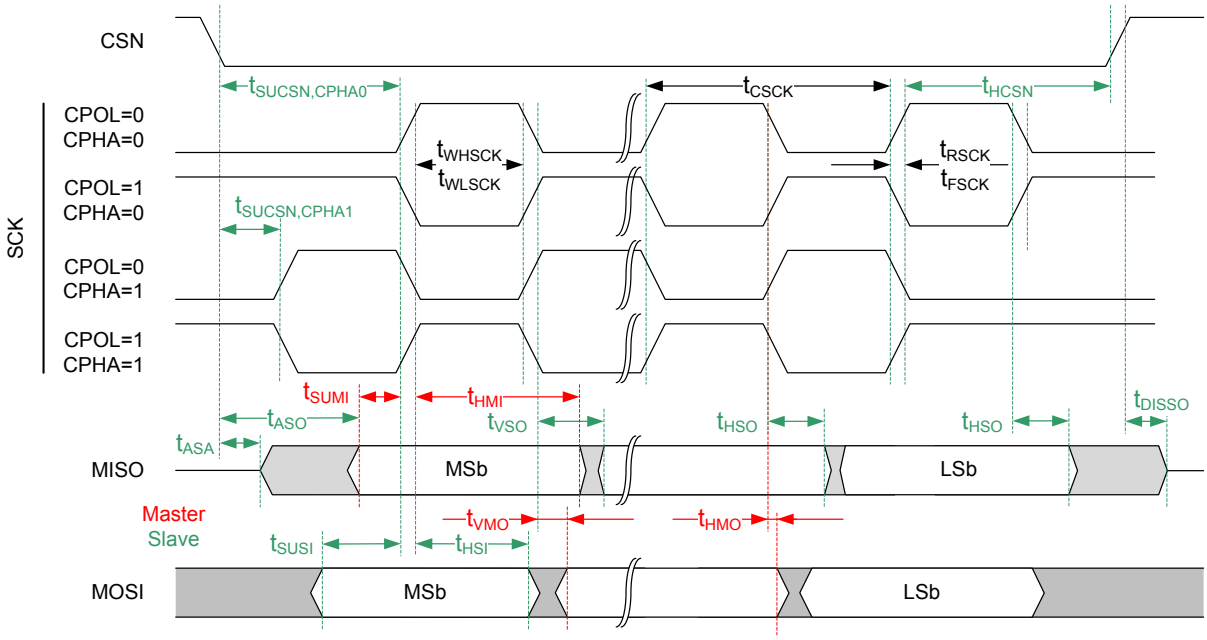



**Figure 86: Common SPIM and SPIS timing diagram**

# 32 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

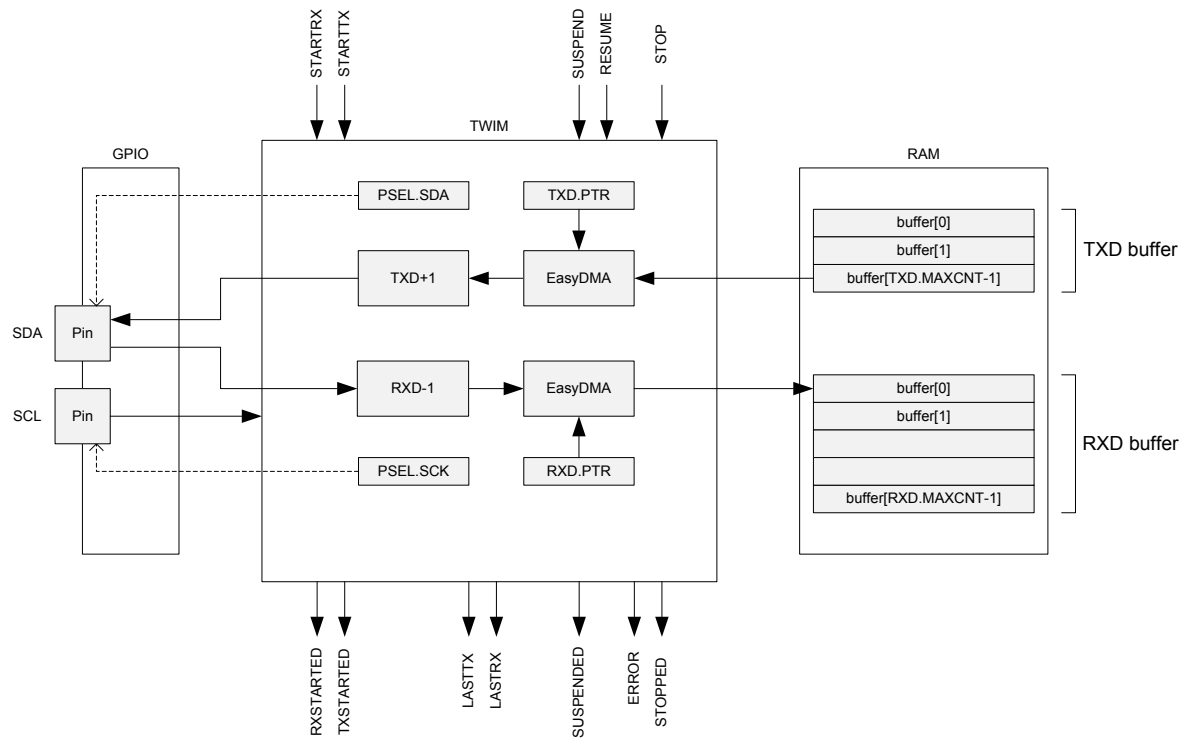



**Figure 87: TWI master with EasyDMA**

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 88: A typical TWI setup comprising one master and three slaves* on page 368. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.

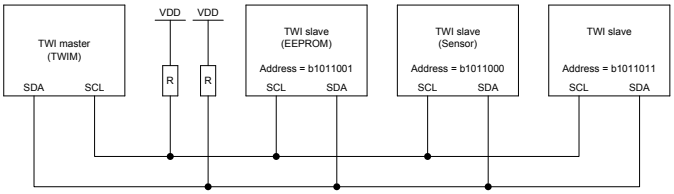



**Figure 88: A typical TWI setup comprising one master and three slaves**

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

## 32.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI.

## 32.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

## 32.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 89: TWI master writing data to a slave* on page 369. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

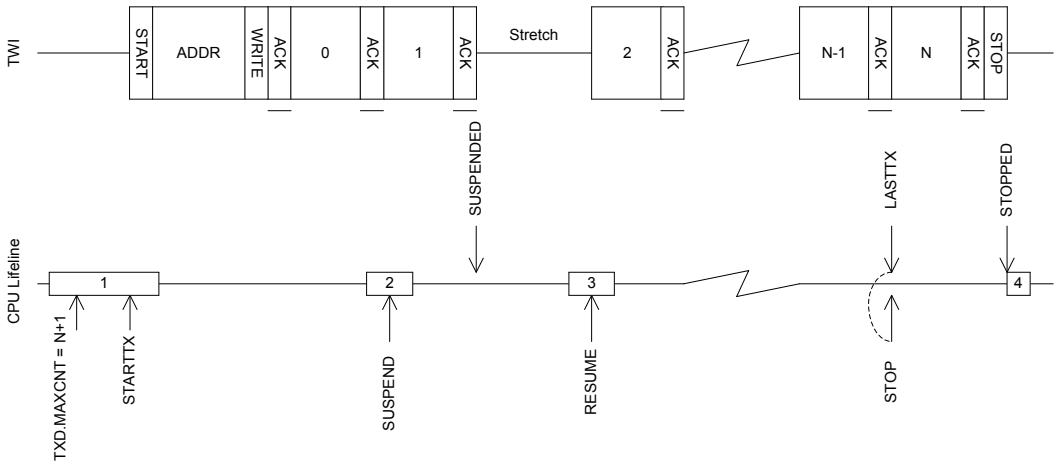



**Figure 89: TWI master writing data to a slave**

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 89: TWI master writing data to a slave* on page 369

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

## 32.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 90: The TWI master reading data from a slave* on page 370. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 90: The TWI master reading data from a slave* on page 370. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

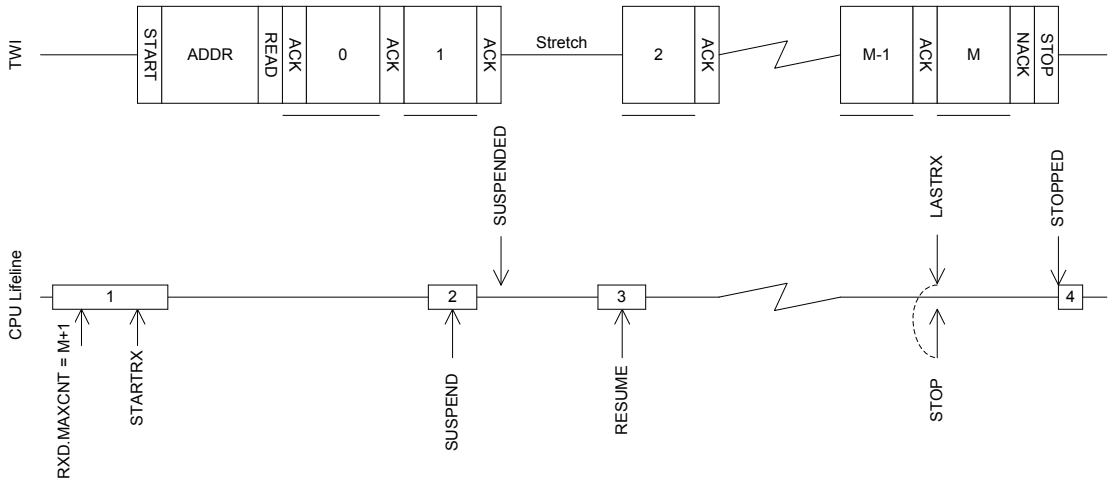



**Figure 90: The TWI master reading data from a slave**

## 32.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure *Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave* on page 370 illustrates this:

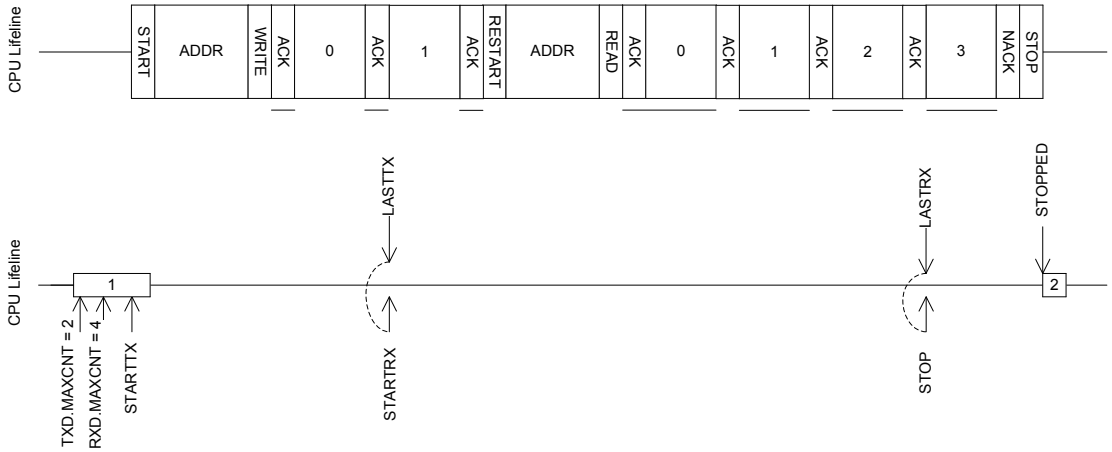



**Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave**

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the

correct tasks are generated at the correct time. This is illustrated in *Figure 92: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts* on page 371.

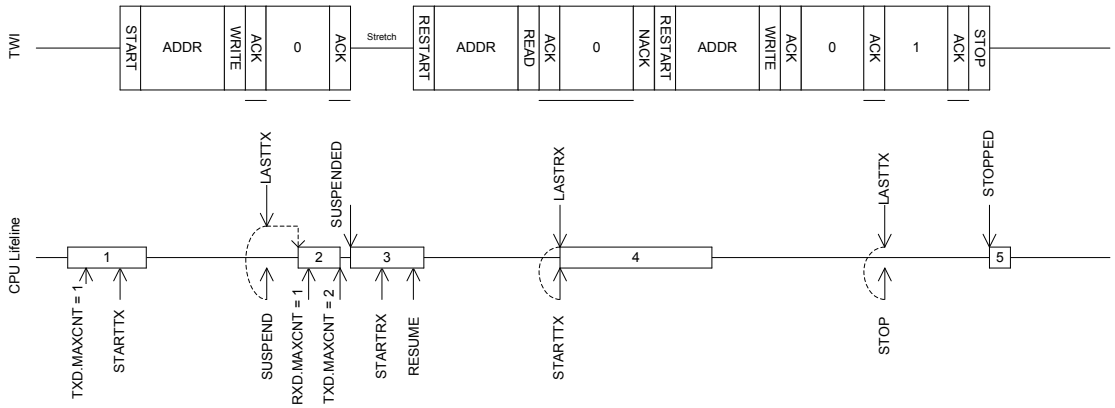



**Figure 92: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts**

## 32.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

## 32.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 66: GPIO configuration before enabling peripheral* on page 371.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

**Table 66: GPIO configuration before enabling peripheral**

| TWI master signal | TWI master pin | Direction | Output value | Drive strength |
|---|---|---|---|---|
| SCL | As specified in PSEL.SCL | Input | Not applicable | S0D1 |
| SDA | As specified in PSEL.SDA | Input | Not applicable | S0D1 |

## 32.8 Registers

**Table 67: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40003000 | TWIM | TWIM0 | Two-wire interface master 0 | |
| 0x40004000 | TWIM | TWIM1 | Two-wire interface master 1 | |

### Table 68: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTRX | 0x000 | Start TWI receive sequence |
| TASKS_STARTTX | 0x008 | Start TWI transmit sequence |
| TASKS_STOP | 0x014 | Stop TWI transaction. Must be issued while the TWI master is not suspended. |
| TASKS_SUSPEND | 0x01C | Suspend TWI transaction |
| TASKS_RESUME | 0x020 | Resume TWI transaction |
| EVENTS_STOPPED | 0x104 | TWI stopped |
| EVENTS_ERROR | 0x124 | TWI error |
| EVENTS_SUSPENDED | 0x148 | Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended. |
| EVENTS_RXSTARTED | 0x14C | Receive sequence started |
| EVENTS_TXSTARTED | 0x150 | Transmit sequence started |
| EVENTS_LASTRX | 0x15C | Byte boundary, starting to receive the last byte |
| EVENTS_LASTTX | 0x160 | Byte boundary, starting to transmit the last byte |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSRC* | 0x4C4 | Error source |
| *ENABLE* | 0x500 | Enable TWIM |
| *PSEL.SCL* | 0x508 | Pin select for SCL signal |
| *PSEL.SDA* | 0x50C | Pin select for SDA signal |
| *FREQUENCY* | 0x524 | TWI frequency. Accuracy depends on the HFCLK source selected. |
| *RXD.PTR* | 0x534 | Data pointer |
| *RXD.MAXCNT* | 0x538 | Maximum number of bytes in receive buffer |
| *RXD.AMOUNT* | 0x53C | Number of bytes transferred in the last transaction |
| *RXD.LIST* | 0x540 | EasyDMA list type |
| *TXD.PTR* | 0x544 | Data pointer |
| *TXD.MAXCNT* | 0x548 | Maximum number of bytes in transmit buffer |
| *TXD.AMOUNT* | 0x54C | Number of bytes transferred in the last transaction |
| *TXD.LIST* | 0x550 | EasyDMA list type |
| *ADDRESS* | 0x588 | Address used in the TWI transfer |

## 32.8.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | F | | D | C | B | A | | | | | |
| **Reset 0x00000000** | | | | | | | | | | | | | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | LASTTX_STARTRX | | | Shortcut between LASTTX event and STARTRX task<br><br>See *EVENTS_LASTTX* and *TASKS_STARTRX* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | LASTTX_SUSPEND | | | Shortcut between LASTTX event and SUSPEND task<br><br>See *EVENTS_LASTTX* and *TASKS_SUSPEND* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| C | RW | LASTTX_STOP | | | Shortcut between LASTTX event and STOP task<br><br>See *EVENTS_LASTTX* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| D | RW | LASTRX_STARTTX | | | Shortcut between LASTRX event and STARTTX task<br><br>See *EVENTS_LASTRX* and *TASKS_STARTTX* |
| | | | Disabled | 0 | Disable shortcut |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | F | | D | C | B | A | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | LASTRX_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_LASTRX* and *TASKS_STOP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | J | I | | | H | G | F | | | | | | | | | D | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STOPPED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ERROR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SUSPENDED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_SUSPENDED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | LASTRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_LASTRX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | LASTTX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_LASTTX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | J | I | | | H | G | F | | | | | | | | | D | | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SUSPENDED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | LASTRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | LASTTX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | J | I | | | H | G | F | | | | | | | | | D | | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | J | I | | | H | G | F | | | | | | | | | D | | | | | | | | A | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| F | RW | SUSPENDED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for SUSPENDED event<br><br>See *EVENTS_SUSPENDED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| G | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for RXSTARTED event<br><br>See *EVENTS_RXSTARTED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| H | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for TXSTARTED event<br><br>See *EVENTS_TXSTARTED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| I | RW | LASTRX | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for LASTRX event<br><br>See *EVENTS_LASTRX* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| J | RW | LASTTX | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for LASTTX event<br><br>See *EVENTS_LASTTX* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |

## 32.8.5 ERRORSRC

Address offset: 0x4C4

Error source

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | OVERRUN | | | | | | | | | | | | | | | | | | | | | | | | Overrun error<br><br>A new byte was received before previous byte got transferred into RXD buffer. (Previous data is lost) | | | | | | | | | |
| | | | NotReceived | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Received | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |
| B | RW | ANACK | | | | | | | | | | | | | | | | | | | | | | | | NACK received after sending the address (write '1' to clear) | | | | | | | | | |
| | | | NotReceived | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Received | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |
| C | RW | DNACK | | | | | | | | | | | | | | | | | | | | | | | | NACK received after sending a data byte (write '1' to clear) | | | | | | | | | |
| | | | NotReceived | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Received | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |

## 32.8.6 ENABLE

Address offset: 0x500

Enable TWIM

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.8 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.9 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x04000000** | | | | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FREQUENCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K100 | 0x01980000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K250 | 0x04000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K400 | 0x06400000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 32.8.10 RXD.PTR

Address offset: 0x534

Data pointer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PTR | | | Data pointer |

## 32.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | MAXCNT | | [1..255] | Maximum number of bytes in receive buffer |

## 32.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte. |

## 32.8.13 RXD.LIST

Address offset: 0x540

EasyDMA list type

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | LIST | | | List type |
| | | | Disabled | 0 | Disable EasyDMA list |
| | | | ArrayList | 1 | Use array list |

## 32.8.14 TXD.PTR

Address offset: 0x544

Data pointer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PTR | | | Data pointer |

## 32.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | MAXCNT | | [1..255] | Maximum number of bytes in transmit buffer |

## 32.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte. |

## 32.8.17 TXD.LIST

Address offset: 0x550

EasyDMA list type

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | LIST | | | List type |
| | | | Disabled | 0 | Disable EasyDMA list |
| | | | ArrayList | 1 | Use array list |

## 32.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ADDRESS | | | Address used in the TWI transfer |

# 32.9 Electrical specification

## 32.9.1 TWIM interface electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{TWIM,SCL}$ | Bit rates for TWIM[27] | 100 | | 400 | kbps |
| $I_{TWIM,100kbps}$ | Run current for TWIM, 100 kbps | | 50 | | µA |
| $I_{TWIM,400kbps}$ | Run current for TWIM, 400 kbps | | 50 | | µA |
| $t_{TWIM,START}$ | Time from STARTRX/STARTTX task to transmission started | | 1.5 | | µs |

## 32.9.2 Two Wire Interface Master (TWIM) timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWIM,SU\_DAT}$ | Data setup time before positive edge on SCL – all modes | 300 | | | ns |
| $t_{TWIM,HD\_DAT}$ | Data hold time after negative edge on SCL – all modes | 500 | | | ns |

[27] High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWIM,HD\_STA,100kbps}$ | TWIM master hold time for START and repeated START condition, 100 kbps | 10000 | | | ns |
| $t_{TWIM,HD\_STA,250kbps}$ | TWIM master hold time for START and repeated START condition, 250kbps | 4000 | | | ns |
| $t_{TWIM,HD\_STA,400kbps}$ | TWIM master hold time for START and repeated START condition, 400 kbps | 2500 | | | ns |
| $t_{TWIM,SU\_STO,100kbps}$ | TWIM master setup time from SCL high to STOP condition, 100 kbps | 5000 | | | ns |
| $t_{TWIM,SU\_STO,250kbps}$ | TWIM master setup time from SCL high to STOP condition, 250 kbps | 2000 | | | ns |
| $t_{TWIM,SU\_STO,400kbps}$ | TWIM master setup time from SCL high to STOP condition, 400 kbps | 1250 | | | ns |
| $t_{TWIM,BUF,100kbps}$ | TWIM master bus free time between STOP and START conditions, 100 kbps | 5800 | | | ns |
| $t_{TWIM,BUF,250kbps}$ | TWIM master bus free time between STOP and START conditions, 250 kbps | 2700 | | | ns |
| $t_{TWIM,BUF,400kbps}$ | TWIM master bus free time between STOP and START conditions, 400 kbps | 2100 | | | ns |

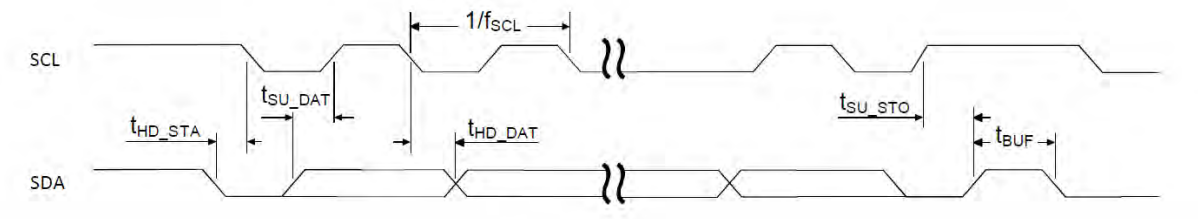



**Figure 93: TWIM timing diagram, 1 byte transaction**

## 32.10 Pullup resistor

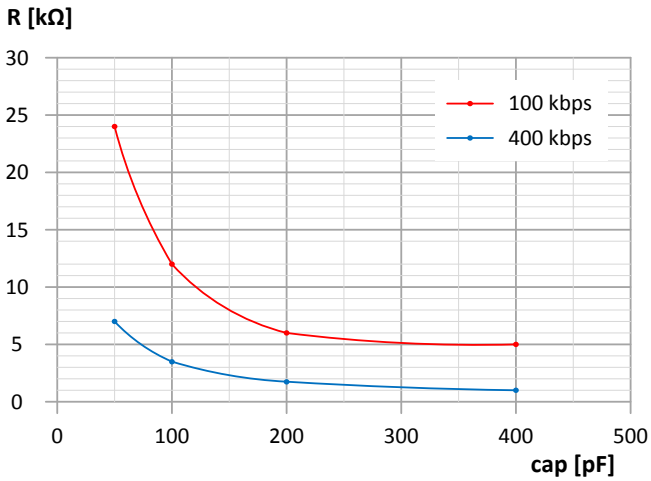



**Figure 94: Recommended TWIM pullup value vs. line capacitance**

- The I2C specification allows a line capacitance of 400 pF at most.
- The value of internal pullup resistor ($R_{PU}$) for nRF52840 can be found in the *GPIO — General purpose input/output* on page 154 section.

# 33 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

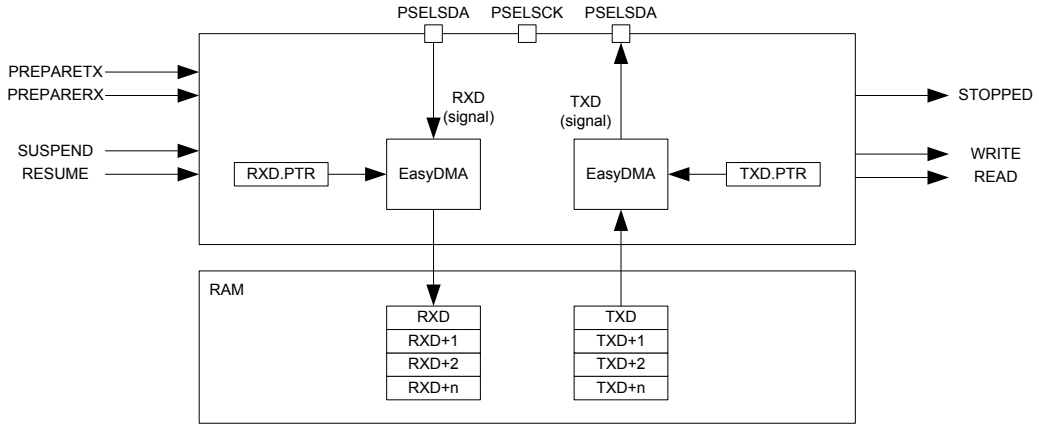



**Figure 95: TWI slave with EasyDMA**

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 96: A typical TWI setup comprising one master and three slaves* on page 380. TWIS is only able to operate with a single master on the TWI bus.

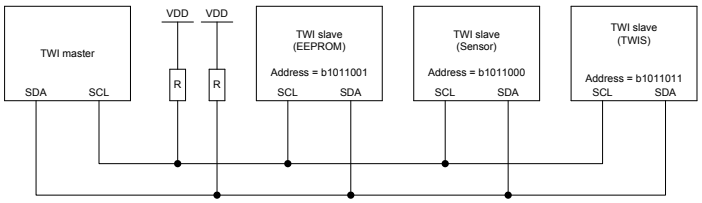



**Figure 96: A typical TWI setup comprising one master and three slaves**

The TWI slave state machine is illustrated in *Figure 97: TWI slave state machine* on page 381 and *Table 69: TWI slave state machine symbols* on page 381 is explaining the different symbols used in the state machine.

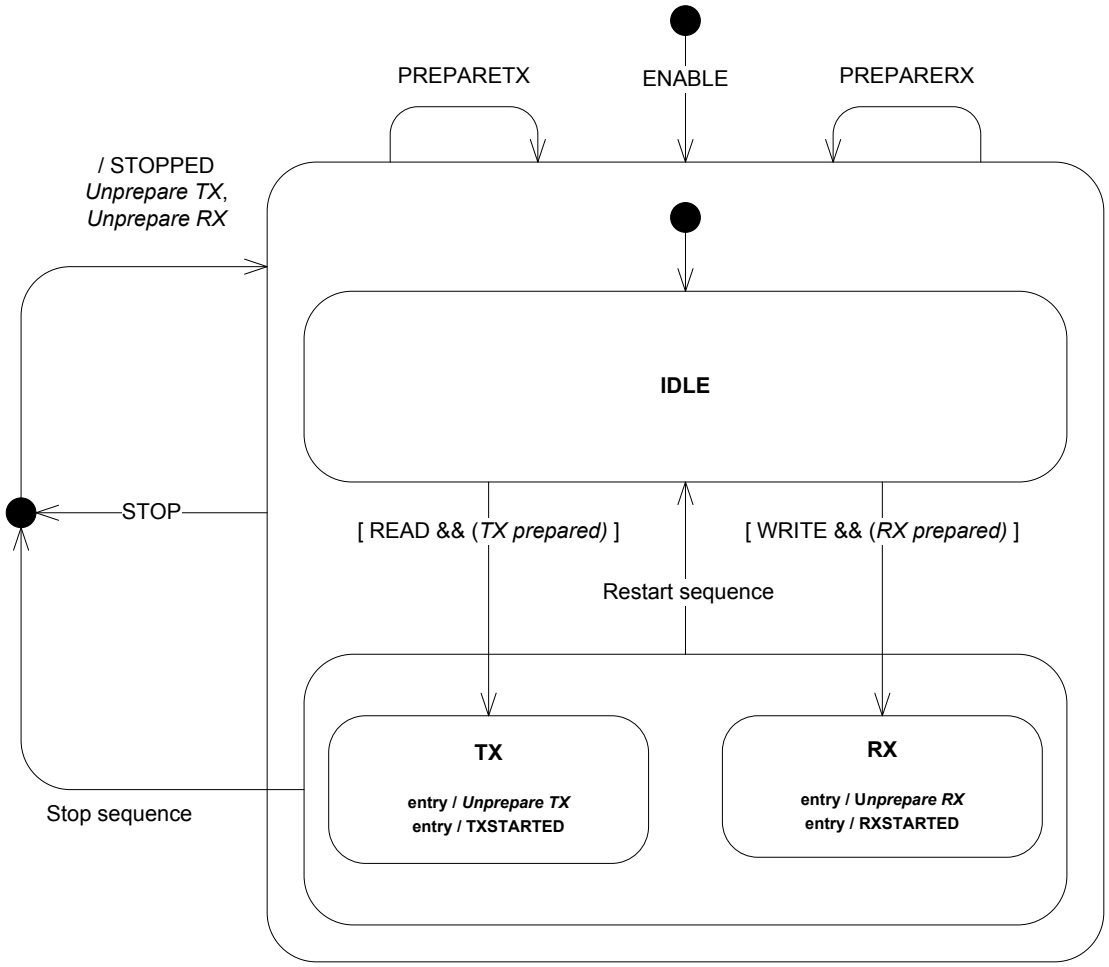



**Figure 97: TWI slave state machine**

**Table 69: TWI slave state machine symbols**

| Symbol | Type | Description |
|---|---|---|
| ENABLE | Register | The TWI slave has been enabled via the *ENABLE* register |
| PREPARETX | Task | The *TASKS_PREPARETX* task has been triggered |
| STOP | Task | The *TASKS_STOP* task has been triggered |
| PREPARERX | Task | The *TASKS_PREPARERX* task has been triggered |
| STOPPED | Event | The *EVENTS_STOPPED* event was generated |
| RXSTARTED | Event | The *EVENTS_RXSTARTED* event was generated |
| TXSTARTED | Event | The *EVENTS_TXSTARTED* event was generated |
| TX prepared | Internal | Internal flag indicating that a *TASKS_PREPARETX* task has been triggered. This flag is not visible to the user. |
| RX prepared | Internal | Internal flag indicating that a *TASKS_PREPARERX* task has been triggered. This flag is not visible to the user. |
| Unprepare TX | Internal | Clears the internal 'TX prepared' flag until next *TASKS_PREPARETX* task. |
| Unprepare RX | Internal | Clears the internal 'RX prepared' flag until next *TASKS_PREPARERX* task. |
| Stop sequence | TWI protocol | A TWI stop sequence was detected |
| Restart sequence | TWI protocol | A TWI restart sequence was detected |

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.

## 33.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI slave.

## 33.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

## 33.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{IDLE}$ .

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume $I_{TX}$ in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master

forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 385.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 98: The TWI slave responding to a read command* on page 383. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

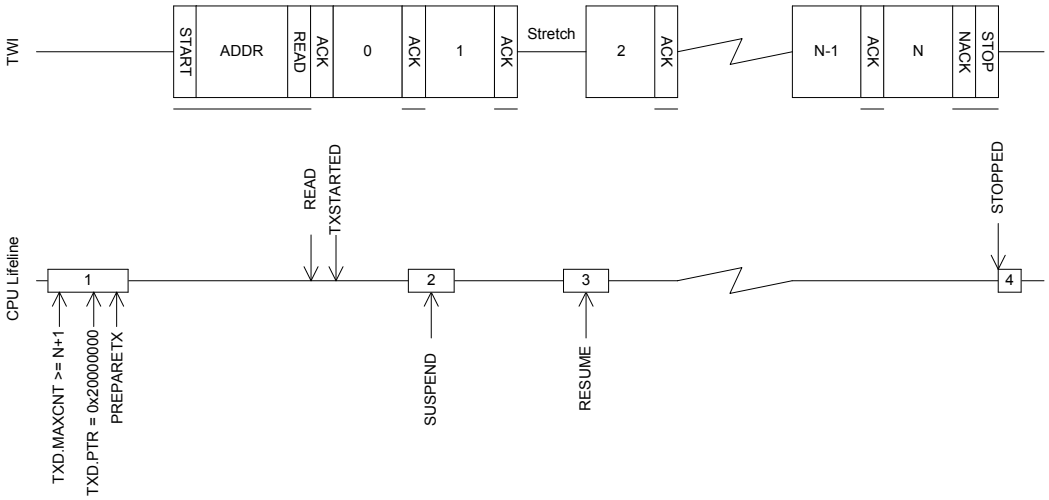



**Figure 98: The TWI slave responding to a read command**

## 33.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.

The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume $I_{RX}$ in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive,these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 385.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 99: The TWI slave responding to a write command* on page 384. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

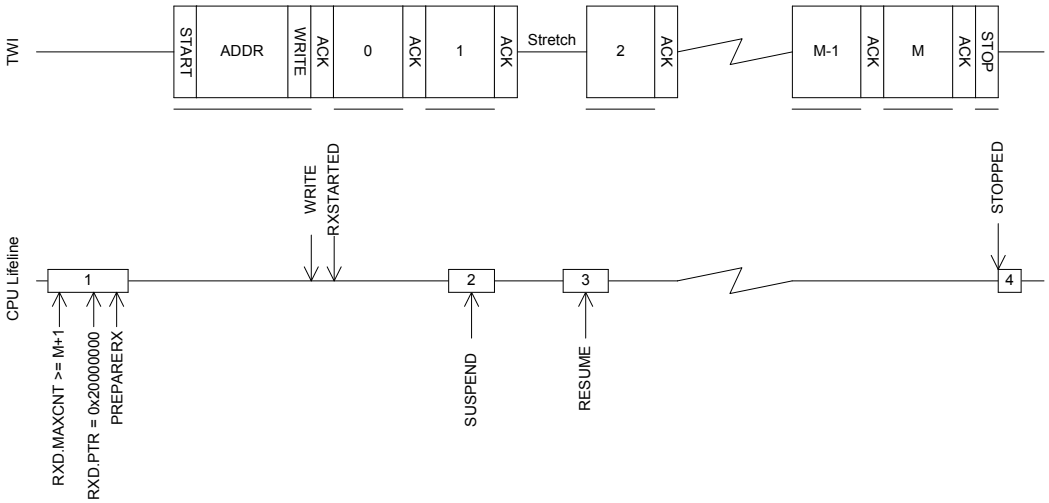



**Figure 99: The TWI slave responding to a write command**

## 33.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in *Figure 100: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave* on page 385.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.

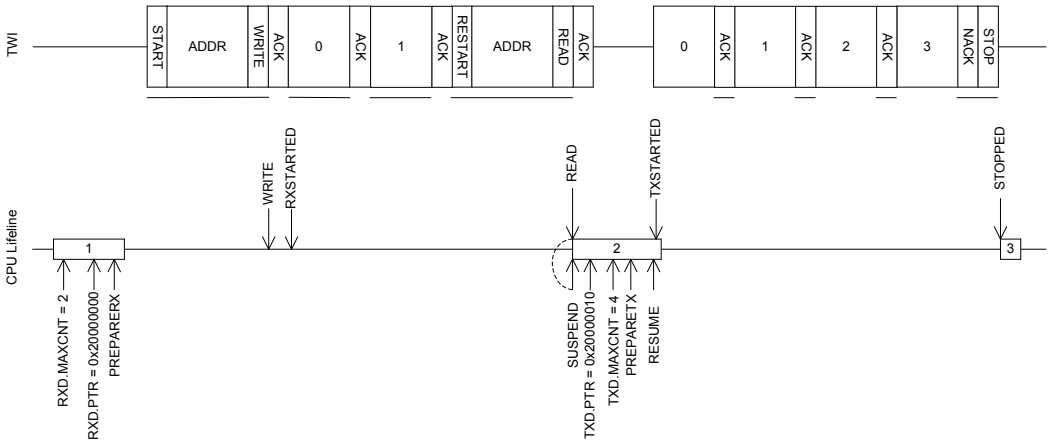



**Figure 100: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave**

## 33.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

## 33.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

## 33.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 70: GPIO configuration before enabling peripheral* on page 385.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

**Table 70: GPIO configuration before enabling peripheral**

| TWI slave signal | TWI slave pin | Direction | Output value | Drive strength |
|---|---|---|---|---|
| SCL | As specified in PSEL.SCL | Input | Not applicable | S0D1 |
| SDA | As specified in PSEL.SDA | Input | Not applicable | S0D1 |

## 33.9 Registers

### Table 71: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40003000 | TWIS | TWIS0 | Two-wire interface slave 0 | |
| 0x40004000 | TWIS | TWIS1 | Two-wire interface slave 1 | |

### Table 72: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STOP | 0x014 | Stop TWI transaction |
| TASKS_SUSPEND | 0x01C | Suspend TWI transaction |
| TASKS_RESUME | 0x020 | Resume TWI transaction |
| TASKS_PREPARERX | 0x030 | Prepare the TWI slave to respond to a write command |
| TASKS_PREPARETX | 0x034 | Prepare the TWI slave to respond to a read command |
| EVENTS_STOPPED | 0x104 | TWI stopped |
| EVENTS_ERROR | 0x124 | TWI error |
| EVENTS_RXSTARTED | 0x14C | Receive sequence started |
| EVENTS_TXSTARTED | 0x150 | Transmit sequence started |
| EVENTS_WRITE | 0x164 | Write command received |
| EVENTS_READ | 0x168 | Read command received |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSRC* | 0x4D0 | Error source |
| *MATCH* | 0x4D4 | Status register indicating which address had a match |
| *ENABLE* | 0x500 | Enable TWIS |
| *PSEL.SCL* | 0x508 | Pin select for SCL signal |
| *PSEL.SDA* | 0x50C | Pin select for SDA signal |
| *RXD.PTR* | 0x534 | RXD Data pointer |
| *RXD.MAXCNT* | 0x538 | Maximum number of bytes in RXD buffer |
| *RXD.AMOUNT* | 0x53C | Number of bytes transferred in the last RXD transaction |
| *TXD.PTR* | 0x544 | TXD Data pointer |
| *TXD.MAXCNT* | 0x548 | Maximum number of bytes in TXD buffer |
| *TXD.AMOUNT* | 0x54C | Number of bytes transferred in the last TXD transaction |
| *ADDRESS[0]* | 0x588 | TWI slave address 0 |
| *ADDRESS[1]* | 0x58C | TWI slave address 1 |
| *CONFIG* | 0x594 | Configuration register for the address match mechanism |
| *ORC* | 0x5C0 | Over-read character. Character sent out in case of an over-read of the transmit buffer. |

## 33.9.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | B | A | | | | | | | | | | | | | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | WRITE_SUSPEND | | | Shortcut between WRITE event and SUSPEND task<br>See *EVENTS_WRITE* and *TASKS_SUSPEND* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | READ_SUSPEND | | | Shortcut between READ event and SUSPEND task<br>See *EVENTS_READ* and *TASKS_SUSPEND* |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | B | A | | | | | | | | | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable shortcut | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable shortcut | | | | | | | | | |

## 33.9.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | H | G | | | | | F | E | | | | | | | | | | B | | | | | | | A | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for STOPPED event<br><br>See *EVENTS_STOPPED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| B | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for ERROR event<br><br>See *EVENTS_ERROR* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| E | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for RXSTARTED event<br><br>See *EVENTS_RXSTARTED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| F | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for TXSTARTED event<br><br>See *EVENTS_TXSTARTED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| G | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for WRITE event<br><br>See *EVENTS_WRITE* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| H | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for READ event<br><br>See *EVENTS_READ* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |

## 33.9.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | H | G | | | | | F | E | | | | | | | | | | B | | | | | | | A | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for STOPPED event<br><br>See *EVENTS_STOPPED* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| B | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for ERROR event | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | H | G | | | | | F | E | | | | | | | | | | B | | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ERROR* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| E | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for RXSTARTED event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_RXSTARTED* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| F | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for TXSTARTED event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_TXSTARTED* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| G | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for WRITE event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_WRITE* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| H | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for READ event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_READ* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |

## 33.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | H | G | | | | | F | E | | | | | | | | | | B | | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for STOPPED event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_STOPPED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| B | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ERROR event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ERROR* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| E | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for RXSTARTED event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_RXSTARTED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| F | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for TXSTARTED event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_TXSTARTED* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | H | G | | | | | F | E | | | | | | | | | | B | | | | | | | | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| G | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for WRITE event<br><br>See *EVENTS_WRITE* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| H | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for READ event<br><br>See *EVENTS_READ* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |

## 33.9.5 ERRORSRC

Address offset: 0x4D0

Error source

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | OVERFLOW | | | | | | | | | | | | | | | | | | | | | | | | RX buffer overflow detected, and prevented | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |
| B | RW | DNACK | | | | | | | | | | | | | | | | | | | | | | | | NACK sent after receiving a data byte | | | | | | | | | |
| | | | NotReceived | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Received | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |
| C | RW | OVERREAD | | | | | | | | | | | | | | | | | | | | | | | | TX buffer over-read detected, and prevented | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | Error did not occur | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | Error occurred | | | | | | | | | |

## 33.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | R | MATCH | | [0..1] | | | | | | | | | | | | | | | | | | | | | | Which of the addresses in {ADDRESS} matched the incoming address | | | | | | | | | |

## 33.9.7 ENABLE

Address offset: 0x500

Enable TWIS

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable TWIS | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable TWIS | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 33.9.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 33.9.9 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 33.9.10 RXD.PTR

Address offset: 0x534

RXD Data pointer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 33.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MAXCNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 33.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last RXD transaction |

## 33.9.13 TXD.PTR

Address offset: 0x544

TXD Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | TXD Data pointer |

## 33.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in TXD buffer |

## 33.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last TXD transaction |

## 33.9.16 ADDRESS[0]

Address offset: 0x588

TWI slave address 0

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ADDRESS | | | TWI slave address |

## 33.9.17 ADDRESS[1]

Address offset: 0x58C

TWI slave address 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | ADDRESS | | | | | | | | | | | | | | | | | | | | | | | | | | | TWI slave address | | | | | | |

## 33.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | ADDRESS0 | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable address matching on ADDRESS[0] | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | Disabled | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | Enabled | | | | | | |
| B | RW | ADDRESS1 | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable address matching on ADDRESS[1] | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | Disabled | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | Enabled | | | | | | |

## 33.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | ORC | | | | | | | | | | | | | | | | | | | | | | | | | | | Over-read character. Character sent out in case of an over-read of the transmit buffer. | | | | | | |

# 33.10 Electrical specification

## 33.10.1 TWIS slave interface electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{TWIS,SCL}$ | Bit rates for TWIS[28] | 100 | | 400 | kbps |
| $I_{TWIS,100kbps}$ | Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps | | 45 | | µA |
| $I_{TWIS,400kbps}$ | Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps | | 45 | | µA |
| $I_{TWIS,IDLE}$ | Idle current for TWIS | | 1 | | µA |
| $t_{TWIS,START}$ | Time from PREPARERX/PREPARETX task to ready to receive/ transmit | | 1.5 | | µs |

## 33.10.2 TWIS slave timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWIS,SU\_DAT}$ | Data setup time before positive edge on SCL – all modes | 300 | | | ns |
| $t_{TWIS,HD\_DAT}$ | Data hold time after negative edge on SCL – all modes | 500 | | | ns |
| $t_{TWIS,HD\_STA,100kbps}$ | TWI slave hold time from for START condition (SDA low to SCL low), 100 kbps | 5200 | | | ns |

[28] High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWIS,HD\_STA,400kbps}$ | TWI slave hold time from for START condition (SDA low to SCL low), 400 kbps | 1300 | | | ns |
| $t_{TWIS,SU\_STO,100kbps}$ | TWI slave setup time from SCL high to STOP condition, 100 kbps | 5200 | | | ns |
| $t_{TWIS,SU\_STO,400kbps}$ | TWI slave setup time from SCL high to STOP condition, 400 kbps | 1300 | | | ns |
| $t_{TWIS,BUF,100kbps}$ | TWI slave bus free time between STOP and START conditions, 100 kbps | | 4700 | | ns |
| $t_{TWIS,BUF,400kbps}$ | TWI slave bus free time between STOP and START conditions, 400 kbps | | 1300 | | ns |

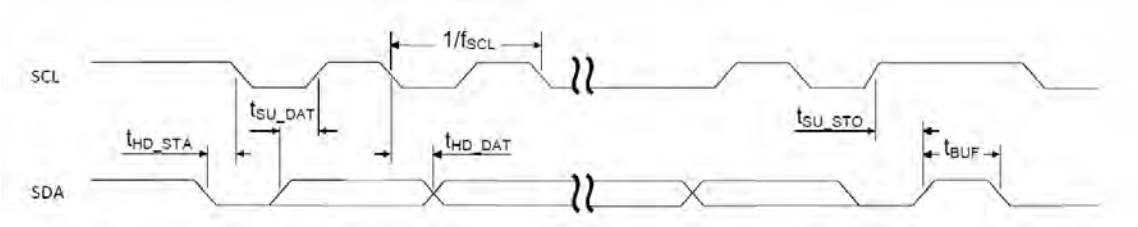



**Figure 101: TWIS timing diagram, 1 byte transaction**

# 34 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- Automatic hardware flow control
- Optional even parity bit checking and generation
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- One or two stop bit
- Least significant bit (LSB) first

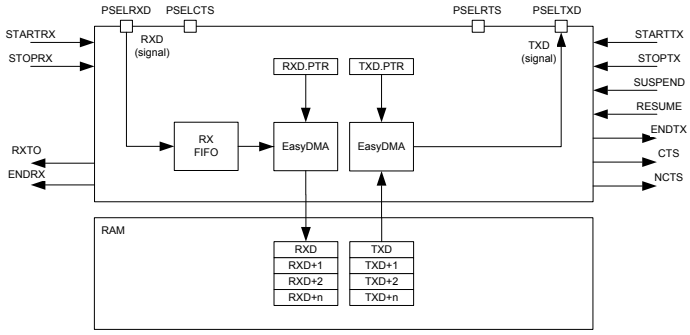



**Figure 102: UARTE configuration**

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

## 34.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

## 34.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

## 34.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled through the HWFC field in the CONFIG register, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 103: UARTE transmission* on page 395. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

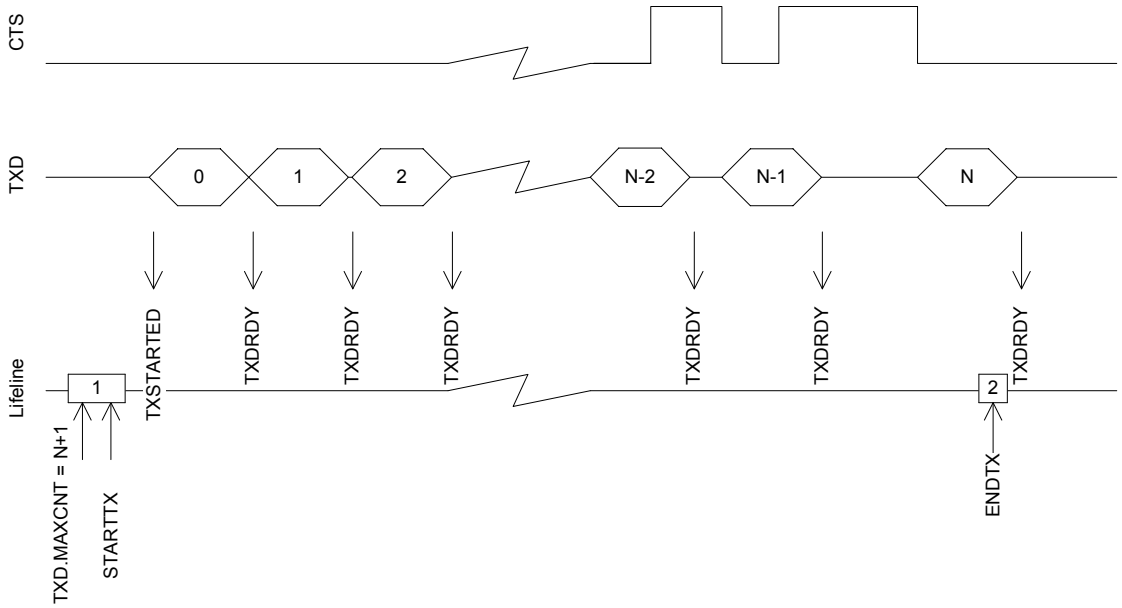



**Figure 103: UARTE transmission**

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER — Power supply* on page 66 for more information about power modes.

## 34.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.

The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 104: UARTE reception* on page 396.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

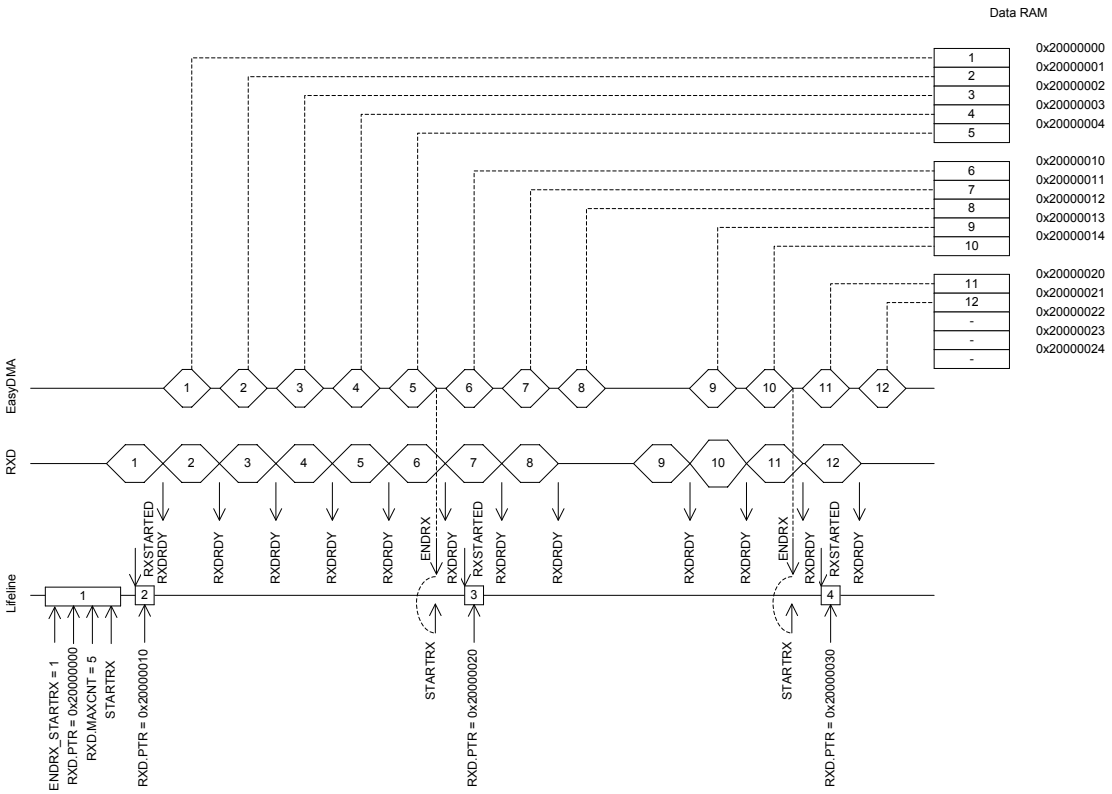



**Figure 104: UARTE reception**

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

> **Important:** If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered.

To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 105: UARTE reception with forced stop via STOPRX* on page 397. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

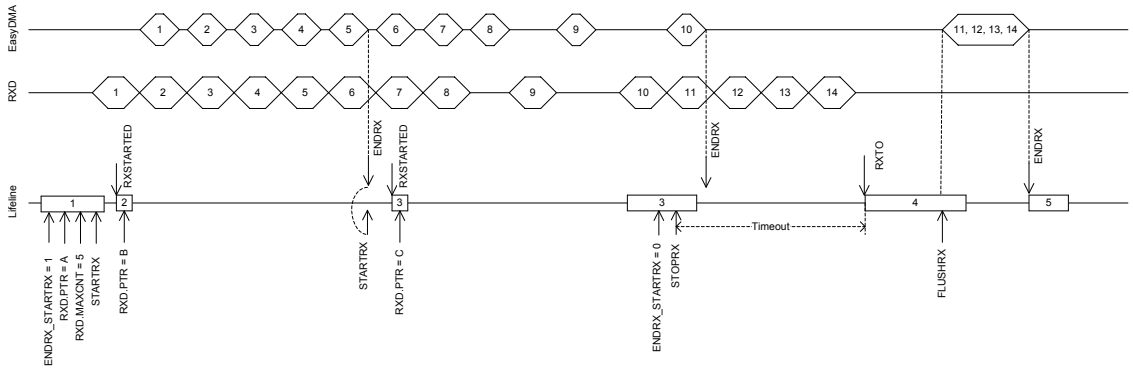



**Figure 105: UARTE reception with forced stop via STOPRX**

If HW flow control is enabled through the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER — Power supply* on page 66 for more information about power modes.

## 34.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

## 34.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

## 34.7 Parity and stop bit configuration

When parity is enabled through the PARITY field in the CONFIG register, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

The amount of stop bits can be configured through the STOP field in the CONFIG register.

## 34.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

## 34.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 73: GPIO configuration before enabling peripheral* on page 398.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

### Table 73: GPIO configuration before enabling peripheral

| UARTE signal | UARTE pin | Direction | Output value |
|---|---|---|---|
| RXD | As specified in PSEL.RXD | Input | Not applicable |
| CTS | As specified in PSEL.CTS | Input | Not applicable |
| RTS | As specified in PSEL.RTS | Output | 1 |
| TXD | As specified in PSEL.TXD | Output | 1 |

## 34.10 Registers

### Table 74: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40002000 | UARTE | UARTE0 | Universal asynchronous receiver/ transmitter with EasyDMA, unit 0 | |
| 0x40028000 | UARTE | UARTE1 | Universal asynchronous receiver/ transmitter with EasyDMA, unit 1 | |

### Table 75: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTRX | 0x000 | Start UART receiver |
| TASKS_STOPRX | 0x004 | Stop UART receiver |
| TASKS_STARTTX | 0x008 | Start UART transmitter |
| TASKS_STOPTX | 0x00C | Stop UART transmitter |
| TASKS_FLUSHRX | 0x02C | Flush RX FIFO into RX buffer |
| EVENTS_CTS | 0x100 | CTS is activated (set low). Clear To Send. |
| EVENTS_NCTS | 0x104 | CTS is deactivated (set high). Not Clear To Send. |
| EVENTS_RXDRDY | 0x108 | Data received in RXD (but potentially not yet transferred to Data RAM) |
| EVENTS_ENDRX | 0x110 | Receive buffer is filled up |
| EVENTS_TXDRDY | 0x11C | Data sent from TXD |
| EVENTS_ENDTX | 0x120 | Last TX byte transmitted |
| EVENTS_ERROR | 0x124 | Error detected |
| EVENTS_RXTO | 0x144 | Receiver timeout |

| Register | Offset | Description |
|---|---|---|
| EVENTS_RXSTARTED | 0x14C | UART receiver has started |
| EVENTS_TXSTARTED | 0x150 | UART transmitter has started |
| EVENTS_TXSTOPPED | 0x158 | Transmitter stopped |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSRC* | 0x480 | Error source<br><br>Note : this register is read / write one to clear. |
| *ENABLE* | 0x500 | Enable UART |
| *PSEL.RTS* | 0x508 | Pin select for RTS signal |
| *PSEL.TXD* | 0x50C | Pin select for TXD signal |
| *PSEL.CTS* | 0x510 | Pin select for CTS signal |
| *PSEL.RXD* | 0x514 | Pin select for RXD signal |
| *BAUDRATE* | 0x524 | Baud rate. Accuracy depends on the HFCLK source selected. |
| *RXD.PTR* | 0x534 | Data pointer |
| *RXD.MAXCNT* | 0x538 | Maximum number of bytes in receive buffer |
| *RXD.AMOUNT* | 0x53C | Number of bytes transferred in the last transaction |
| *TXD.PTR* | 0x544 | Data pointer |
| *TXD.MAXCNT* | 0x548 | Maximum number of bytes in transmit buffer |
| *TXD.AMOUNT* | 0x54C | Number of bytes transferred in the last transaction |
| *CONFIG* | 0x56C | Configuration of parity and hardware flow control |

## 34.10.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | | | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ENDRX_STARTRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDRX* and *TASKS_STARTRX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ENDRX_STOPRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDRX* and *TASKS_STOPRX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CTS* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NCTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_NCTS* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| C | RW | RXDRDY | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for RXDRDY event<br><br>See *EVENTS_RXDRDY* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| D | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for ENDRX event<br><br>See *EVENTS_ENDRX* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| E | RW | TXDRDY | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for TXDRDY event<br><br>See *EVENTS_TXDRDY* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| F | RW | ENDTX | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for ENDTX event<br><br>See *EVENTS_ENDTX* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| G | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for ERROR event<br><br>See *EVENTS_ERROR* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| H | RW | RXTO | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for RXTO event<br><br>See *EVENTS_RXTO* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| I | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for RXSTARTED event<br><br>See *EVENTS_RXSTARTED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| J | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for TXSTARTED event<br><br>See *EVENTS_TXSTARTED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |
| L | RW | TXSTOPPED | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for TXSTOPPED event<br><br>See *EVENTS_TXSTOPPED* | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |

## 34.10.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | CTS | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for CTS event<br><br>See *EVENTS_CTS* | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NCTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_NCTS* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXDRDY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDRX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXDRDY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | ENDTX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDTX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ERROR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RXTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXTO* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | TXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | TXSTOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXSTOPPED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |

## 34.10.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | CTS | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for CTS event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_CTS* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| B | RW | NCTS | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for NCTS event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_NCTS* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| C | RW | RXDRDY | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for RXDRDY event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_RXDRDY* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| D | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ENDRX event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDRX* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| E | RW | TXDRDY | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for TXDRDY event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_TXDRDY* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| F | RW | ENDTX | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ENDTX event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ENDTX* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| G | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for ERROR event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_ERROR* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| H | RW | RXTO | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for RXTO event | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_RXTO* | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | | | |
| I | RW | RXSTARTED | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for RXSTARTED event | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | L | | J | I | | H | | | | | | | | G | F | E | | | D | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_RXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | TXSTARTED | | | | | | | | | | Write '1' to Disable interrupt for TXSTARTED event<br>See *EVENTS_TXSTARTED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | TXSTOPPED | | | | | | | | | | Write '1' to Disable interrupt for TXSTOPPED event<br>See *EVENTS_TXSTOPPED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.5 ERRORSRC

Address offset: 0x480

Error source

Note : this register is read / write one to clear.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OVERRUN | | | | | | | | | | Overrun error<br>A start bit is received while the previous data still lies in RXD. (Previous data is lost.) | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | Read: error not present | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | Read: error present | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PARITY | | | | | | | | | | Parity error<br>A character with bad parity is received, if HW parity check is enabled. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | Read: error not present | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | Read: error present | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | FRAMING | | | | | | | | | | Framing error occurred<br>A valid stop bit is not detected on the serial data input after all bits in a character have been received. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | Read: error not present | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | Read: error present | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | BREAK | | | | | | | | | | Break condition<br>The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.). | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | Read: error not present | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | Read: error present | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.6 ENABLE

Address offset: 0x500

Enable UART

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.8 PSEL.TXD

Address offset: 0x50C

Pin select for TXD signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.11 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x04000000** | | | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BAUDRATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud1200 | 0x0004F000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud2400 | 0x0009D000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud4800 | 0x0013B000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud9600 | 0x00275000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud14400 | 0x003AF000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud19200 | 0x004EA000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud28800 | 0x0075C000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud31250 | 0x00800000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud38400 | 0x009D0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud56000 | 0x00E50000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud57600 | 0x00EB0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud76800 | 0x013A9000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud115200 | 0x01D60000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud230400 | 0x03B00000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud250000 | 0x04000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud460800 | 0x07400000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud921600 | 0x0F000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Baud1M | 0x10000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.12 RXD.PTR

Address offset: 0x534

Data pointer

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 34.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in receive buffer |

## 34.10.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 34.10.15 TXD.PTR

Address offset: 0x544

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer |

## 34.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes in transmit buffer |

## 34.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 34.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | B | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | HWFC | | | Hardware flow control |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | B | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Excluded | 0x0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Included | 0x7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | One | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Two | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 34.11 Electrical specification

## 34.11.1 UARTE electrical specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{UARTE}$ | Baud rate for UARTE[29]. | | | 1000 | kbps |
| $I_{UARTE1M}$ | Run current at max baud rate. | | 55 | | µA |
| $I_{UARTE115k}$ | Run current at 115200 bps. | | 55 | | µA |
| $I_{UARTE1k2}$ | Run current at 1200 bps. | | 55 | | µA |
| $I_{UARTE,IDLE}$ | Idle current for UARTE (STARTed, no XXX activity) | | 1 | | µA |
| $t_{UARTE,CTSH}$ | CTS high time | 1 | | | µs |
| $t_{UARTE,START}$ | Time from STARTRX/STARTTX task to transmission started | | 1 | | µs |

[29] High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

# 35 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

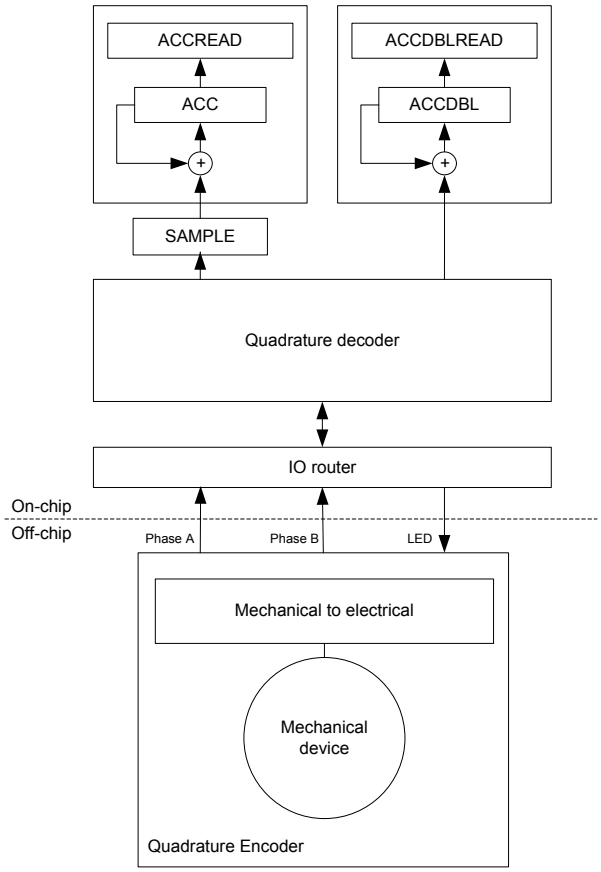



**Figure 106: Quadrature decoder configuration**

## 35.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.

The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

**Table 76: Sampled value encoding**

| Previous sample pair(n - 1) | | Current samples pair(n) | | SAMPLE register | ACC operation | ACCDBL operation | Description |
|---|---|---|---|---|---|---|---|
| A | B | A | B | | | | |
| 0 | 0 | 0 | 0 | 0 | No change | No change | No movement |
| 0 | 0 | 0 | 1 | 1 | Increment | No change | Movement in positive direction |
| 0 | 0 | 1 | 0 | -1 | Decrement | No change | Movement in negative direction |
| 0 | 0 | 1 | 1 | 2 | No change | Increment | Error: Double transition |
| 0 | 1 | 0 | 0 | -1 | Decrement | No change | Movement in negative direction |
| 0 | 1 | 0 | 1 | 0 | No change | No change | No movement |
| 0 | 1 | 1 | 0 | 2 | No change | Increment | Error: Double transition |
| 0 | 1 | 1 | 1 | 1 | Increment | No change | Movement in positive direction |
| 1 | 0 | 0 | 0 | 1 | Increment | No change | Movement in positive direction |
| 1 | 0 | 0 | 1 | 2 | No change | Increment | Error: Double transition |
| 1 | 0 | 1 | 0 | 0 | No change | No change | No movement |
| 1 | 0 | 1 | 1 | -1 | Decrement | No change | Movement in negative direction |
| 1 | 1 | 0 | 0 | 2 | No change | Increment | Error: Double transition |
| 1 | 1 | 0 | 1 | -1 | Decrement | No change | Movement in negative direction |
| 1 | 1 | 1 | 0 | 1 | Increment | No change | Movement in positive direction |
| 1 | 1 | 1 | 1 | 0 | No change | No change | No movement |

## 35.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

## 35.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.

Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

## 35.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

## 35.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

## 35.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in

ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 77: GPIO configuration before enabling peripheral* on page 411 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

### Table 77: GPIO configuration before enabling peripheral

| QDEC signal | QDEC pin | Direction | Output value | Comment |
|---|---|---|---|---|
| Phase A | As specified in PSEL.A | Input | Not applicable | |
| Phase B | As specified in PSEL.B | Input | Not applicable | |
| LED | As specified in PSEL.LED | Input | Not applicable | |

## 35.7 Registers

### Table 78: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40012000 | QDEC | QDEC | Quadrature decoder | |

### Table 79: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Task starting the quadrature decoder |
| TASKS_STOP | 0x004 | Task stopping the quadrature decoder |
| TASKS_READCLRACC | 0x008 | Read and clear ACC and ACCDBL |
| TASKS_RDCLRACC | 0x00C | Read and clear ACC |
| TASKS_RDCLRDBL | 0x010 | Read and clear ACCDBL |
| EVENTS_SAMPLERDY | 0x100 | Event being generated for every new sample value written to the SAMPLE register |
| EVENTS_REPORTRDY | 0x104 | Non-null report ready |
| EVENTS_ACCOF | 0x108 | ACC or ACCDBL register overflow |
| EVENTS_DBLRDY | 0x10C | Double displacement(s) detected |
| EVENTS_STOPPED | 0x110 | QDEC has been stopped |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | Enable the quadrature decoder |
| *LEDPOL* | 0x504 | LED output pin polarity |
| *SAMPLEPER* | 0x508 | Sample period |
| *SAMPLE* | 0x50C | Motion sample value |
| *REPORTPER* | 0x510 | Number of samples to be taken before REPORTRDY and DBLRDY events can be generated |
| *ACC* | 0x514 | Register accumulating the valid transitions |
| *ACCREAD* | 0x518 | Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task |
| *PSEL.LED* | 0x51C | Pin select for LED signal |
| *PSEL.A* | 0x520 | Pin select for A signal |
| *PSEL.B* | 0x524 | Pin select for B signal |
| *DBFEN* | 0x528 | Enable input debounce filters |
| *LEDPRE* | 0x540 | Time period the LED is switched ON prior to sampling |
| *ACCDBL* | 0x544 | Register accumulating the number of detected double transitions |
| *ACCDBLREAD* | 0x548 | Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task |

### 35.7.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | REPORTRDY_READCLRACC | | | Shortcut between REPORTRDY event and READCLRACC task<br><br>See *EVENTS_REPORTRDY* and *TASKS_READCLRACC* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | SAMPLERDY_STOP | | | Shortcut between SAMPLERDY event and STOP task<br><br>See *EVENTS_SAMPLERDY* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| C | RW | REPORTRDY_RDCLRACC | | | Shortcut between REPORTRDY event and RDCLRACC task<br><br>See *EVENTS_REPORTRDY* and *TASKS_RDCLRACC* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| D | RW | REPORTRDY_STOP | | | Shortcut between REPORTRDY event and STOP task<br><br>See *EVENTS_REPORTRDY* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| E | RW | DBLRDY_RDCLRDBL | | | Shortcut between DBLRDY event and RDCLRDBL task<br><br>See *EVENTS_DBLRDY* and *TASKS_RDCLRDBL* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| F | RW | DBLRDY_STOP | | | Shortcut between DBLRDY event and STOP task<br><br>See *EVENTS_DBLRDY* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| G | RW | SAMPLERDY_READCLRACC | | | Shortcut between SAMPLERDY event and READCLRACC task<br><br>See *EVENTS_SAMPLERDY* and *TASKS_READCLRACC* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 35.7.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SAMPLERDY | | | Write '1' to Enable interrupt for SAMPLERDY event<br><br>See *EVENTS_SAMPLERDY* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | REPORTRDY | | | Write '1' to Enable interrupt for REPORTRDY event<br><br>See *EVENTS_REPORTRDY* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | ACCOF | | | Write '1' to Enable interrupt for ACCOF event<br><br>See *EVENTS_ACCOF* |
| | | | Set | 1 | Enable |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DBLRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SAMPLERDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | REPORTRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ACCOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DBLRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.5 LEDPOL

Address offset: 0x504

LED output pin polarity

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LEDPOL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveLow | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveHigh | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.6 SAMPLEPER

Address offset: 0x508

Sample period

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SAMPLEPER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 128us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 256us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 512us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1024us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2048us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4096us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 8192us | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 16384us | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 32ms | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 65ms | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 131ms | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.7 SAMPLE

Address offset: 0x50C

Motion sample value

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | SAMPLE | | [-1..2] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | REPORTPER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Specifies the number of samples to be accumulated in the ACC register before the REPORTRDY and DBLRDY events can be generated<br><br>The report period in [us] is given as: RPUS = SP * RP Where RPUS is the report period in [us/report], SP is the sample period in [us/sample] specified in SAMPLEPER, and RP is the report period in [samples/report] specified in REPORTPER . | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10Smpl | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 10 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40Smpl | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 40 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 80Smpl | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 80 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 120Smpl | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 120 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 160Smpl | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 160 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 200Smpl | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 200 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 240Smpl | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 240 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 280Smpl | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 280 samples / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1Smpl | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1 sample / report | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ACC | | [-1024..1023] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Register accumulating all valid samples (not double transition) read from the SAMPLE register<br><br>Double transitions ( SAMPLE = 2 ) will not be accumulated in this register. The value is a 32 bit 2's complement value. If a sample that would cause this register to overflow or underflow is received, the sample will be ignored and an overflow event ( ACCOF ) will be generated. The ACC register is cleared by triggering the READCLRACC or the RDCLRACC task. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ACCREAD | | [-1024..1023] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Snapshot of the ACC register.<br>The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.11 PSEL.LED

Address offset: 0x51C

Pin select for LED signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.12 PSEL.A

Address offset: 0x520

Pin select for A signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.13 PSEL.B

Address offset: 0x524

Pin select for B signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 35.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | DBFEN | | | Enable input debounce filters |
| | | | Disabled | 0 | Debounce input filters disabled |
| | | | Enabled | 1 | Debounce input filters enabled |

## 35.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000010** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | LEDPRE | | [1..511] | Period in us the LED is switched on prior to sampling |

## 35.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | ACCDBL | | [0..15] | Register accumulating the number of detected double or illegal transitions. ( SAMPLE = 2 ).<br><br>When this register has reached its maximum value the accumulation of double / illegal transitions will stop. An overflow event ( ACCOF ) will be generated if any double or illegal transitions are detected after the maximum value was reached. This field is cleared by triggering the READCLRACC or RDCLRDBL task. |

## 35.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | ACCDBLREAD | | [0..15] | Snapshot of the ACCDBL register. This field is updated when the READCLRACC or RDCLRDBL task is triggered. |

# 35.8 Electrical specification

## 35.8.1 QDEC Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{QDEC}$ | Run current | | 5 | | µA |
| $t_{SAMPLE}$ | Time between sampling signals from quadrature decoder | 128 | | 131072 | µs |
| $t_{LED}$ | Time from LED is turned on to signals are sampled | 0 | | 511 | µs |

# 36 SAADC — Successive approximation analog-to-digital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
  - One channel per single-ended input and two channels per differential input
  - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is $t_{ack} + t_{conv}$ which may vary between channels according to user configuration of $t_{ack}$.
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2’s complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- Internal resistor string
- Limit checking on the fly

## 36.1 Shared resources

The ADC can coexist with COMP, LPCOMP and other peripherals using one of `AIN0-AIN7`, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

## 36.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select the `AIN0` to `AIN7` pins, the `VDD` pin, or the `VDDH` pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.

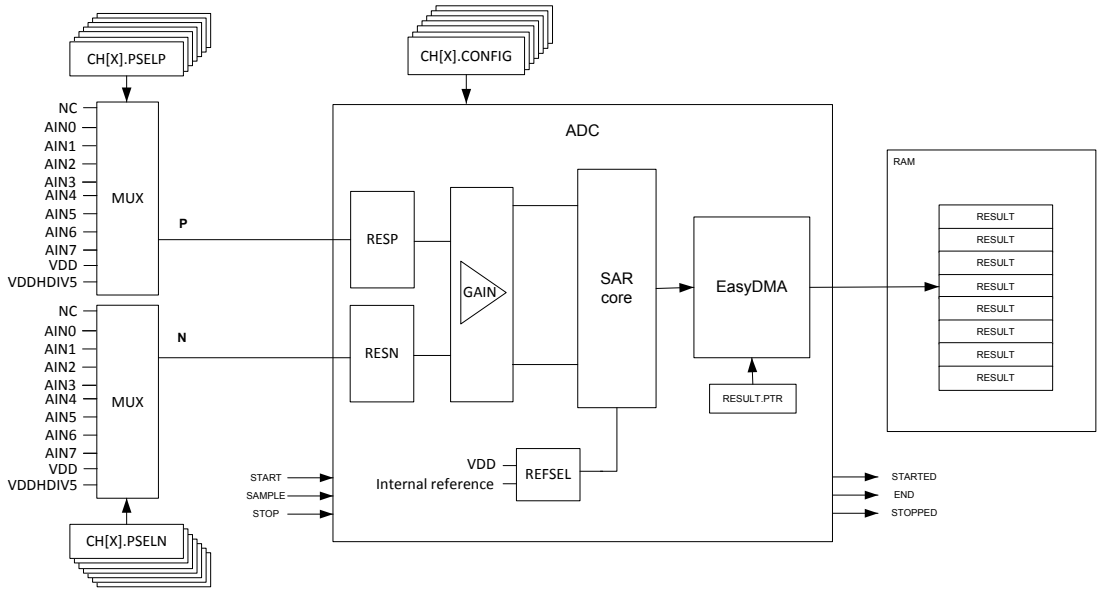



**Figure 107: Simplified ADC block diagram**

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

## 36.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

$$RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2^{(RESOLUTION - m)}$$

where

**V(P)**
: is the voltage at input P

**V(N)**
: is the voltage at input N

**GAIN**
: is the selected gain setting

**REFERENCE**
: is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.

The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ±0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete. Since calibration involves acquiring a sample, a DONE and a RESULTDONE event will be fired as well.

## 36.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See *Shared resources* on page 418 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

> **Important:** Channels selected for either COMP or LPCOMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

## 36.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

### 36.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 422.

### 36.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

$$f_{SAMPLE} < 1/[t_{ACQ} + t_{conv}]$$

The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

### 36.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set $2^{OVERSAMPLE}$ number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE $2^{OVERSAMPLE}$ times from software
- Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{OVERSAMPLE}$ times. With BURST = 1 the ADC will sample the input $2^{OVERSAMPLE}$ times as fast as it can (actual timing: $<(t_{ACQ}+t_{CONV})\times 2^{OVERSAMPLE}$). Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

### 36.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

$$\text{Total time} < \text{Sum}(CH[x].t_{ACQ}+t_{CONV}),\ x=0..\text{enabled channels}$$

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

*Figure 108: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled* on page 422 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.

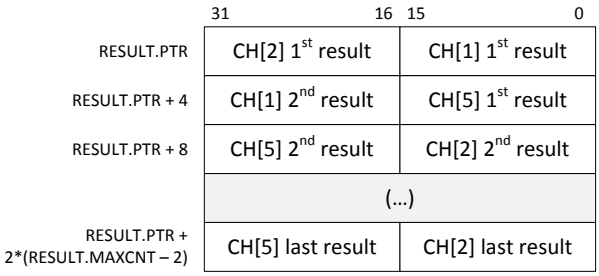



**Figure 108: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled**

*Figure 109: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled* on page 422 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

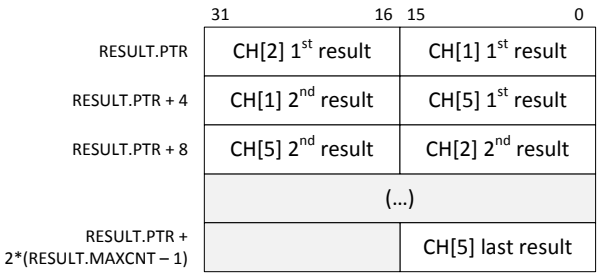



**Figure 109: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled**

## 36.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 110: ADC* on page 423. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.

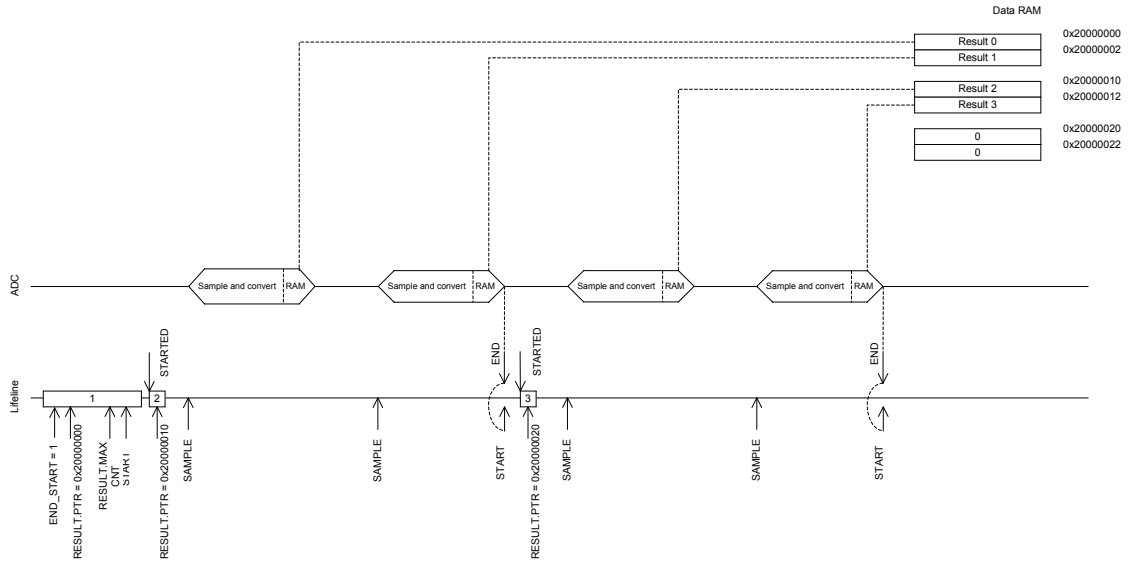



**Figure 110: ADC**

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 421 for more information about Scan mode.

## 36.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See *Figure 111: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)* on page 424. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.

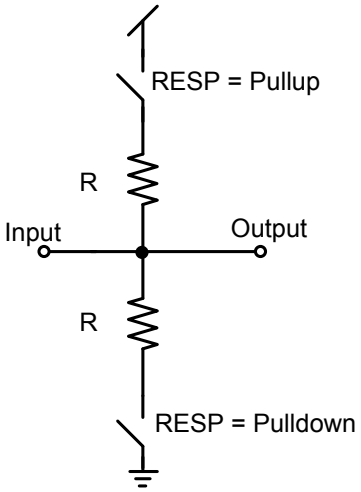



**Figure 111: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)**

## 36.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- Internal reference
- VDD as reference

The internal reference results in an input range of ±0.6 V on the ADC core. VDD as reference results in an input range of ±VDD/4 on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 V or +-VDD/4)/Gain
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 V)/(1/6) = 3.6 V
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

## 36.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 112: Simplified ADC sample network* on page 425. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source ($R_{source}$) resistance. For high source resistance the acquisition time should be increased, see *Table 80: Acquisition time* on page 425.

When using `VDDHDIV5` as input, the acquisition time needs to be 10 µs or higher.

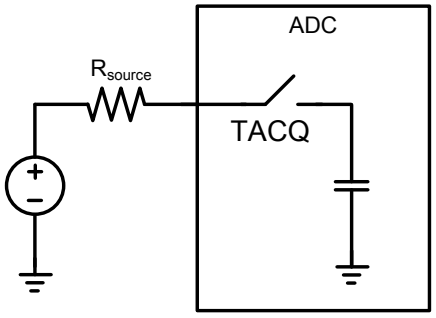



**Figure 112: Simplified ADC sample network**

**Table 80: Acquisition time**

| TACQ [µs] | Maximum source resistance [kOhm] |
|---|---|
| 3 | 10 |
| 5 | 40 |
| 10 | 100 |
| 15 | 200 |
| 20 | 400 |
| 40 | 800 |

## 36.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

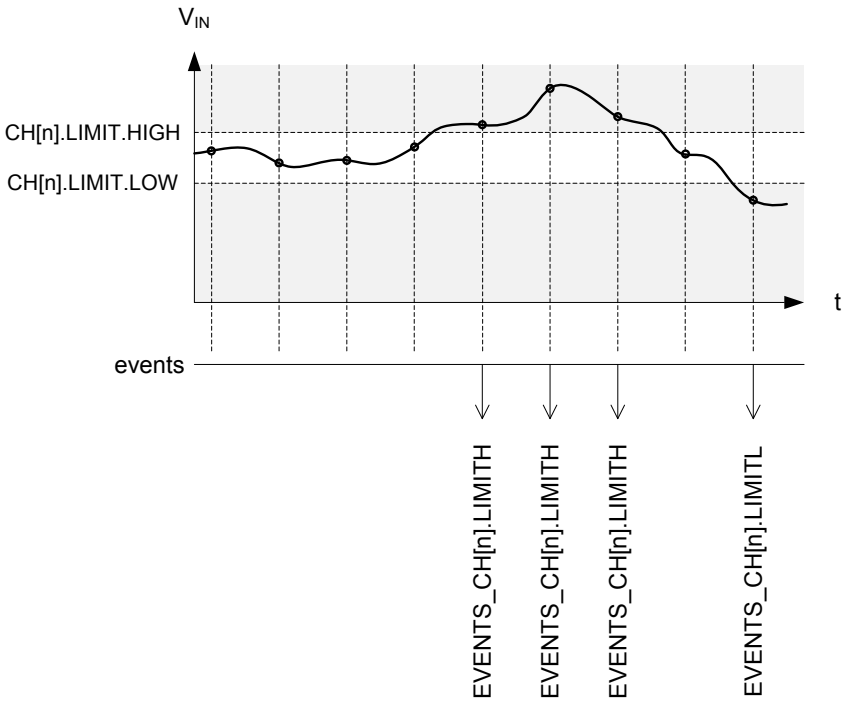



**Figure 113: Example of limits monitoring on channel 'n'**

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled

outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

## 36.11 Registers

### Table 81: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40007000 | SAADC | SAADC | Analog to digital converter | |

### Table 82: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start the ADC and prepare the result buffer in RAM |
| TASKS_SAMPLE | 0x004 | Take one ADC sample, if scan is enabled all channels are sampled |
| TASKS_STOP | 0x008 | Stop the ADC and terminate any on-going conversion |
| TASKS_CALIBRATEOFFSE | 0x00C | Starts offset auto-calibration |
| EVENTS_STARTED | 0x100 | The ADC has started |
| EVENTS_END | 0x104 | The ADC has filled up the Result buffer |
| EVENTS_DONE | 0x108 | A conversion task has been completed. Depending on the mode, multiple conversions might be needed for a result to be transferred to RAM. |
| EVENTS_RESULTDONE | 0x10C | A result is ready to get transferred to RAM. |
| EVENTS_CALIBRATEDON | 0x110 | Calibration is complete |
| EVENTS_STOPPED | 0x114 | The ADC has stopped |
| EVENTS_CH[0].LIMITH | 0x118 | Last results is equal or above CH[0].LIMIT.HIGH |
| EVENTS_CH[0].LIMITL | 0x11C | Last results is equal or below CH[0].LIMIT.LOW |
| EVENTS_CH[1].LIMITH | 0x120 | Last results is equal or above CH[1].LIMIT.HIGH |
| EVENTS_CH[1].LIMITL | 0x124 | Last results is equal or below CH[1].LIMIT.LOW |
| EVENTS_CH[2].LIMITH | 0x128 | Last results is equal or above CH[2].LIMIT.HIGH |
| EVENTS_CH[2].LIMITL | 0x12C | Last results is equal or below CH[2].LIMIT.LOW |
| EVENTS_CH[3].LIMITH | 0x130 | Last results is equal or above CH[3].LIMIT.HIGH |
| EVENTS_CH[3].LIMITL | 0x134 | Last results is equal or below CH[3].LIMIT.LOW |
| EVENTS_CH[4].LIMITH | 0x138 | Last results is equal or above CH[4].LIMIT.HIGH |
| EVENTS_CH[4].LIMITL | 0x13C | Last results is equal or below CH[4].LIMIT.LOW |
| EVENTS_CH[5].LIMITH | 0x140 | Last results is equal or above CH[5].LIMIT.HIGH |
| EVENTS_CH[5].LIMITL | 0x144 | Last results is equal or below CH[5].LIMIT.LOW |
| EVENTS_CH[6].LIMITH | 0x148 | Last results is equal or above CH[6].LIMIT.HIGH |
| EVENTS_CH[6].LIMITL | 0x14C | Last results is equal or below CH[6].LIMIT.LOW |
| EVENTS_CH[7].LIMITH | 0x150 | Last results is equal or above CH[7].LIMIT.HIGH |
| EVENTS_CH[7].LIMITL | 0x154 | Last results is equal or below CH[7].LIMIT.LOW |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *STATUS* | 0x400 | Status |
| *ENABLE* | 0x500 | Enable or disable ADC |
| *CH[0].PSELP* | 0x510 | Input positive pin selection for CH[0] |
| *CH[0].PSELN* | 0x514 | Input negative pin selection for CH[0] |
| *CH[0].CONFIG* | 0x518 | Input configuration for CH[0] |
| *CH[0].LIMIT* | 0x51C | High/low limits for event monitoring a channel |
| *CH[1].PSELP* | 0x520 | Input positive pin selection for CH[1] |
| *CH[1].PSELN* | 0x524 | Input negative pin selection for CH[1] |
| *CH[1].CONFIG* | 0x528 | Input configuration for CH[1] |
| *CH[1].LIMIT* | 0x52C | High/low limits for event monitoring a channel |
| *CH[2].PSELP* | 0x530 | Input positive pin selection for CH[2] |

| Register | Offset | Description |
|---|---|---|
| *CH[2].PSELN* | 0x534 | Input negative pin selection for CH[2] |
| *CH[2].CONFIG* | 0x538 | Input configuration for CH[2] |
| *CH[2].LIMIT* | 0x53C | High/low limits for event monitoring a channel |
| *CH[3].PSELP* | 0x540 | Input positive pin selection for CH[3] |
| *CH[3].PSELN* | 0x544 | Input negative pin selection for CH[3] |
| *CH[3].CONFIG* | 0x548 | Input configuration for CH[3] |
| *CH[3].LIMIT* | 0x54C | High/low limits for event monitoring a channel |
| *CH[4].PSELP* | 0x550 | Input positive pin selection for CH[4] |
| *CH[4].PSELN* | 0x554 | Input negative pin selection for CH[4] |
| *CH[4].CONFIG* | 0x558 | Input configuration for CH[4] |
| *CH[4].LIMIT* | 0x55C | High/low limits for event monitoring a channel |
| *CH[5].PSELP* | 0x560 | Input positive pin selection for CH[5] |
| *CH[5].PSELN* | 0x564 | Input negative pin selection for CH[5] |
| *CH[5].CONFIG* | 0x568 | Input configuration for CH[5] |
| *CH[5].LIMIT* | 0x56C | High/low limits for event monitoring a channel |
| *CH[6].PSELP* | 0x570 | Input positive pin selection for CH[6] |
| *CH[6].PSELN* | 0x574 | Input negative pin selection for CH[6] |
| *CH[6].CONFIG* | 0x578 | Input configuration for CH[6] |
| *CH[6].LIMIT* | 0x57C | High/low limits for event monitoring a channel |
| *CH[7].PSELP* | 0x580 | Input positive pin selection for CH[7] |
| *CH[7].PSELN* | 0x584 | Input negative pin selection for CH[7] |
| *CH[7].CONFIG* | 0x588 | Input configuration for CH[7] |
| *CH[7].LIMIT* | 0x58C | High/low limits for event monitoring a channel |
| *RESOLUTION* | 0x5F0 | Resolution configuration |
| *OVERSAMPLE* | 0x5F4 | Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used. |
| *SAMPLERATE* | 0x5F8 | Controls normal or continuous sample rate |
| *RESULT.PTR* | 0x62C | Data pointer |
| *RESULT.MAXCNT* | 0x630 | Maximum number of buffer words to transfer |
| *RESULT.AMOUNT* | 0x634 | Number of buffer words transferred since last START |

## 36.11.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RESULTDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CALIBRATEDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH0LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH0LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH1LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH1LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH2LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH2LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH3LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH3LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH4LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | CH4LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH5LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH5LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[5].LIMITL* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | CH6LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[6].LIMITH* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH6LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[6].LIMITL* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH7LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[7].LIMITH* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | CH7LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | See *EVENTS_CH[7].LIMITL* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_END* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | See *EVENTS_DONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RESULTDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | See *EVENTS_RESULTDONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CALIBRATEDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH0LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH0LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH1LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH1LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH2LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH2LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | CH3LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | CH3LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH4LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | | | See *EVENTS_CH[4].LIMITH* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| P | RW | CH4LIMITL | | | Write '1' to Enable interrupt for CH[4].LIMITL event |
| | | | | | See *EVENTS_CH[4].LIMITL* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| Q | RW | CH5LIMITH | | | Write '1' to Enable interrupt for CH[5].LIMITH event |
| | | | | | See *EVENTS_CH[5].LIMITH* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| R | RW | CH5LIMITL | | | Write '1' to Enable interrupt for CH[5].LIMITL event |
| | | | | | See *EVENTS_CH[5].LIMITL* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| S | RW | CH6LIMITH | | | Write '1' to Enable interrupt for CH[6].LIMITH event |
| | | | | | See *EVENTS_CH[6].LIMITH* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| T | RW | CH6LIMITL | | | Write '1' to Enable interrupt for CH[6].LIMITL event |
| | | | | | See *EVENTS_CH[6].LIMITL* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| U | RW | CH7LIMITH | | | Write '1' to Enable interrupt for CH[7].LIMITH event |
| | | | | | See *EVENTS_CH[7].LIMITH* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| V | RW | CH7LIMITL | | | Write '1' to Enable interrupt for CH[7].LIMITL event |
| | | | | | See *EVENTS_CH[7].LIMITL* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 36.11.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | STARTED | | | Write '1' to Disable interrupt for STARTED event |
| | | | | | See *EVENTS_STARTED* |
| | | | Clear | 1 | Disable |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_END* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_DONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RESULTDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RESULTDONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CALIBRATEDONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CALIBRATEDONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STOPPED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | CH0LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[0].LIMITH* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | CH0LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[0].LIMITL* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | CH1LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[1].LIMITH* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | CH1LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[1].LIMITL* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | CH2LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CH[2].LIMITH* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | CH2LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | CH4LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | CH5LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | CH5LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | CH6LIMITL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | CH7LIMITH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| V | RW | CH7LIMITL | | | Write '1' to Disable interrupt for CH[7].LIMITL event<br><br>See *EVENTS_CH[7].LIMITL* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 36.11.4 STATUS

Address offset: 0x400

Status

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | STATUS | | | Status |
| | | | Ready | 0 | ADC is ready. No on-going conversion. |
| | | | Busy | 1 | ADC is busy. Conversion in progress. |

## 36.11.5 ENABLE

Address offset: 0x500

Enable or disable ADC

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENABLE | | | Enable or disable ADC |
| | | | Disabled | 0 | Disable ADC |
| | | | Enabled | 1 | Enable ADC<br><br>When enabled, the ADC will acquire access to the analog input pins specified in the CH[n].PSELP and CH[n].PSELN registers. |

## 36.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PSELP | | | Analog positive input channel |
| | | | NC | 0 | Not connected |
| | | | AnalogInput0 | 1 | AIN0 |
| | | | AnalogInput1 | 2 | AIN1 |
| | | | AnalogInput2 | 3 | AIN2 |
| | | | AnalogInput3 | 4 | AIN3 |
| | | | AnalogInput4 | 5 | AIN4 |
| | | | AnalogInput5 | 6 | AIN5 |
| | | | AnalogInput6 | 7 | AIN6 |
| | | | AnalogInput7 | 8 | AIN7 |
| | | | VDD | 9 | VDD |
| | | | VDDHDIV5 | 0x0D | VDDH/5 |

## 36.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | | | | | | | | 4 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | | | | | | | | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | | | | | | | | 6 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | | | | | | | | 7 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | | | | | | | | 8 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | | | | | | | | 9 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | | | | | | | | 0x0D | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | | | | | | | | 4 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | | | | | | | | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | | | | | | | | 6 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | | | | | | | | 7 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | | | | | | | | 8 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | | | | | | | | 9 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | | | | | | | | 0x0D | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pulldown | | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pullup | | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_2 | | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Gain control |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/6 |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/5 |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/4 |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/3 |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/2 |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 2 |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 4 |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reference control |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Internal reference (0.6 V) |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | VDD/4 as reference |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Acquisition time, the time the ADC uses to sample the input voltage |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3 us |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 5 us |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 10 us |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 15 us |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 20 us |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 40 us |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable differential mode |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Single ended, PSELN will be ignored, negative input to ADC shorted to GND |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Differential |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable burst mode |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Burst mode is disabled (normal operation) |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of samples as fast as it can, and sends the average to Data RAM. |

## 36.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Low level limit |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | High level limit |

## 36.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Analog positive input channel |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Not connected |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN0 |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN1 |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN2 |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| | | | AnalogInput3 | | | | | | | 4 | | | | | | | | | | | | | | | | | | | | | | | | AIN3 |
| | | | AnalogInput4 | | | | | | | 5 | | | | | | | | | | | | | | | | | | | | | | | | AIN4 |
| | | | AnalogInput5 | | | | | | | 6 | | | | | | | | | | | | | | | | | | | | | | | | AIN5 |
| | | | AnalogInput6 | | | | | | | 7 | | | | | | | | | | | | | | | | | | | | | | | | AIN6 |
| | | | AnalogInput7 | | | | | | | 8 | | | | | | | | | | | | | | | | | | | | | | | | AIN7 |
| | | | VDD | | | | | | | 9 | | | | | | | | | | | | | | | | | | | | | | | | VDD |
| | | | VDDHDIV5 | | | | | | | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | VDDH/5 |

## 36.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Analog negative input, enables differential channel |
| | | | NC | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | Not connected |
| | | | AnalogInput0 | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | AIN0 |
| | | | AnalogInput1 | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | | AIN1 |
| | | | AnalogInput2 | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | | AIN2 |
| | | | AnalogInput3 | | | | | | | 4 | | | | | | | | | | | | | | | | | | | | | | | | AIN3 |
| | | | AnalogInput4 | | | | | | | 5 | | | | | | | | | | | | | | | | | | | | | | | | AIN4 |
| | | | AnalogInput5 | | | | | | | 6 | | | | | | | | | | | | | | | | | | | | | | | | AIN5 |
| | | | AnalogInput6 | | | | | | | 7 | | | | | | | | | | | | | | | | | | | | | | | | AIN6 |
| | | | AnalogInput7 | | | | | | | 8 | | | | | | | | | | | | | | | | | | | | | | | | AIN7 |
| | | | VDD | | | | | | | 9 | | | | | | | | | | | | | | | | | | | | | | | | VDD |
| | | | VDDHDIV5 | | | | | | | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | VDDH/5 |

## 36.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Positive channel resistor control |
| | | | Bypass | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | Bypass resistor ladder |
| | | | Pulldown | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | Pull-down to GND |
| | | | Pullup | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | | Pull-up to VDD |
| | | | VDD1_2 | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | | Set input at VDD/2 |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Negative channel resistor control |
| | | | Bypass | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | Bypass resistor ladder |
| | | | Pulldown | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | Pull-down to GND |
| | | | Pullup | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | | Pull-up to VDD |
| | | | VDD1_2 | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | | Set input at VDD/2 |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Gain control |
| | | | Gain1_6 | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | 1/6 |
| | | | Gain1_5 | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | 1/5 |
| | | | Gain1_4 | | | | | | | 2 | | | | | | | | | | | | | | | | | | | | | | | | 1/4 |
| | | | Gain1_3 | | | | | | | 3 | | | | | | | | | | | | | | | | | | | | | | | | 1/3 |
| | | | Gain1_2 | | | | | | | 4 | | | | | | | | | | | | | | | | | | | | | | | | 1/2 |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **Value Id** | **Value** | **Description** |
| | VDDHDIV5 | 0x0D | VDDH/5 |

## 36.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **Value Id** | **Value** | **Description** |
| A | NC | 0 | Analog negative input, enables differential channel<br>Not connected |
| | AnalogInput0 | 1 | AIN0 |
| | AnalogInput1 | 2 | AIN1 |
| | AnalogInput2 | 3 | AIN2 |
| | AnalogInput3 | 4 | AIN3 |
| | AnalogInput4 | 5 | AIN4 |
| | AnalogInput5 | 6 | AIN5 |
| | AnalogInput6 | 7 | AIN6 |
| | AnalogInput7 | 8 | AIN7 |
| | VDD | 9 | VDD |
| | VDDHDIV5 | 0x0D | VDDH/5 |

## 36.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | G F E E E D C C C B B A A |
| **Reset 0x00020000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **Value Id** | **Value** | **Description** |
| A | | | Positive channel resistor control |
| | Bypass | 0 | Bypass resistor ladder |
| | Pulldown | 1 | Pull-down to GND |
| | Pullup | 2 | Pull-up to VDD |
| | VDD1_2 | 3 | Set input at VDD/2 |
| B | | | Negative channel resistor control |
| | Bypass | 0 | Bypass resistor ladder |
| | Pulldown | 1 | Pull-down to GND |
| | Pullup | 2 | Pull-up to VDD |
| | VDD1_2 | 3 | Set input at VDD/2 |
| C | | | Gain control |
| | Gain1_6 | 0 | 1/6 |
| | Gain1_5 | 1 | 1/5 |
| | Gain1_4 | 2 | 1/4 |
| | Gain1_3 | 3 | 1/3 |
| | Gain1_2 | 4 | 1/2 |
| | Gain1 | 5 | 1 |
| | Gain2 | 6 | 2 |
| | Gain4 | 7 | 4 |
| D | | | Reference control |
| | Internal | 0 | Internal reference (0.6 V) |
| | VDD1_4 | 1 | VDD/4 as reference |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSELP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | PSELN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Analog negative input, enables differential channel |
| | | | NC | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Not connected |
| | | | AnalogInput0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN0 |
| | | | AnalogInput1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN1 |
| | | | AnalogInput2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN2 |
| | | | AnalogInput3 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN3 |
| | | | AnalogInput4 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN4 |
| | | | AnalogInput5 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN5 |
| | | | AnalogInput6 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN6 |
| | | | AnalogInput7 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | AIN7 |
| | | | VDD | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | VDD |
| | | | VDDHDIV5 | 0x0D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | VDDH/5 |

## 36.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | RESP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Positive channel resistor control |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Bypass resistor ladder |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull-down to GND |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull-up to VDD |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Set input at VDD/2 |
| B | RW | RESN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Negative channel resistor control |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Bypass resistor ladder |
| | | | Pulldown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull-down to GND |
| | | | Pullup | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pull-up to VDD |
| | | | VDD1_2 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Set input at VDD/2 |
| C | RW | GAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Gain control |
| | | | Gain1_6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/6 |
| | | | Gain1_5 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/5 |
| | | | Gain1_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/4 |
| | | | Gain1_3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/3 |
| | | | Gain1_2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1/2 |
| | | | Gain1 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 |
| | | | Gain2 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 2 |
| | | | Gain4 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 4 |
| D | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reference control |
| | | | Internal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Internal reference (0.6 V) |
| | | | VDD1_4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | VDD/4 as reference |
| E | RW | TACQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Acquisition time, the time the ADC uses to sample the input voltage |
| | | | 3us | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3 us |
| | | | 5us | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 5 us |
| | | | 10us | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 10 us |
| | | | 15us | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 15 us |
| | | | 20us | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 20 us |
| | | | 40us | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 40 us |
| F | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable differential mode |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Single ended, PSELN will be ignored, negative input to ADC shorted to GND |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | G | | | | F | | E | E | E | | | | D | | C | C | C | | | B | B | | | A | A |
| **Reset 0x00020000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | BURST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.37 CH[7].LIMIT

Address offset: 0x58C

High/low limits for event monitoring a channel

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x7FFF8000** | | | | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOW | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HIGH | | [-32768 to +32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.38 RESOLUTION

Address offset: 0x5F0

Resolution configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | VAL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 8bit | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 10bit | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 12bit | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 14bit | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 36.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OVERSAMPLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Bypass | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over2x | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over4x | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over8x | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over16x | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over32x | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over64x | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over128x | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Over256x | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 36.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | B | | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CC | | [80..2047] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Task | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Timers | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 36.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 36.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MAXCNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 36.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | AMOUNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Number of buffer words transferred since last START. This register can be read after an END or STOPPED event.

## 36.12 Electrical specification

### 36.12.1 SAADC Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| DNL | Differential non-linearity, 10-bit resolution | -0.95 | <1 | | LSB |
| INL | Integral non-linearity, 10-bit resolution | | 1 | | LSB |
| $V_{OS}$ | Differential offset error (calibrated), 10-bit resolution [a] | | +-2 | | LSB |
| $E_{VDDHDIV5}$ | Error on VDDHDIV5 input | | +-1 | | % |

[a] Digital output code at zero volt differential input.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{EG}$ | Gain error temperature coefficient | | 0.02 | | %/°C |
| $f_{SAMPLE}$ | Maximum sampling rate | | | 200 | kHz |
| $t_{ACQ,10k}$ | Acquisition time (configurable), source Resistance <= 10kOhm | | 3 | | µs |
| $t_{ACQ,40k}$ | Acquisition time (configurable), source Resistance <= 40kOhm | | 5 | | µs |
| $t_{ACQ,100k}$ | Acquisition time (configurable), source Resistance <= 100kOhm | | 10 | | µs |
| $t_{ACQ,200k}$ | Acquisition time (configurable), source Resistance <= 200kOhm | | 15 | | µs |
| $t_{ACQ,400k}$ | Acquisition time (configurable), source Resistance <= 400kOhm | | 20 | | µs |
| $t_{ACQ,800k}$ | Acquisition time (configurable), source Resistance <= 800kOhm | | 40 | | µs |
| $t_{CONV}$ | Conversion time | | <2 | | µs |
| $I_{ADC,CONV}$ | ADC current during ACQuisition and CONVersion | | 700 | | µA |
| $I_{ADC,IDLE}$ | Idle current, when not sampling, excluding clock sources and regulator base currents[30] | | <5 | | µA |
| $E_{G1/6}$ | Error[b] for Gain = 1/6 | -3 | | 3 | % |
| $E_{G1/4}$ | Error[b] for Gain = 1/4 | -3 | | 3 | % |
| $E_{G1/2}$ | Error[b] for Gain = 1/2 | -3 | | 4 | % |
| $E_{G1}$ | Error[b] for Gain = 1 | -3 | | 4 | % |
| $C_{SAMPLE}$ | Sample and hold capacitance at maximum gain[31] | | 2.5 | | pF |
| $R_{INPUT}$ | Input resistance | | >1 | | MΩ |
| $E_{NOB}$ | Effective number of bits, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps | | 9 | | Bit |
| $S_{NDR}$ | Peak signal to noise and distortion ratio, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps | | 56 | | dB |
| $S_{FDR}$ | Spurious free dynamic range, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps | | 70 | | dBc |
| $R_{LADDER}$ | Ladder resistance | | 160 | | kΩ |

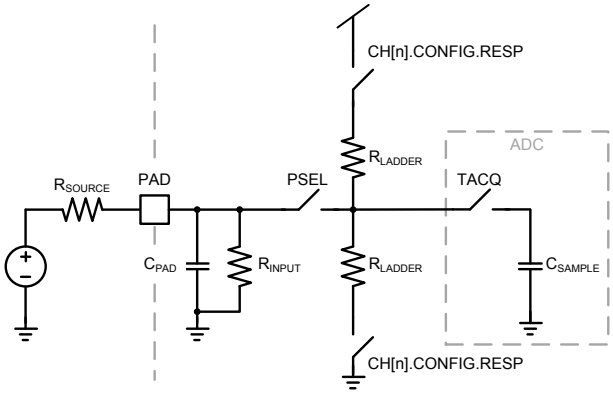



**Figure 114: Model of SAADC input (one channel)**

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time ( $t_{conv}$ and $t_{ACQ}$) and conversion and idle current ($I_{ADC,CONV}$ and $I_{ADC,IDLE}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{(t_{CONV} + t_{ACQ})}{250}\right)(I_{ADC,CONV}) + \left(\frac{250 - (t_{CONV} + t_{ACQ})}{250}\right)(I_{ADC,IDLE})$$

30 When $t_{ACQ}$ is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If $t_{ACQ}$ is smaller than 10us and DC/DC is active, refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on $t_{ACQ}$ and other resources' needs, the appropriate base current needs to be taken into account.

b Does not include temperature drift

31 Maximum gain corresponds to highest capacitance.

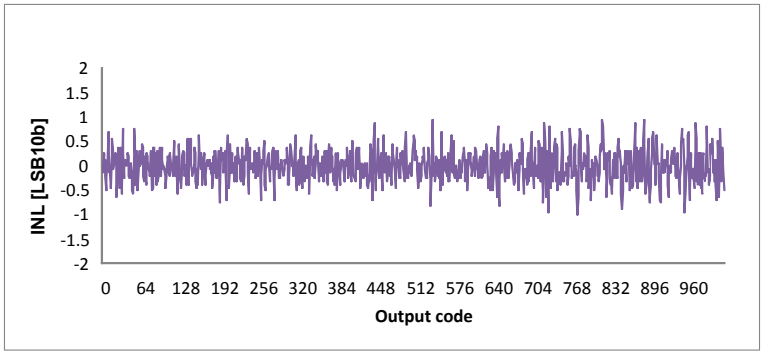



**Figure 115: ADC INL vs Output Code**

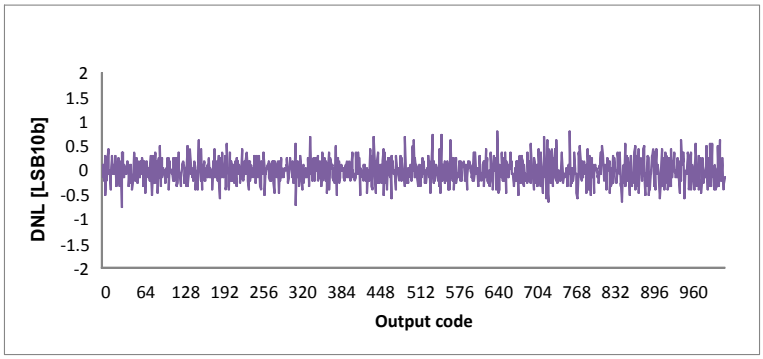



**Figure 116: ADC DNL vs Output Code**

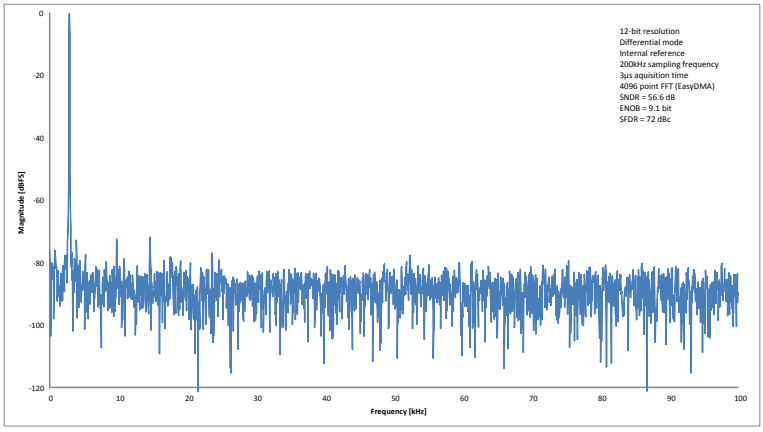



**Figure 117: FFT of a 2.8 kHz sine at 200 ksps ()**

## 36.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.

# 37 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
  - Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
  - Configurable 50 mV hysteresis
- Reference inputs (VREF):
  - VDD
  - External reference from AIN0 to AIN7 (between 0 V and VDD)
  - Internal references 1.2 V, 1.8 V and 2.4 V
- Three speed/power consumption modes: low-power, normal and high-speed
- Single-pin capacitive sensor support
- Event generation on output changes
  - UP event on VIN- > VIN+
  - DOWN event on VIN- < VIN+
  - CROSS event on VIN+ and VIN- crossing
  - READY event on core and internal reference (if used) ready

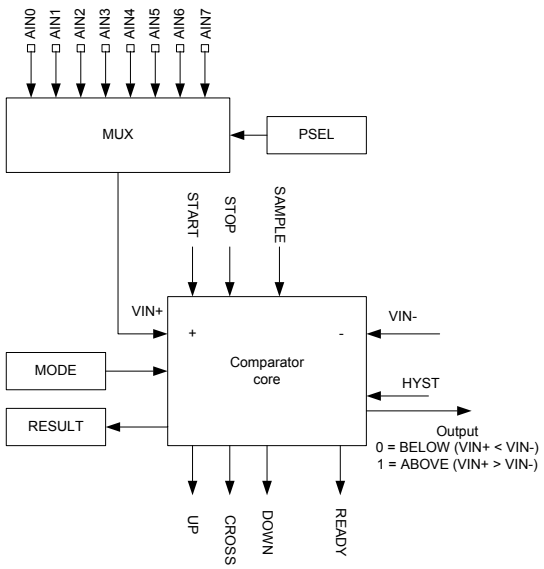



**Figure 118: Comparator overview**

Once enabled (using the *ENABLE* register), the comparator is started by triggering the START task and stopped by triggering the STOP task. After a start-up time of $t_{COMP,START}$, the comparator will generate a READY event to indicate that it is ready for use and that its output is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.

### 37 Operation modes

The comparator can be configured to operate in two main operation modes, differential mode and single-ended mode. See the *MODE* register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the *PSEL* register to select any of the AIN0-AIN7 pins as VIN+ input, irregardless of the operation mode selected for the comparator. The source of VIN- depends on which operation mode is used:

- Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the *HYST* register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see *Figure 121: Comparator in single-ended mode* on page 456). This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 122: Hysteresis example where VIN+ starts below VUP* on page 456 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to *RESULT* register by triggering the SAMPLE task.

## 37.1 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the differential mode:

- *PSEL*
- *MODE*
- *EXTREFSEL*

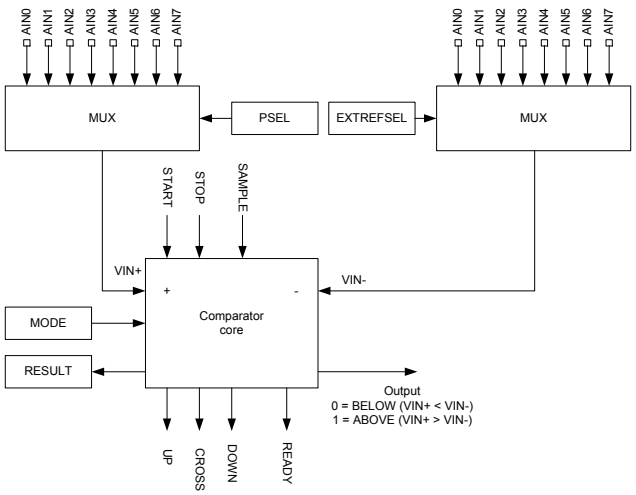



**Figure 119: Comparator in differential mode**

**Restriction:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When *HYST* register is turned on while in this mode, the output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes lower than VIN- - ($V_{DIFFHYST}$ / 2). It will also change from BELOW to ABOVE whenever VIN+ becomes higher than VIN- + ($V_{DIFFHYST}$ / 2). This behavior is illustrated in *Figure 120: Hysteresis enabled in differential mode* on page 455.

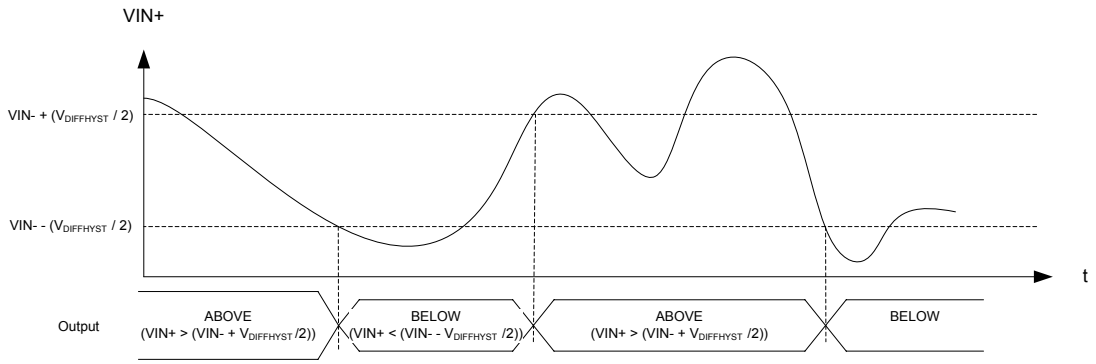



**Figure 120: Hysteresis enabled in differential mode**

## 37.2 Single-ended mode

In single-ended mode, VIN- is derived from the reference ladder.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the single-ended mode:

- *PSEL*
- *MODE*
- *REFSEL*
- *EXTREFSEL*
- *TH*

The reference ladder uses the reference voltage (VREF) to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured using THUP and THDOWN respectively in the *TH* register. VREF can be derived from any of the available reference sources, configured using the *EXTREFSEL* and *REFSEL* registers as illustrated in *Figure 121: Comparator in single-ended mode* on page 456. When AREF is selected in the *REFSEL* register, the *EXTREFSEL* register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.

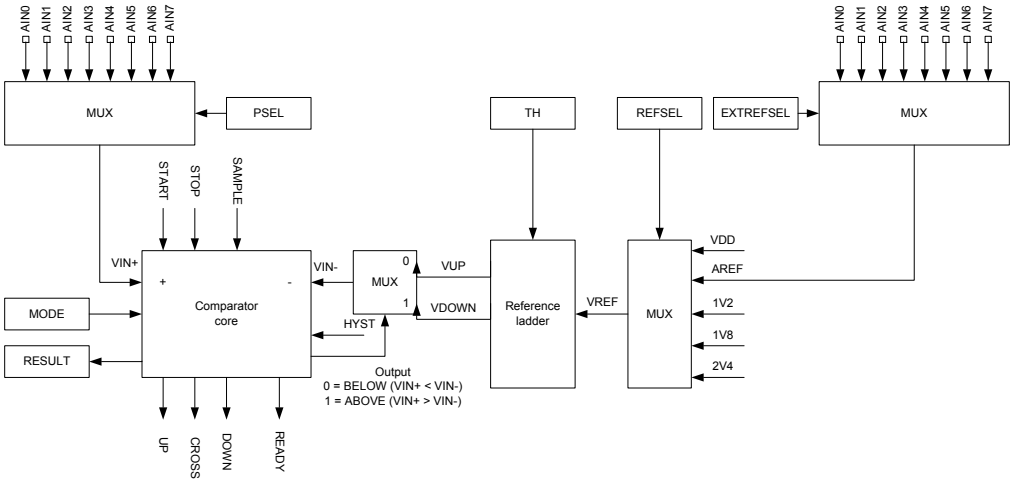



**Figure 121: Comparator in single-ended mode**

> **Restriction:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the *RESULT* register, VIN- will switch to VDOWN. When VIN+ falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis can be generated as illustrated in *Figure 122: Hysteresis example where VIN+ starts below VUP* on page 456 and *Figure 123: Hysteresis example where VIN+ starts above VUP* on page 457.

Writing to *HYST* has no effect in single-ended mode, and the content of this register is ignored.

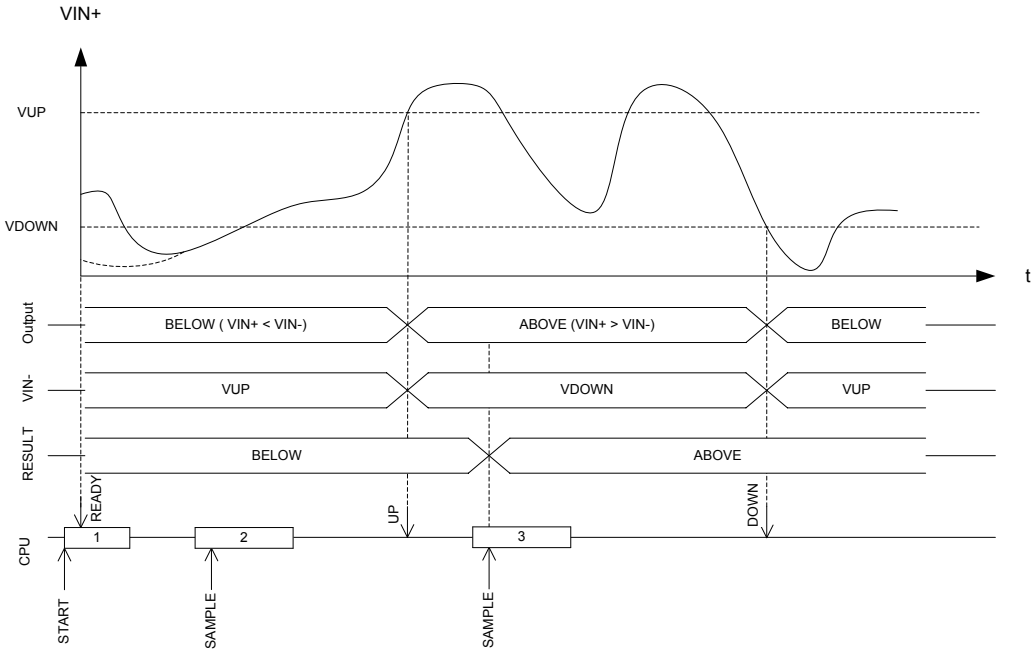



**Figure 122: Hysteresis example where VIN+ starts below VUP**

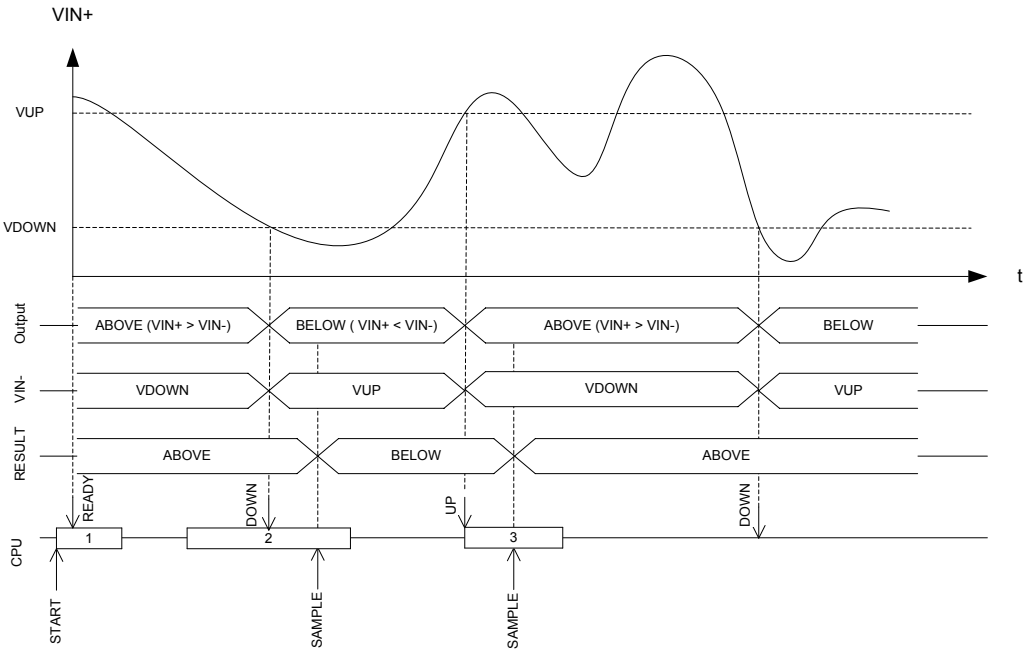



**Figure 123: Hysteresis example where VIN+ starts above VUP**

# 37.3 Registers

### Table 83: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40013000 | COMP | COMP | General purpose comparator | |

### Table 84: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start comparator |
| TASKS_STOP | 0x004 | Stop comparator |
| TASKS_SAMPLE | 0x008 | Sample comparator value |
| EVENTS_READY | 0x100 | COMP is ready and output is valid |
| EVENTS_DOWN | 0x104 | Downward crossing |
| EVENTS_UP | 0x108 | Upward crossing |
| EVENTS_CROSS | 0x10C | Downward or upward crossing |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *RESULT* | 0x400 | Compare result |
| *ENABLE* | 0x500 | COMP enable |
| *PSEL* | 0x504 | Pin select |
| *REFSEL* | 0x508 | Reference source select for single-ended mode |
| *EXTREFSEL* | 0x50C | External reference select |
| *TH* | 0x530 | Threshold configuration for hysteresis unit |
| *MODE* | 0x534 | Mode configuration |
| *HYST* | 0x538 | Comparator hysteresis enable |

## 37.3.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY_SAMPLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | READY_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DOWN_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | UP_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | CROSS_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 37.3.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | UP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CROSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 37.3.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | UP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CROSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 37.3.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | UP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CROSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.5 RESULT

Address offset: 0x400

Compare result

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RESULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Below | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Above | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.6 ENABLE

Address offset: 0x500

COMP enable

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.7 PSEL

Address offset: 0x504

Pin select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.8 REFSEL

Address offset: 0x508

Reference source select for single-ended mode

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000004** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Int1V2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Int1V8 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Int2V4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | VDD | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ARef | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.9 EXTREFSEL

Address offset: 0x50C

External reference select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EXTREFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference2 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference4 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference5 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference6 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference7 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | B | B | B | B | B | B | | | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | THDOWN | | [63:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | THUP | | [63:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.11 MODE

Address offset: 0x534

Mode configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Normal | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | MAIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SE | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Diff | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 37.3.12 HYST

Address offset: 0x538

Comparator hysteresis enable

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | HYST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoHyst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Hyst50mV | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 37.4 Electrical specification

### 37.4.1 COMP Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{COMP,LP}$ | Core run current in low power mode | | 2 | | µA |
| $I_{COMP,N}$ | Core run current in normal mode | | 5 | | µA |
| $I_{COMP,HS}$ | Core run current in high-speed mode | | 10 | | µA |
| $t_{PROPDLY,LP}$ | Propagation delay, low-power mode[a] | | 0.6 | | µS |
| $t_{PROPDLY,N}$ | Propagation delay, normal mode[a] | | 0.2 | | µS |
| $t_{PROPDLY,HS}$ | Propagation delay, high-speed mode[a] | | 0.1 | | µS |
| $V_{DIFFHYST}$ | Optional hysteresis applied to differential input | | 30 | | mV |
| $V_{VDD-VREF}$ | Required difference between VDD and a selected VREF, VDD > VREF | 0.3 | | | V |
| $I_{INT\_REF}$ | Current used by the internal bandgap reference when selected as source for VREF | | 13 | | µA |
| $t_{INT\_REF,START}$ | Startup time for the internal bandgap reference | | 50 | 80 | µS |
| $E_{INT\_REF}$ | Internal bandgap reference error | -3 | | 3 | % |
| $R_{LADDER}$ | Reference ladder resistance, $I_{LADDER}$ = VREF / $R_{LADDER}$ | | 550 | | kΩ |
| $V_{INPUTOFFSET}$ | Input offset | -10 | | 10 | mV |
| $D_{NLLADDER}$ | Differential non-linearity of reference ladder | .. | .. | .. | LSB |
| $t_{COMP,START}$ | Startup time for the comparator core | | 3 | | µS |

Total comparator run current must be calculated from the $I_{COMP}$, $I_{INT\_REF}$, and $I_{LADDER}$ values for a given reference voltage.

[a] Propagation delay is with 10 mV overdrive.

# 38 LPCOMP — Low power comparator

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 - VDD input range
- Ultra low power
- Eight input options (AIN0 to AIN7)
- Reference voltage options:
  - Two external analog reference inputs, or
  - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Wakeup source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

**Restriction:** LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

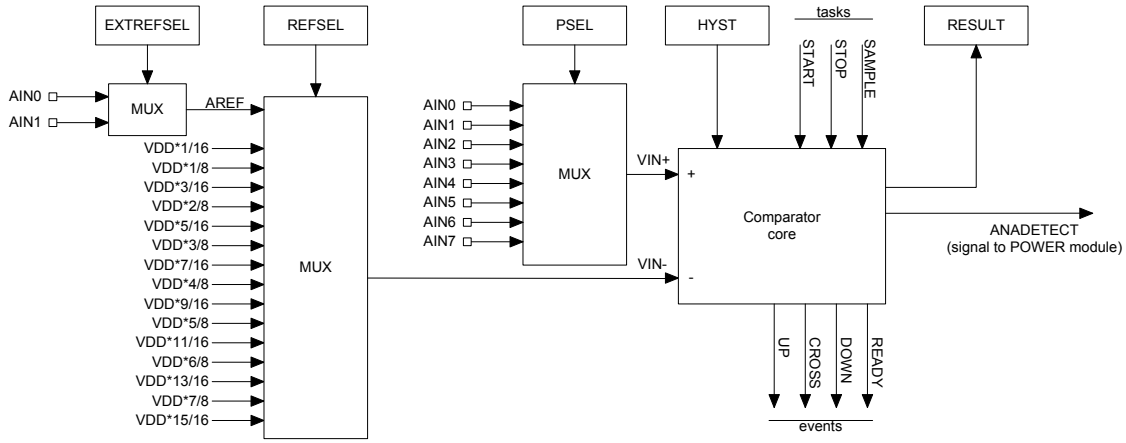



**Figure 124: Low power comparator**

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the *REFSEL* on page 468 and *EXTREFSEL* registers.

The *PSEL*, *REFSEL*, and *EXTREFSEL* registers must be configured before the LPCOMP is enabled through the *ENABLE* register.

The *HYST* register allows enabling an optional hysteresis in the comparator core. This hysteresis shall prevent noise on the signal to create unwanted events. See *Figure 125: Effect of hysteresis on a noisy input signal* on page 464 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

The LPCOMP is started by triggering the START task. After a start-up time of $t_{LPCOMP,STARTUP}$ the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).

The LPCOMP is stopped by triggering the STOP task.

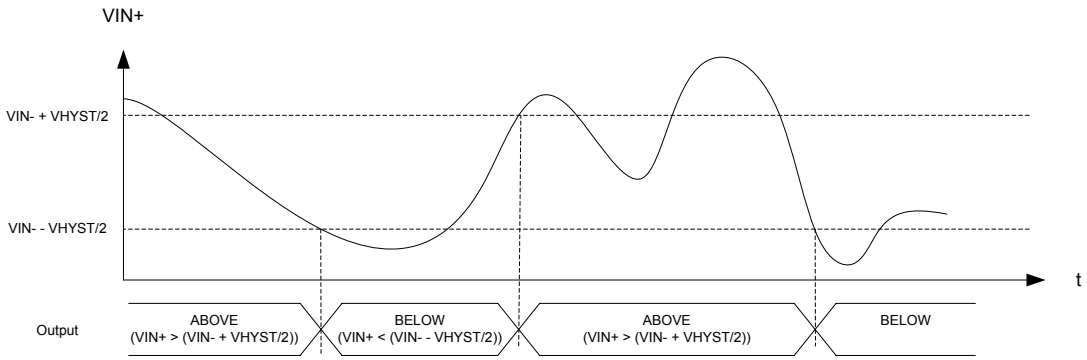



**Figure 125: Effect of hysteresis on a noisy input signal**

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See *POWER — Power supply* on page 66 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including *ENABLE*, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register ( *ANADETECT* on page 468) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to *RESULT* on page 467 by triggering the SAMPLE task.

See *RESETREAS* on page 77 for more information on how to detect a wakeup from LPCOMP.

## 38.1 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behaviour.

## 38.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, `AIN0` through `AIN7`, as the analog input pin for the LPCOMP.

See *GPIO — General purpose input/output* on page 154 for more information about the pins. Similarly, you can use *EXTREFSEL* on page 468 to select one of the analog reference input pins, `AIN0` and `AIN1`, as input for AREF in case AREF is selected in *EXTREFSEL* on page 468. The selected analog pins will be acquired by the LPCOMP when it is enabled through *ENABLE* on page 467.

## 38.3 Registers

### Table 85: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40013000 | LPCOMP | LPCOMP | Low power comparator | |

### Table 86: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start comparator |
| TASKS_STOP | 0x004 | Stop comparator |
| TASKS_SAMPLE | 0x008 | Sample comparator value |
| EVENTS_READY | 0x100 | LPCOMP is ready and output is valid |
| EVENTS_DOWN | 0x104 | Downward crossing |
| EVENTS_UP | 0x108 | Upward crossing |
| EVENTS_CROSS | 0x10C | Downward or upward crossing |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *RESULT* | 0x400 | Compare result |
| *ENABLE* | 0x500 | Enable LPCOMP |
| *PSEL* | 0x504 | Input pin select |
| *REFSEL* | 0x508 | Reference select |
| *EXTREFSEL* | 0x50C | External reference select |
| *ANADETECT* | 0x520 | Analog detect configuration |
| *HYST* | 0x538 | Comparator hysteresis enable |

### 38.3.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | | | | | | | | | | | | | | | | | | | | | | | | | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | READY_SAMPLE | | | Shortcut between READY event and SAMPLE task<br>See *EVENTS_READY* and *TASKS_SAMPLE* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | READY_STOP | | | Shortcut between READY event and STOP task<br>See *EVENTS_READY* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| C | RW | DOWN_STOP | | | Shortcut between DOWN event and STOP task<br>See *EVENTS_DOWN* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| D | RW | UP_STOP | | | Shortcut between UP event and STOP task<br>See *EVENTS_UP* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| E | RW | CROSS_STOP | | | Shortcut between CROSS event and STOP task<br>See *EVENTS_CROSS* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Enable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 38.3.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Enable interrupt for READY event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Enable interrupt for DOWN event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_DOWN* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | UP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Enable interrupt for UP event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_UP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CROSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Enable interrupt for CROSS event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_CROSS* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 38.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Disable interrupt for READY event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Disable interrupt for DOWN event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_DOWN* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | UP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Write '1' to Disable interrupt for UP event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_UP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CROSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 38.3.4 RESULT

Address offset: 0x400

Compare result

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RESULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Below | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Above | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 38.3.5 ENABLE

Address offset: 0x500

Enable LPCOMP

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 38.3.6 PSEL

Address offset: 0x504

Input pin select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput2 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput4 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput5 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput6 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogInput7 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 38.3.7 REFSEL

Address offset: 0x508

Reference select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000004** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | REFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref1_8Vdd | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref2_8Vdd | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref3_8Vdd | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref4_8Vdd | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref5_8Vdd | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref6_8Vdd | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref7_8Vdd | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ARef | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref1_16Vdd | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref3_16Vdd | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref5_16Vdd | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref7_16Vdd | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref9_16Vdd | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref11_16Vdd | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref13_16Vdd | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ref15_16Vdd | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 38.3.8 EXTREFSEL

Address offset: 0x50C

External reference select

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EXTREFSEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | AnalogReference1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 38.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ANADETECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Cross | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Up | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Down | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 38.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | HYST | | | Comparator hysteresis enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Comparator hysteresis disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Comparator hysteresis enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 38.4 Electrical specification

## 38.4.1 LPCOMP Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{LPC}$ | Run current for low power comparator | | 0.5 | | µA |
| $t_{LPCANADET}$ | Time from VIN crossing (>=50mV above threshold) to ANADETECT signal generated. | | 5 | | µs |
| $V_{INPOFFSET}$ | Input offset including reference ladder error | -40 | | 40 | mV |
| $V_{HYST}$ | Optional hysteresis | | 35 | | mV |
| $t_{STARTUP}$ | Startup time for LPCOMP | | 140 | | µs |

# 39 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK — Clock control* on page 141.

## 39.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

## 39.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

## 39.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 73 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 74.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.

# 39.4 Registers

### Table 87: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40010000 | WDT | WDT | Watchdog timer | |

### Table 88: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Start the watchdog |
| EVENTS_TIMEOUT | 0x100 | Watchdog timeout |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *RUNSTATUS* | 0x400 | Run status |
| *REQSTATUS* | 0x404 | Request status |
| *CRV* | 0x504 | Counter reload value |
| *RREN* | 0x508 | Enable register for reload request registers |
| *CONFIG* | 0x50C | Configuration register |
| *RR[0]* | 0x600 | Reload request 0 |
| *RR[1]* | 0x604 | Reload request 1 |
| *RR[2]* | 0x608 | Reload request 2 |
| *RR[3]* | 0x60C | Reload request 3 |
| *RR[4]* | 0x610 | Reload request 4 |
| *RR[5]* | 0x614 | Reload request 5 |
| *RR[6]* | 0x618 | Reload request 6 |
| *RR[7]* | 0x61C | Reload request 7 |

## 39.4.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TIMEOUT | | | Write '1' to Enable interrupt for TIMEOUT event<br>See *EVENTS_TIMEOUT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TIMEOUT | | | Write '1' to Disable interrupt for TIMEOUT event<br>See *EVENTS_TIMEOUT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | Disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 39.4.3 RUNSTATUS

Address offset: 0x400

Run status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RUNSTATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotRunning | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Running | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 39.4.4 REQSTATUS

Address offset: 0x404

Request status

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | RR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | RR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | R | RR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | R | RR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | R | RR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | R | RR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | R | RR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DisabledOrRequested | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | EnabledAndUnrequested | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 39.4.5 CRV

Address offset: 0x504

Counter reload value

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CRV | | [0x0000000F..0xFFFFFFFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | clock | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | RR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.7 CONFIG

Address offset: 0x50C

Configuration register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | | | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SLEEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pause | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Run | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | HALT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pause | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Run | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.8 RR[0]

Address offset: 0x600

Reload request 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.9 RR[1]

Address offset: 0x604

Reload request 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.10 RR[2]

Address offset: 0x608

Reload request 2

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.11 RR[3]

Address offset: 0x60C

Reload request 3

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.12 RR[4]

Address offset: 0x610

Reload request 4

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 39.4.13 RR[5]

Address offset: 0x614

Reload request 5

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | Reload request register | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | Value to request a reload of the watchdog timer | | | | | | | | | |

### 39.4.14 RR[6]

Address offset: 0x618

Reload request 6

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | Reload request register | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | Value to request a reload of the watchdog timer | | | | | | | | | |

### 39.4.15 RR[7]

Address offset: 0x61C

Reload request 7

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | W | RR | | | | | | | | | | | | | | | | | | | | | | | | Reload request register | | | | | | | | | |
| | | | Reload | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | Value to request a reload of the watchdog timer | | | | | | | | | |

## 39.5 Electrical specification

### 39.5.1 Watchdog Timer Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{WDT}$ | Run current for watchdog timer | | 0.3 | 2 | µA |
| $t_{WDT}$ | Time out interval | 458 µs | | 36 h | |

# 40 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

## 40.1 Registers

### Table 89: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40014000 | SWI | SWI0 | Software interrupt 0 | |
| 0x40015000 | SWI | SWI1 | Software interrupt 1 | |
| 0x40016000 | SWI | SWI2 | Software interrupt 2 | |
| 0x40017000 | SWI | SWI3 | Software interrupt 3 | |
| 0x40018000 | SWI | SWI4 | Software interrupt 4 | |
| 0x40019000 | SWI | SWI5 | Software interrupt 5 | |

# 41 NFCT — Near field communication tag

The NFCT peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

With appropriate software, the NFCT peripheral can be used as the listening device NFC-A as specified by the *NFC Forum*.

Listed here are the main features for the NFCT peripheral:

- NFC-A listen mode operation
  - 13.56 MHz input frequency
  - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, cyclic redundancy check (CRC), and parity functions

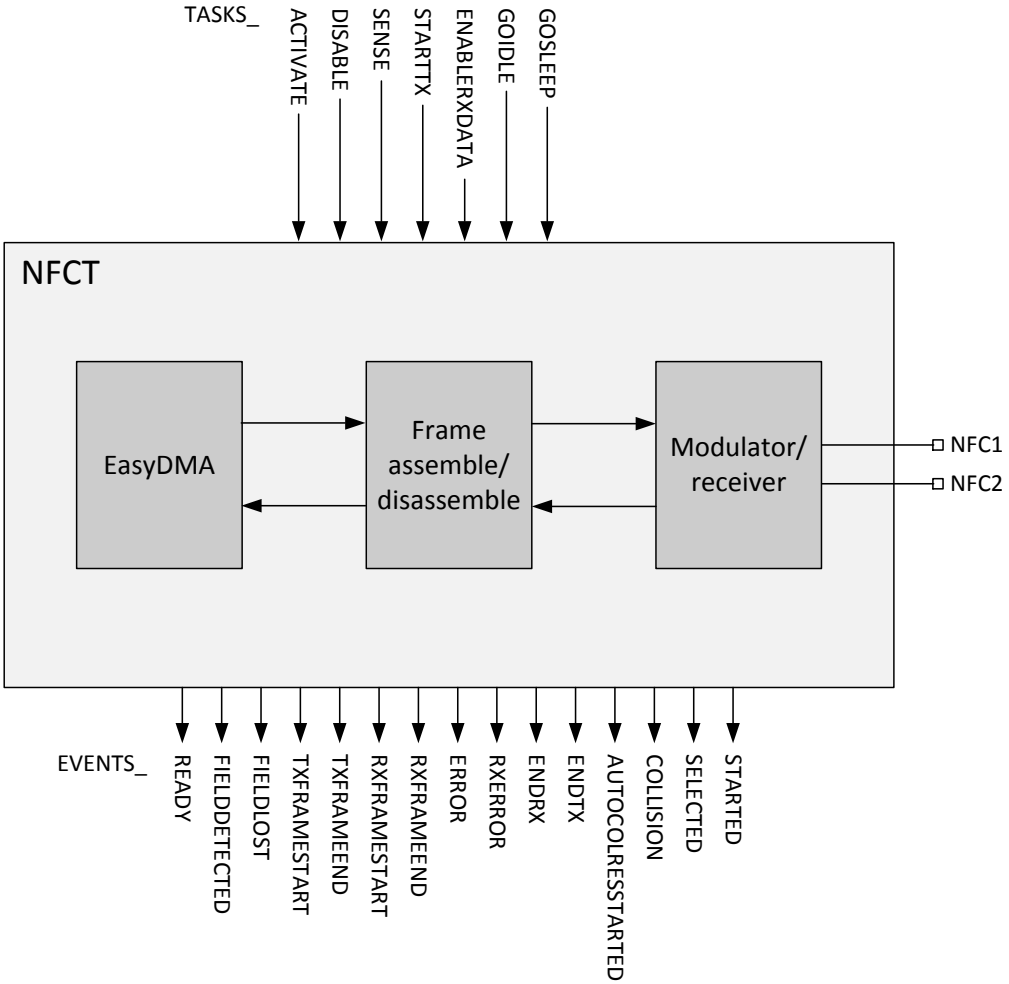



**Figure 126: NFCT block diagram**

## 41.1 Overview

The NFCT peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator with 106 kbps data rate as defined by the NFC Forum.

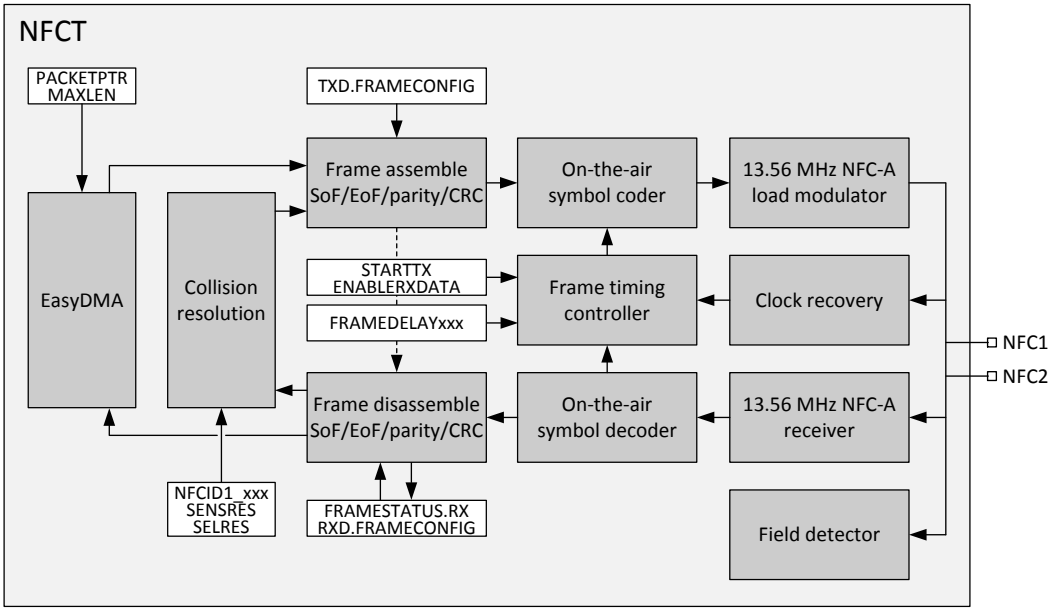



**Figure 127: NFCT overview**

When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent. The received frames will be automatically disassembled and the data part of the frame transferred to RAM.

The NFCT peripheral also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.

Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFCT functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a *FIELDDETECTED* event. When the strength of the field no longer supports NFC communication, the module will generate a *FIELDLOST* event. For the Low Power Field Detect threshold values, refer to *NFCT Electrical Specification* on page 498.

In System OFF, the NFCT Low Power Field Detect function can wake the system up through a reset. The NFC bit in the RESETREAS register in *POWER — Power supply* on page 66 will be set as the cause of the wake-up.

If the system is put into System OFF mode while a field is already present, the NFCT Low Power Field Detect function will wake the system up right away and generate a reset.

> **Important:** As a consequence of a reset, NFCT is disabled, and therefore the reset handler will have to activate NFCT again and set it up properly.

The HFXO must be running before the NFCT peripheral goes into ACTIVATED state. Note that the NFCT peripheral calibration is automatically done on *ACTIVATE* task. The HFXO can be turned off when the NFCT peripheral goes into SENSE mode. The shortcut FIELDDETECTED_ACTIVATE can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the *TXD.FRAMECONFIG* on page 494 register. Incoming data will be disassembled according to the *RXD.FRAMECONFIG* register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFCT peripheral includes a frame timing controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

## 41.2 Operating states

Tasks and events are used to control the operating state of the peripheral. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See *Figure 126: NFCT block diagram* on page 477 and *Figure 128: NFCT state diagram, automatic collision resolution enabled* on page 479 for more information.

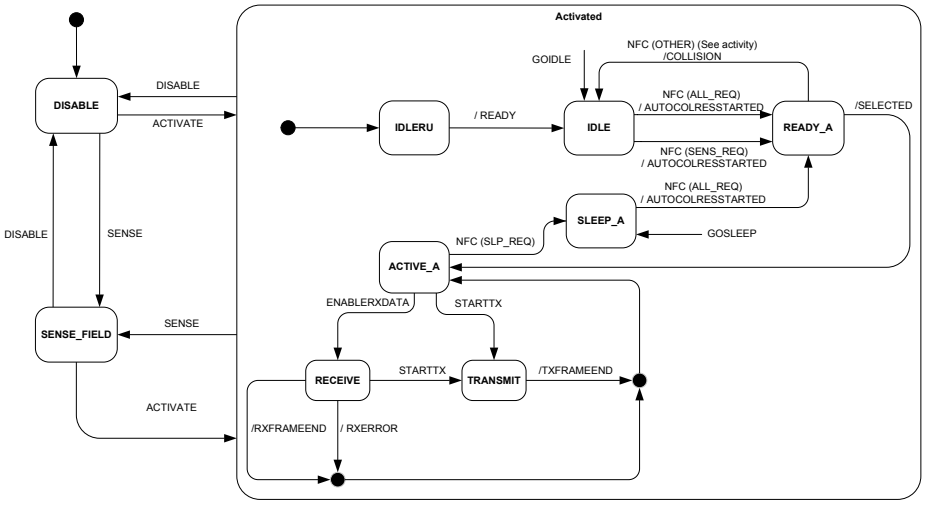



**Figure 128: NFCT state diagram, automatic collision resolution enabled**

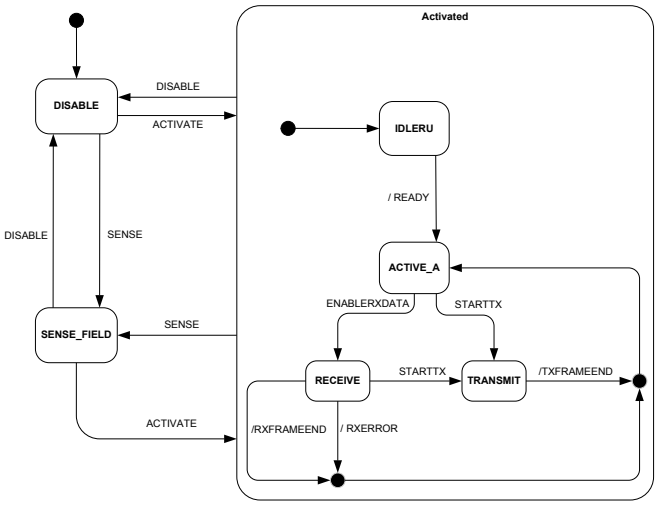



**Figure 129: NFCT state diagram, automatic collision resolution disabled**

**Important:**

- *FIELDLOST* event will not be reflected in the state machine (for instance by going back to the DISABLE state). It is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- Sending SENSE task while field is still present does not generate *FIELDDETECTED* event.
- If the FIELDDETECTED event is cleared before sending the *ACTIVATE* task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.

## 41.3 Pin configuration

NFCT uses two pins to connect the antenna and these pins are shared with GPIOs.

The PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset. See *Pin assignments* on page 13 for the pins used by the NFCT peripheral.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2V. The GPIO function on those pins will also be disabled.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFCT antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFCT antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to $C_{PAD\_NFC}$ in the Electrical Specification of *GPIO — General purpose input/output* on page 154), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power, the two pins should always be set to the same logical value whenever entering one of the device power saving modes. For details, refer to $I_{NFC\_LEAK}$ in the Electrical Specification of *GPIO — General purpose input/output* on page 154.

## 41.4 EasyDMA

The NFCT peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM.

The NFCT EasyDMA utilizes a pointer called *PACKETPTR* on page 494 for receiving and transmitting packets.

The NFCT peripheral uses EasyDMA to read or write RAM, but not both at the same time. The event *RXFRAMESTART* indicates that the EasyDMA has started writing to the RAM for a receive frame and the event *RXFRAMEND* indicates that the EasyDMA has completed writing to the RAM. Similarly, the event *TXFRAMESTART* indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event *TXFRAMEND* indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA is writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation when there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or RXFRAMEEND event for the ongoing transmit or receive before starting a new receive or transmit operation.

The *MAXLEN* on page 494 register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to ensure that the NFCT peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the *RXD.AMOUNT* or *TXD.AMOUNT* register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In that situation, in RX, the OVERRUN bit in the *FRAMESTATUS.RX* register will be set and an *RXERROR* event will be triggered.

> **Important:** The RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding start of frame (SoF), end of frame (EoF), and parity, but including CRC for RXD.AMOUNT only. Make sure to take potential additional bits into account when setting MAXLEN.

Only sending task *ENABLERXDATA* ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a hard fault or RAM corruption. For more information about the different memory regions, see Chapter *Memory* on page 20.

The NFCT peripherals normally do alternative receive and transmit frames. Therefore, to prepare for the next frame, the PACKETPTR, MAXLEN, *TXD.FRAMECONFIG* and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and *RXD.FRAMECONFIG* can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the *STARTED* event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with *NFC Forum, NFC Digital Protocol Technical Specification*, the least significant bit (LSB) from the least significant byte (LSByte) is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

## 41.5 Frame assembler

The NFCT peripheral implements a frame assembler in hardware.

When the NFCT peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For RX, see *Frame disassembler* on page 482. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the *PACKETPTR* and MAXLEN registers respectively, then issuing a STARTTX task.

MAXLEN must be set so that it matches the size of the frame to be sent.

The *STARTED* event indicates that the PACKETPTR and MAXLEN registers have been captured by the frame assembler EasyDMA.

When asserting the *STARTTX* task, the frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFCT peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly if set in TXD.FRAMECONFIG. The NFCT peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to the settings in *TXD.FRAMECONFIG*. Both short frames, standard frames, and bit-oriented SDD frames as specified in the *NFC Forum, NFC Digital Protocol Technical Specification* can be assembled by the correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte, least significant bit (LSB) first. That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum, NFC Digital Protocol Technical Specification*.

> **Important:** Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (most significant bit (MSB)), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally number them from b0 to b7. The present document uses the b0–b7 numbering scheme. Be aware of this when comparing the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add SoF symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES. TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.

The frame assemble operation is illustrated in *Figure 130: Frame assemble illustration* on page 482 for different settings in TXD.FRAMECONFIG. All shaded bit fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFCT peripheral.

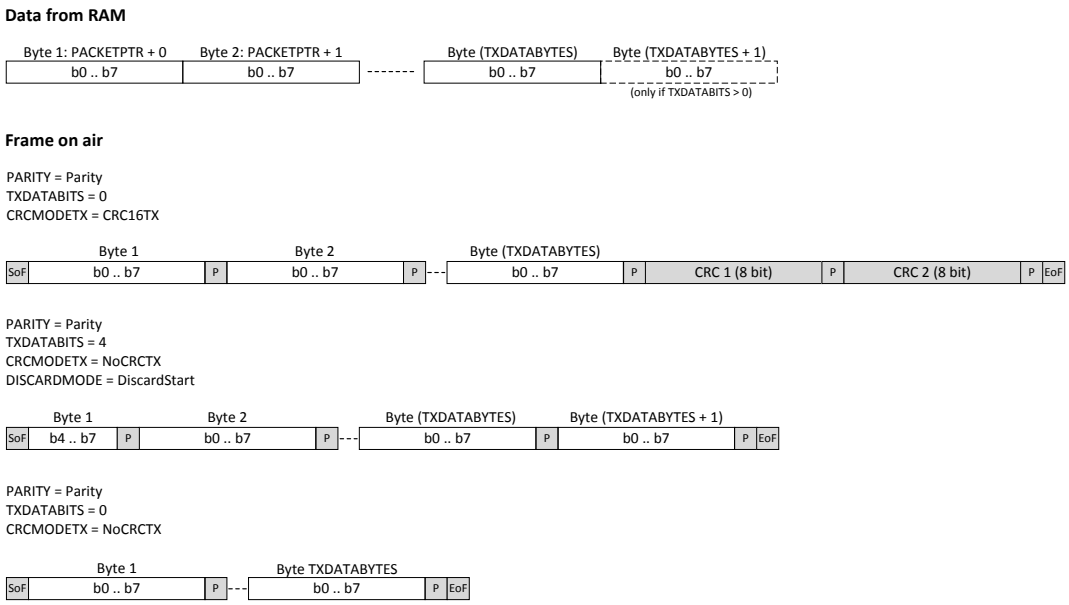



**Figure 130: Frame assemble illustration**

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

## 41.6 Frame disassembler

The NFCT peripheral implements a frame disassembler in hardware.

When the NFCT peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For TX, see *Frame assembler* on page 481. For RX, the software must indicate the address and size of the destination buffer in Data RAM through programming the *PACKETPTR* and MAXLEN registers before issuing an *ENABLERXDATA* task.

The *STARTED* event indicates that the PACKETPTR and MAXLEN registers have been captured by the frame disassembler EasyDMA.

When an incoming frame starts, the *RXFRAMESTART* event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove any parity bits, start of frame (SoF) and end of frame (EoF) symbols on the fly based on *RXD.FRAMECONFIG* register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is enabled through RXD.FRAMECONFIG.

When an EoF symbol is detected, the NFCT peripheral will assert the *RXFRAMEEND* event and write the *RXD.AMOUNT* register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity, and CRC checking, as described above. The frame disassemble operation is illustrated below.

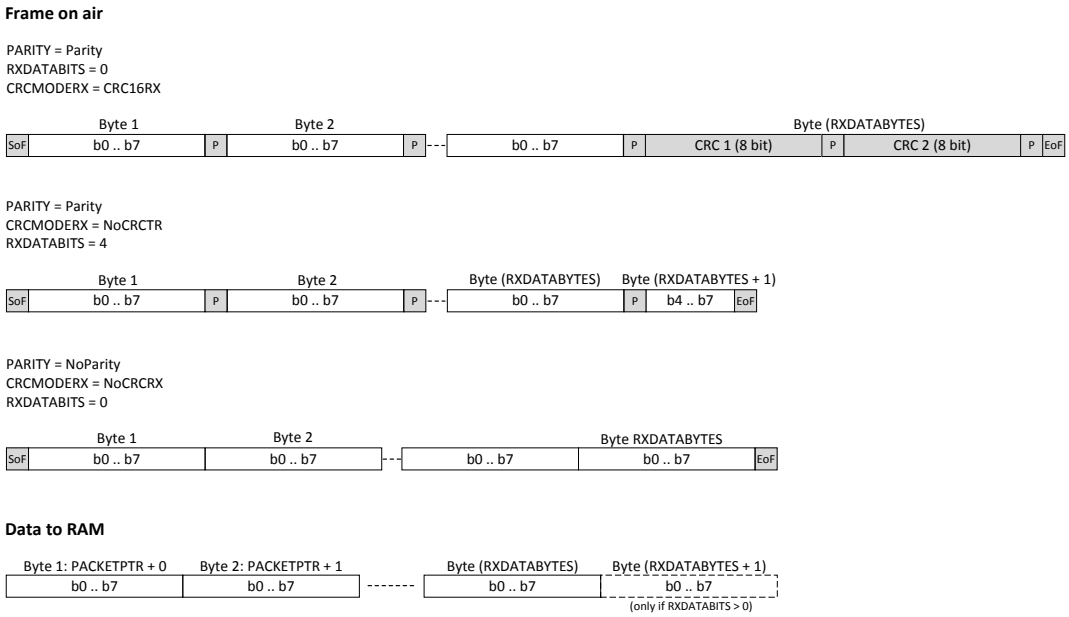



**Figure 131: Frame disassemble illustration**

Per NFC specification, the time between EoF to the next SoF can be as short as 86 µs, and thefore care must be taken that PACKETPTR and MAXLEN are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from *TXFRAMEEND* to ENABLERXDATA is recommended.

## 41.7 Frame timing controller

The NFCT peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF carrier clock periods since the end of the EoF of the last received frame.

The NFCT peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of *FRAMEDELAYMODE* = Window, a *STARTTX* task triggered before the frame timing controller counter is equal to *FRAMEDELAYMIN* will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and *FRAMEDELAYMAX* when the STARTTX task is triggered, the NFCT peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task triggered before the frame delay counter is equal to FRAMEDELAYMAX will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

An *ERROR* event (with FRAMEDELAYTIMEOUT cause in *ERRORSTATUS*) will be asserted if the frame timing controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum, NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS). The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour.

The frame timing controller operation is illustrated in *Figure 132: Frame timing controller (FRAMEDELAYMODE=Window)* on page 484. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.

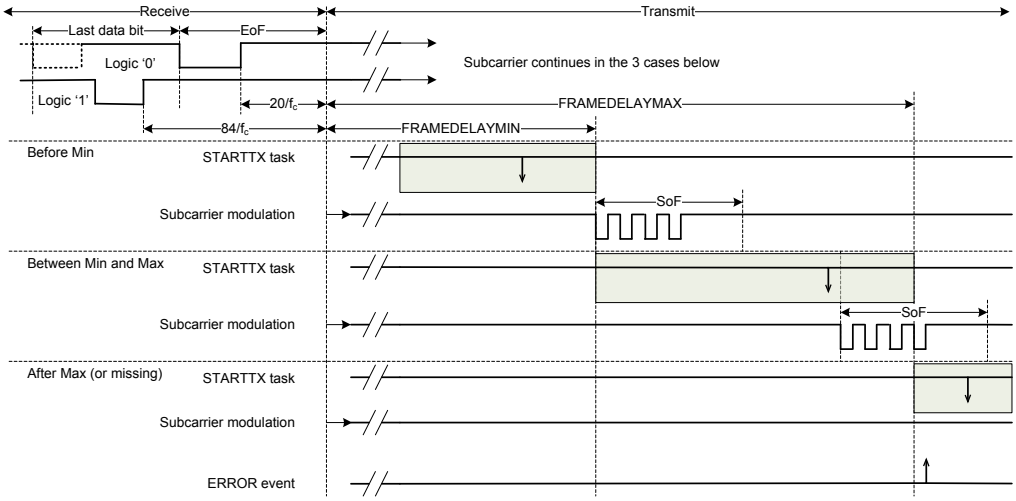



**Figure 132: Frame timing controller (FRAMEDELAYMODE=Window)**

## 41.8 Collision resolution

The NFCT peripheral implements an automatic collision resolution function as defined by the NFC Forum.

Automatic collision resolution is enabled by default, and it is recommended that the feature is used since it is power efficient and reduces the complexity of software handling the collision resolution sequence. This feature can be disabled through the MODE field in the *AUTOCOLRESCONFIG* register. When the automatic collision resolution is disabled, all commands will be sent over EasyDMA as defined in frame disassembler.

The *SENSRES* and *SELRES* registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1_LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR* and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST registers.

*Table 90: NFCID1 byte allocation (top sent first on air)* on page 484 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the *NFC Forum, NFC Digital Protocol Technical Specification*.

**Table 90: NFCID1 byte allocation (top sent first on air)**

| | ID = 4 bytes | ID = 7 bytes | ID = 10 bytes |
|---|---|---|---|
| NFCID1_Q | | | $nfcid1_0$ |
| NFCID1_R | | | $nfcid1_1$ |
| NFCID1_S | | | $nfcid1_2$ |
| NFCID1_T | | $nfcid1_0$ | $nfcid1_3$ |
| NFCID1_U | | $nfcid1_1$ | $nfcid1_4$ |
| NFCID1_V | | $nfcid1_2$ | $nfcid1_5$ |
| NFCID1_W | $nfcid1_0$ | $nfcid1_3$ | $nfcid1_6$ |
| NFCID1_X | $nfcid1_1$ | $nfcid1_4$ | $nfcid1_7$ |
| NFCID1_Y | $nfcid1_2$ | $nfcid1_5$ | $nfcid1_8$ |
| NFCID1_Z | $nfcid1_3$ | $nfcid1_6$ | $nfcid1_9$ |

The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an

*AUTOCOLRESSTARTED* event when it has started. Reaching the ACTIVE_A state is indicated by the *SELECTED* event.

If collision resolution fails, a *COLLISION* event is triggered. Note that errors occurring during automatic collision resolution may also cause *ERROR* and/or *RXERROR* events to be generated. Other events may also get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut is disabled during automatic collision resolution.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE_A state. The automatic collision resolution feature can be disabled while in ACTIVE_A state to avoid this.

The SLP_REQ is automatically handled by the NFCT peripheral when the automatic collision resolution is enabled. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.

## 41.9 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the $V_{swing}$ limit.

Refer to *NFCT Electrical Specification* on page 498.

## 41.10 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between **NFC1** and **NFC2** pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

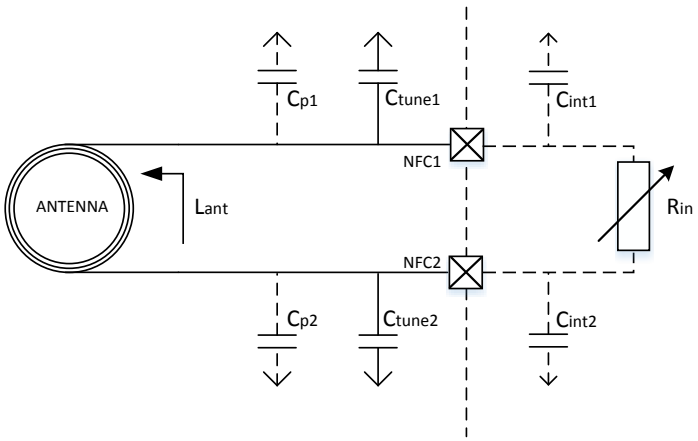



**Figure 133: NFCT antenna recommendations**

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} \quad where\ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{\text{int}} + C_{tune})$$

$$and\ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{\text{int1}} = C_{\text{int2}} = C_{\text{int}}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{\text{int}}$$

An antenna inductance of $L_{ant}$ = 2 µH will give tuning capacitors in the range of 130 pF on each pin. The total capacitance on **NFC1** and **NFC2** must be matched.

## 41.11 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

## 41.12 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

## 41.13 Registers

### Table 91: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40005000 | NFCT | NFCT | Near field communication tag | |

### Table 92: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_ACTIVATE | 0x000 | Activate NFCT peripheral for incoming and outgoing frames, change state to activated |
| TASKS_DISABLE | 0x004 | Disable NFCT peripheral |
| TASKS_SENSE | 0x008 | Enable NFC sense field mode, change state to sense mode |
| TASKS_STARTTX | 0x00C | Start transmission of an outgoing frame, change state to transmit |
| TASKS_ENABLERXDATA | 0x01C | Initializes the EasyDMA for receive. |
| TASKS_GOIDLE | 0x024 | Force state machine to IDLE state |
| TASKS_GOSLEEP | 0x028 | Force state machine to SLEEP_A state |
| EVENTS_READY | 0x100 | The NFCT peripheral is ready to receive and send frames |
| EVENTS_FIELDDETECTED | 0x104 | Remote NFC field detected |
| EVENTS_FIELDLOST | 0x108 | Remote NFC field lost |
| EVENTS_TXFRAMESTART | 0x10C | Marks the start of the first symbol of a transmitted frame |
| EVENTS_TXFRAMEEND | 0x110 | Marks the end of the last transmitted on-air symbol of a frame |
| EVENTS_RXFRAMESTART | 0x114 | Marks the end of the first symbol of a received frame |
| EVENTS_RXFRAMEEND | 0x118 | Received data has been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended accessing the RX buffer |
| EVENTS_ERROR | 0x11C | NFC error reported. The ERRORSTATUS register contains details on the source of the error. |

| Register | Offset | Description |
|---|---|---|
| EVENTS_RXERROR | 0x128 | NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the error. |
| EVENTS_ENDRX | 0x12C | RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full. |
| EVENTS_ENDTX | 0x130 | Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer |
| EVENTS_AUTOCOLRESST | 0x138 | Auto collision resolution process has started |
| EVENTS_COLLISION | 0x148 | NFC auto collision resolution error reported. |
| EVENTS_SELECTED | 0x14C | NFC auto collision resolution successfully completed |
| EVENTS_STARTED | 0x150 | EasyDMA is ready to receive or send frames. |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSTATUS* | 0x404 | NFC Error Status register |
| *FRAMESTATUS.RX* | 0x40C | Result of last incoming frame |
| *NFCTAGSTATE* | 0x410 | NfcTag state register |
| *FIELDPRESENT* | 0x43C | Indicates the presence or not of a valid field |
| *FRAMEDELAYMIN* | 0x504 | Minimum frame delay |
| *FRAMEDELAYMAX* | 0x508 | Maximum frame delay |
| *FRAMEDELAYMODE* | 0x50C | Configuration register for the Frame Delay Timer |
| *PACKETPTR* | 0x510 | Packet pointer for TXD and RXD data storage in Data RAM |
| *MAXLEN* | 0x514 | Size of the RAM buffer allocated to TXD and RXD data storage each |
| *TXD.FRAMECONFIG* | 0x518 | Configuration of outgoing frames |
| *TXD.AMOUNT* | 0x51C | Size of outgoing frame |
| *RXD.FRAMECONFIG* | 0x520 | Configuration of incoming frames |
| *RXD.AMOUNT* | 0x524 | Size of last incoming frame |
| *NFCID1_LAST* | 0x590 | Last NFCID1 part (4, 7 or 10 bytes ID) |
| *NFCID1_2ND_LAST* | 0x594 | Second last NFCID1 part (7 or 10 bytes ID) |
| *NFCID1_3RD_LAST* | 0x598 | Third last NFCID1 part (10 bytes ID) |
| *AUTOCOLRESCONFIG* | 0x59C | Controls the auto collision resolution function. This setting must be done before the NFCT peripheral is enabled. |
| *SENSRES* | 0x5A0 | NFC-A SENS_RES auto-response settings |
| *SELRES* | 0x5A4 | NFC-A SEL_RES auto-response settings |

## 41.13.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | F | | | | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | FIELDDETECTED_ACTIVATE | | | Shortcut between FIELDDETECTED event and ACTIVATE task<br><br>See *EVENTS_FIELDDETECTED* and *TASKS_ACTIVATE* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | FIELDLOST_SENSE | | | Shortcut between FIELDLOST event and SENSE task<br><br>See *EVENTS_FIELDLOST* and *TASKS_SENSE* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| F | RW | TXFRAMEEND_ENABLERXD | | | Shortcut between TXFRAMEEND event and ENABLERXDATA task<br><br>See *EVENTS_TXFRAMEEND* and *TASKS_ENABLERXDATA* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 41.13.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | FIELDDETECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | FIELDLOST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | TXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | RXERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | ENDTX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | AUTOCOLRESSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | COLLISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COLLISION* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SELECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_SELECTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | FIELDDETECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_FIELDDETECTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | FIELDLOST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_FIELDLOST* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | TXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXFRAMESTART* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_TXFRAMEEND* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXFRAMESTART* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXFRAMEEND* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ERROR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | RXERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_RXERROR* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDRX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | ENDTX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDTX* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | AUTOCOLRESSTARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_AUTOCOLRESSTARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | COLLISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_COLLISION* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SELECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_SELECTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.4 INTENCLR

Address offset: 0x308

## Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | FIELDDETECTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | FIELDLOST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | TXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | TXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RXFRAMESTART | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RXFRAMEEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | RXERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | ENDRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | T | S | R | | | | N | | M | L | K | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| M | RW | ENDTX | | | Write '1' to Disable interrupt for ENDTX event<br>See *EVENTS_ENDTX* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| N | RW | AUTOCOLRESSTARTED | | | Write '1' to Disable interrupt for AUTOCOLRESSTARTED event<br>See *EVENTS_AUTOCOLRESSTARTED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| R | RW | COLLISION | | | Write '1' to Disable interrupt for COLLISION event<br>See *EVENTS_COLLISION* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| S | RW | SELECTED | | | Write '1' to Disable interrupt for SELECTED event<br>See *EVENTS_SELECTED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| T | RW | STARTED | | | Write '1' to Disable interrupt for STARTED event<br>See *EVENTS_STARTED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 41.13.5 ERRORSTATUS

Address offset: 0x404

NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | FRAMEDELAYTIMEOUT | | | No STARTTX task triggered before expiration of the time set in FRAMEDELAYMAX |

## 41.13.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frame

Write a bit to '1' to clear it. Writing '0' has no effect.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CRCERROR | | | No valid end of frame (EoF) detected |
| | | | CRCCorrect | 0 | Valid CRC detected |
| | | | CRCError | 1 | CRC received does not match local check |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PARITYSTATUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ParityOK | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ParityError | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | OVERRUN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoOverrun | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Overrun | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.7 NFCTAGSTATE

Address offset: 0x410

NfcTag state register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | NFCTAGSTATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RampUp | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Idle | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Receive | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | FrameDelay | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Transmit | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.8 FIELDPRESENT

Address offset: 0x43C

Indicates the presence or not of a valid field

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | FIELDPRESENT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoField | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | FieldPresent | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | LOCKDETECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotLocked | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Locked | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.9 FRAMEDELAYMIN

Address offset: 0x504

Minimum frame delay

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000480** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FRAMEDELAYMIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.10 FRAMEDELAYMAX

Address offset: 0x508

Maximum frame delay

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00001000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FRAMEDELAYMAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Maximum frame delay in number of 13.56 MHz clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FRAMEDELAYMODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configuration register for the Frame Delay Timer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | FreeRun | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Transmission is independent of frame timer and will start when the STARTTX task is triggered. No timeout. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Window | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Frame is transmitted between FRAMEDELAYMIN and FRAMEDELAYMAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ExactVal | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Frame is transmitted exactly at FRAMEDELAYMAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | WindowGrid | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Frame is transmitted on a bit grid between FRAMEDELAYMIN and FRAMEDELAYMAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Packet pointer for TXD and RXD data storage in Data RAM. This address is a byte-aligned RAM address. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.13 MAXLEN

Address offset: 0x514

Size of the RAM buffer allocated to TXD and RXD data storage each

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MAXLEN | | [0..257] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Size of the RAM buffer allocated to TXD and RXD data storage each | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | | C | B | A |
| **Reset 0x00000017** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Indicates if parity is added to the frame | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | | C | B | A |
| **Reset 0x00000017** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoParity | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Parity | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | DISCARDMODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DiscardEnd | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DiscardStart | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoSoF | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SoF | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | CRCMODETX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoCRCTX | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CRC16TX | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.15 TXD.AMOUNT

Address offset: 0x51C

Size of outgoing frame

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | B | B | B | B | B | B | B | B | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TXDATABITS | | [0..7] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Number of bits in the last or first byte read from RAM that shall be included in the frame (excluding parity bit). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | The DISCARDMODE field in FRAMECONFIG.TX selects if unused bits is discarded at the start or at the end of a frame. A value of 0 data bytes and 0 data bits is invalid. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | TXDATABYTES | | [0..257] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Number of complete bytes that shall be included in the frame, excluding CRC, parity and framing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | | B | | A |
| **Reset 0x00000015** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoParity | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Parity | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoSoF | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | SoF | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CRCMODERX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoCRCRX | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | CRC16RX | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Last 16 bits in RX frame is CRC, CRC is checked and CRCSTATUS updated | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | B | B | B | B | B | B | B | B | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXDATABITS | | | | | | | | | | Number of bits in the last byte in the frame, if less than 8 (including CRC, but excluding parity and SoF/EoF framing).<br>Frames with 0 data bytes and less than 7 data bits are invalid and are not received properly. | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | RXDATABYTES | | | | | | | | | | Number of complete bytes received in the frame (including CRC, but excluding parity and SoF/EoF framing) | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00006363** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NFCID1_Z | | | | | | | | | | NFCID1 byte Z (very last byte sent) | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NFCID1_Y | | | | | | | | | | NFCID1 byte Y | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | NFCID1_X | | | | | | | | | | NFCID1 byte X | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | NFCID1_W | | | | | | | | | | NFCID1 byte W | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NFCID1_V | | | | | | | | | | NFCID1 byte V | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NFCID1_U | | | | | | | | | | NFCID1 byte U | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | NFCID1_T | | | | | | | | | | NFCID1 byte T | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | NFCID1_S | | | | | | | | | | NFCID1 byte S | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NFCID1_R | | | | | | | | | | NFCID1 byte R | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | NFCID1_Q | | | | | | | | | | NFCID1 byte Q | | | | | | | | | | | | | | | | | | | | | | | |

## 41.13.21 AUTOCOLRESCONFIG

Address offset: 0x59C

Controls the auto collision resolution function. This setting must be done before the NFCT peripheral is enabled.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000002** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enables/disables auto collision resolution |
| | | | Enabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Auto collision resolution enabled |
| | | | Disabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Auto collision resolution disabled |

## 41.13.22 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | E | E | E | E | D | D | D | D | C | C | B | A | A | A | A | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | BITFRAMESDD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Bit frame SDD as defined by the b5:b1 of byte 1 in SENS_RES response in the NFC Forum, NFC Digital Protocol Technical Specification |
| | | | SDD00000 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 00000 |
| | | | SDD00001 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 00001 |
| | | | SDD00010 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 00010 |
| | | | SDD00100 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 00100 |
| | | | SDD01000 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 01000 |
| | | | SDD10000 | 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SDD pattern 10000 |
| B | RW | RFU5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reserved for future use. Shall be 0. |
| C | RW | NFCIDSIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | NFCID1 size. This value is used by the auto collision resolution engine. |
| | | | NFCID1Single | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | NFCID1 size: single (4 bytes) |
| | | | NFCID1Double | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | NFCID1 size: double (7 bytes) |
| | | | NFCID1Triple | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | NFCID1 size: triple (10 bytes) |
| D | RW | PLATFCONFIG | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Tag platform configuration as defined by the b4:b1 of byte 2 in SENS_RES response in the NFC Forum, NFC Digital Protocol Technical Specification |
| E | RW | RFU74 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reserved for future use. Shall be 0. |

## 41.13.23 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | D | C | C | B | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | RFU10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reserved for future use. Shall be 0. |
| B | RW | CASCADE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Cascade as defined by the b3 of SEL_RES response in the NFC Forum, NFC Digital Protocol Technical Specification (controlled by hardware, shall be 0) |
| C | RW | RFU43 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reserved for future use. Shall be 0. |
| D | RW | PROTOCOL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Protocol as defined by the b7:b6 of SEL_RES response in the NFC Forum, NFC Digital Protocol Technical Specification |
| E | RW | RFU7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Reserved for future use. Shall be 0. |

# 41.14 Electrical specification

## 41.14.1 NFCT Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_c$ | Frequency of operation | | 13.56 | | MHz |
| $C_{MI}$ | Carrier modulation index | 95 | | | % |
| DR | Data Rate | | 106 | | kbps |
| $V_{sense}$ | Peak differential Field detect threshold level on NFC1-NFC2[32] | | 0.59 | | Vp |
| $I_{sense}$ | Current in SENSE STATE[33] | | 100 | | nA |
| $I_{activated}$ | Current in ACTIVATED STATE | | 400 | | µA |
| $I_{max}$ | Maximum input current on NFCT pins | | | 80 | mA |

## 41.14.2 NFCT Timing Parameters

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{activate}$ | Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state[34] | | | 500 | µs |
| $t_{sense}$ | Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted | | | 20 | µs |

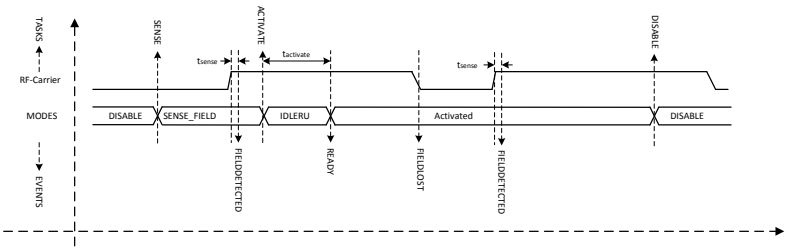



**Figure 134: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)**

[32] Input is high impedance in sense mode
[33] This current does not apply when in NFC field
[34] Does not account for voltage supply and oscillator startup times

# 42 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters
- Selectable ratio of 64 or 80 between PDM_CLK and output sample rate

The PDM module illustrated in *Figure 135: PDM module* on page 499 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

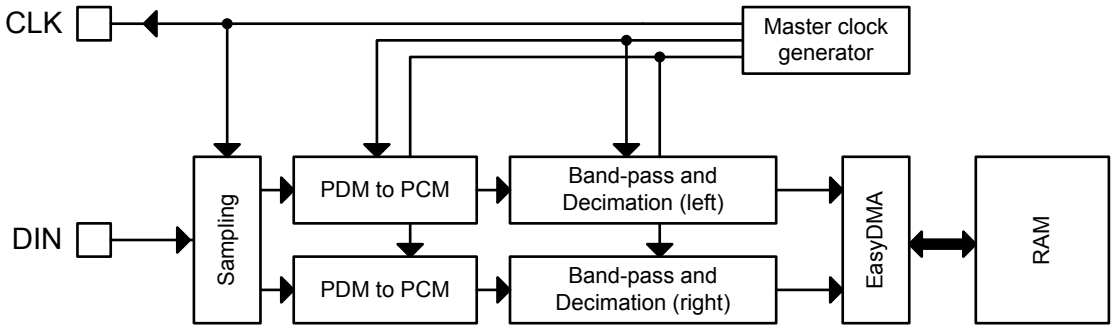



**Figure 135: PDM module**

## 42.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

## 42.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

## 42.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low). Depending on the RATIO selected, its output is 2 × 16-bit PCM samples at a sample rate either 64 times or 80 times (depending on the RATIO register) lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain ( $G_{PDM,default}$ ) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to $-G_{PDM,default}$ dB to achieve the requirement.

With $G_{PDM,default}$=3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

## 42.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

**Table 93: DMA sample storage**

| MODE.OPERATION | Bits per sample | Result stored per RAM word | Physical RAM allocated (32 bit words) | Result boundary indexes in RAM | Note |
|---|---|---|---|---|---|
| Stereo | 32 (2x16) | L+R | ceil(SAMPLE.MAXCNT/2) | R0=[31:16]; L0=[15:0] | Default |
| Mono | 16 | 2xL | ceil(SAMPLE.MAXCNT/2) | L1=[31:16]; L0=[15:0] | |

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.

For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

## 42.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.

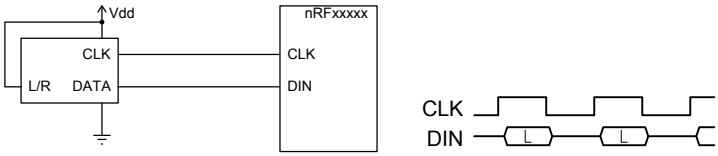



**Figure 136: Example of a single PDM microphone, wired as left**

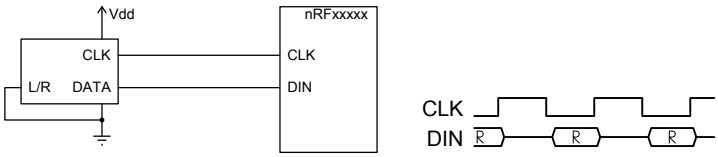



**Figure 137: Example of a single PDM microphone, wired as right**

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

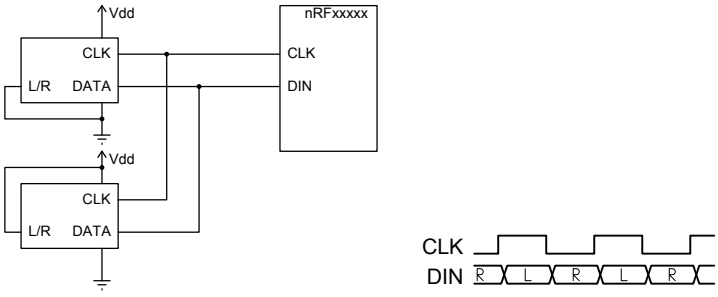



**Figure 138: Example of two PDM microphones**

## 42.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.

The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER — Power supply* on page 66 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 94: GPIO configuration before enabling peripheral* on page 502 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

**Table 94: GPIO configuration before enabling peripheral**

| PDM signal | PDM pin | Direction | Output value | Comment |
|---|---|---|---|---|
| CLK | As specified in PSEL.CLK | Output | 0 | |
| DIN | As specified in PSEL.DIN | Input | Not applicable | |

## 42.7 Registers

**Table 95: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4001D000 | PDM | PDM | Pulse Density modulation (digital microphone) interface | |

**Table 96: Register Overview**

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Starts continuous PDM transfer |
| TASKS_STOP | 0x004 | Stops PDM transfer |
| EVENTS_STARTED | 0x100 | PDM transfer has started |
| EVENTS_STOPPED | 0x104 | PDM transfer has finished |
| EVENTS_END | 0x108 | The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP task has been received) to Data RAM |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | PDM module enable register |
| *PDMCLKCTRL* | 0x504 | PDM clock generator control |
| *MODE* | 0x508 | Defines the routing of the connected PDM microphones' signals |
| *GAINL* | 0x518 | Left output gain adjustment |
| *GAINR* | 0x51C | Right output gain adjustment |
| *RATIO* | 0x520 | Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly. |
| *PSEL.CLK* | 0x540 | Pin number configuration for PDM CLK signal |
| *PSEL.DIN* | 0x544 | Pin number configuration for PDM DIN signal |
| *SAMPLE.PTR* | 0x560 | RAM address pointer to write samples to with EasyDMA |
| *SAMPLE.MAXCNT* | 0x564 | Number of samples to allocate memory for in EasyDMA mode |

### 42.7.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_STOPPED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | END | | | Write '1' to Disable interrupt for END event |
| | | | | | See *EVENTS_END* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 42.7.4 ENABLE

Address offset: 0x500

PDM module enable register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ENABLE | | | Enable or disable PDM module |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

### 42.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x08400000** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | FREQ | | | PDM_CLK frequency |
| | | | 1000K | 0x08000000 | PDM_CLK = 32 MHz / 32 = 1.000 MHz |
| | | | Default | 0x08400000 | PDM_CLK = 32 MHz / 31 = 1.032 MHz. Nominal clock for RATIO=Ratio64. |
| | | | 1067K | 0x08800000 | PDM_CLK = 32 MHz / 30 = 1.067 MHz |
| | | | 1231K | 0x09800000 | PDM_CLK = 32 MHz / 26 = 1.231 MHz |
| | | | 1280K | 0x0A000000 | PDM_CLK = 32 MHz / 25 = 1.280 MHz. Nominal clock for RATIO=Ratio80. |
| | | | 1333K | 0x0A800000 | PDM_CLK = 32 MHz / 24 = 1.333 MHz |

### 42.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | OPERATION | | | Mono or stereo operation |
| | | | Stereo | 0 | Sample and store one pair (Left + Right) of 16bit samples per RAM word R=[31:16]; L=[15:0] |

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | Mono | | | | | | | | 1 | | | | | | | | | | | | | | | | | Sample and store two successive Left samples (16 bit each) per RAM word L1=[31:16]; L0=[15:0] | | | | | | | |
| B | RW | EDGE | | | | | | | | | | | | | | | | | | | | | | | | | | Defines on which PDM_CLK edge Left (or mono) is sampled | | | | | | | |
| | | | LeftFalling | | | | | | | | 0 | | | | | | | | | | | | | | | | | Left (or mono) is sampled on falling edge of PDM_CLK | | | | | | | |
| | | | LeftRising | | | | | | | | 1 | | | | | | | | | | | | | | | | | Left (or mono) is sampled on rising edge of PDM_CLK | | | | | | | |

## 42.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000028** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | GAINL | | | | | | | | | | | | | | | | | | | | | | | | | | Left output gain adjustment, in 0.5 dB steps, around the default module gain (see electrical parameters) | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x00 -20 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x01 -19.5 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | (...) | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x27 -0.5 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x28 0 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x29 +0.5 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | (...) | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x4F +19.5 dB gain adjust | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x50 +20 dB gain adjust | | | | | | | |
| | | | MinGain | | | | | | | | 0x00 | | | | | | | | | | | | | | | | | -20dB gain adjustment (minimum) | | | | | | | |
| | | | DefaultGain | | | | | | | | 0x28 | | | | | | | | | | | | | | | | | 0dB gain adjustment ('2500 RMS' requirement) | | | | | | | |
| | | | MaxGain | | | | | | | | 0x50 | | | | | | | | | | | | | | | | | +20dB gain adjustment (maximum) | | | | | | | |

## 42.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000028** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | GAINR | | | | | | | | | | | | | | | | | | | | | | | | | | Right output gain adjustment, in 0.5 dB steps, around the default module gain (see electrical parameters) | | | | | | | |
| | | | MinGain | | | | | | | | 0x00 | | | | | | | | | | | | | | | | | -20dB gain adjustment (minimum) | | | | | | | |
| | | | DefaultGain | | | | | | | | 0x28 | | | | | | | | | | | | | | | | | 0dB gain adjustment ('2500 RMS' requirement) | | | | | | | |
| | | | MaxGain | | | | | | | | 0x50 | | | | | | | | | | | | | | | | | +20dB gain adjustment (maximum) | | | | | | | |

## 42.7.9 RATIO

Address offset: 0x520

Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RATIO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ratio64 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ratio80 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.10 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.11 PSEL.DIN

Address offset: 0x544

Pin number configuration for PDM DIN signal

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.12 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SAMPLEPTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 42.7.13 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BUFFSIZE | | [0..32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 42.8 Electrical specification

## 42.8.1 PDM Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{PDM,stereo}$ | PDM module active current, stereo operation[35] | | 250 | | µA |
| $f_{PDM,CLK,64}$ | PDM clock speed, RATIO of 64 | | 1.032 | | MHz |
| $f_{PDM,CLK,80}$ | PDM clock speed, RATIO of 80 | .. | .. | .. | MHz |
| $t_{PDM,JITTER}$ | Jitter in PDM clock output | | | 20 | ns |
| $T_{dPDM,CLK}$ | PDM clock duty cycle | 40 | 50 | 60 | % |
| $t_{PDM,DATA}$ | Decimation filter delay | | | 5 | ms |
| $t_{PDM,cv}$ | Allowed clock edge to data valid | | | 125 | ns |
| $t_{PDM,ci}$ | Allowed (other) clock edge to data invalid | 0 | | | ns |
| $t_{PDM,s}$ | Data setup time at $f_{PDM,CLK}$=1.024 MHz or 1.280 MHz | 65 | | | ns |
| $t_{PDM,h}$ | Data hold time at $f_{PDM,CLK}$=1.024 MHz or 1.280 MHz | 0 | | | ns |
| $G_{PDM,default}$ | Default (reset) absolute gain of the PDM module | | 3.2 | | dB |

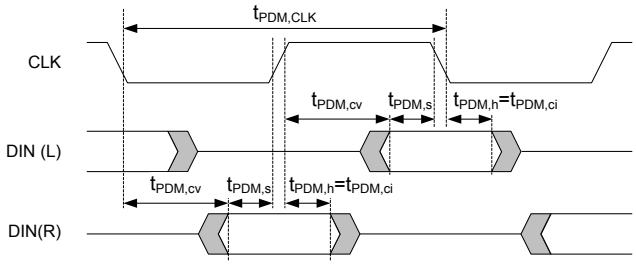



**Figure 139: PDM timing diagram**

[35] Average current including PDM and DMA transfers, excluding clock and power supply base currents

# 43 I2S — Inter-IC sound interface

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I2S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

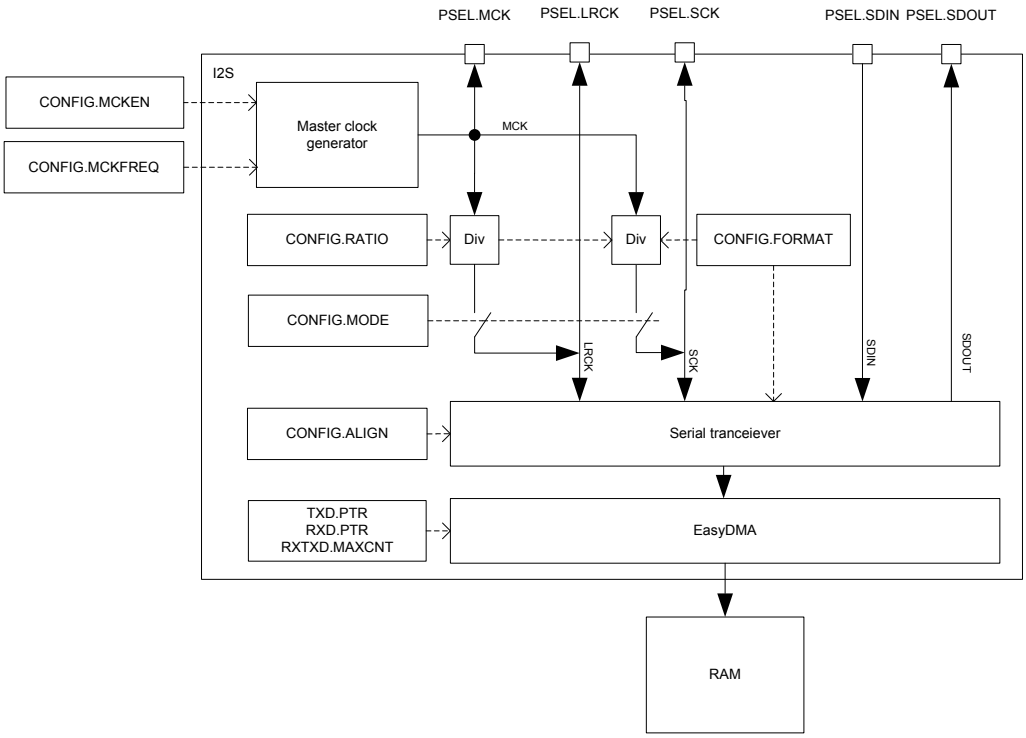



**Figure 140: I2S master**

## 43.1 Mode

The I2S protocol specification defines two modes of operation, Master and Slave.

The I2S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

## 43.2 Transmitting and receiving

The I2S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.

TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the *CONFIG.TXEN* on page 518 and *CONFIG.RXEN* on page 518.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in *CONFIG.TXEN* on page 518), the TXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 521 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in *CONFIG.RXEN* on page 518), the RXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 521 received data words.

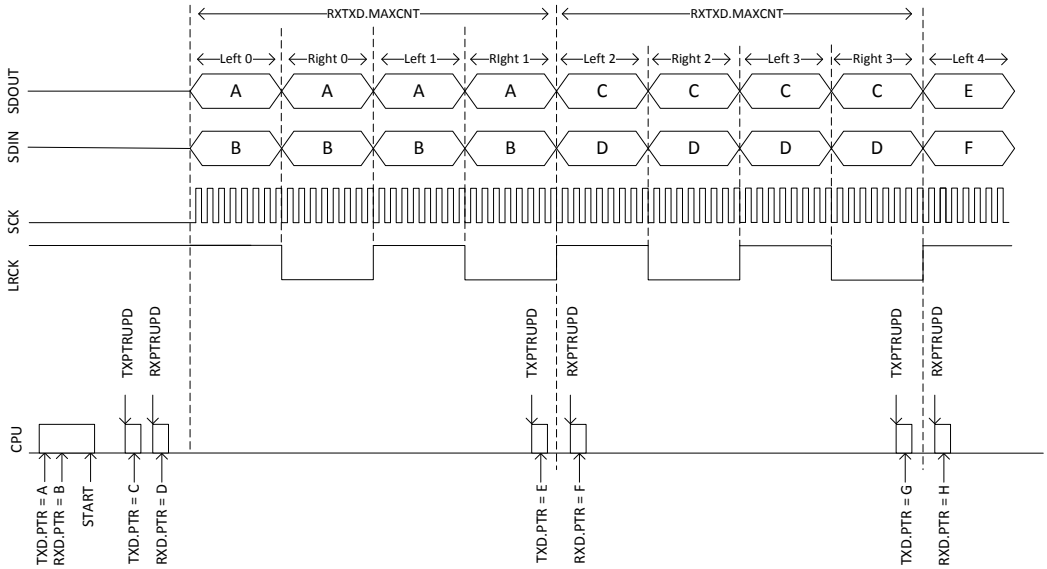



**Figure 141: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.**

## 43.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I2S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

## 43.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.

When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I2S master.

## 43.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register *CONFIG.MCKEN* on page 519, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through *CONFIG.RATIO* on page 519 and *CONFIG.SWIDTH* on page 520.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I2S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I2S module does not use the MCK and the MCK generator does not need to be enabled.

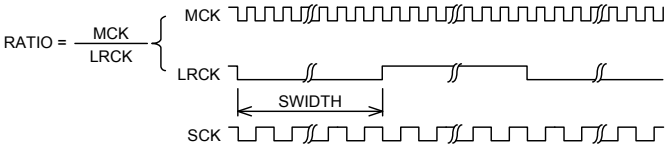



**Figure 142: Relation between RATIO, MCK and LRCK.**

**Table 97: Configuration examples**

| Desired LRCK [Hz] | CONFIG.SWIDTH | CONFIG.RATIO | CONFIG.MCKFREQ | MCK [Hz] | LRCK [Hz] | LRCK error [%] |
|---|---|---|---|---|---|---|
| 16000 | 16Bit | 32X | 32MDIV63 | 507936.5 | 15873.0 | -0.8 |
| 16000 | 16Bit | 64X | 32MDIV31 | 1032258.1 | 16129.0 | 0.8 |
| 16000 | 16Bit | 256X | 32MDIV8 | 4000000.0 | 15625.0 | -2.3 |
| 32000 | 16Bit | 32X | 32MDIV31 | 1032258.1 | 32258.1 | 0.8 |
| 32000 | 16Bit | 64X | 32MDIV16 | 2000000.0 | 31250.0 | -2.3 |
| 32000 | 16Bit | 256X | 32MDIV4 | 8000000.0 | 31250.0 | -2.3 |
| 44100 | 16Bit | 32X | 32MDIV23 | 1391304.3 | 43478.3 | -1.4 |
| 44100 | 16Bit | 64X | 32MDIV11 | 2909090.9 | 45454.5 | 3.1 |
| 44100 | 16Bit | 256X | 32MDIV3 | 10666666.7 | 41666.7 | -5.5 |

## 43.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.

When using I2S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in *CONFIG.ALIGN* on page 520. *CONFIG.ALIGN* on page 520 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in *CONFIG.SWIDTH* requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for left-alignment).

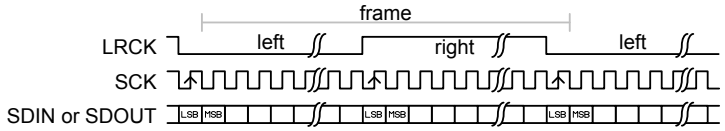



**Figure 143: I2S format. CONFIG.SWIDTH equalling half-frame size.**

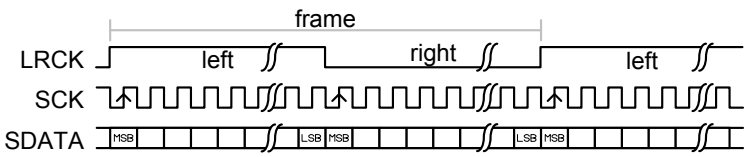



**Figure 144: Aligned format. CONFIG.SWIDTH equalling half-frame size.**

## 43.7 EasyDMA

The I2S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in *TXD.PTR* on page 521 and *RXD.PTR* on page 521. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in *CONFIG.TXEN* on page 518 and *CONFIG.RXEN* on page 518.

The addresses written to the pointer registers *TXD.PTR* on page 521 and *RXD.PTR* on page 521 are double-buffered in hardware, and these double buffers are updated for every *RXTXD.MAXCNT* on page 521 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If *TXD.PTR* on page 521 is not pointing to the Data RAM region when transmission is enabled, or *RXD.PTR* on page 521 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 20 for more information about the different memory regions.

Due to the nature of I2S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register *RXTXD.MAXCNT* on page 521 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (CONFIG.CHANNELS=Stereo), the samples are stored as "left and right sample pairs" in memory. Figure *Figure 145: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.* on page 512, *Figure 147: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.* on page 513 and *Figure 149: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.* on page 513 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In mono mode (CONFIG.CHANNELS=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Illustrations *Figure 146: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.* on page 513, *Figure 148: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.* on page 513 and *Figure 150: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.* on page 514 show how RX samples are mapped to memory in this mode.

For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

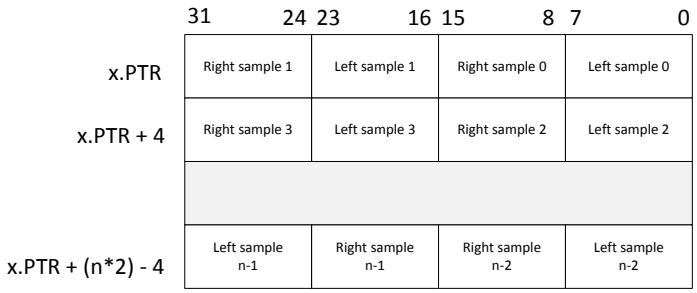



**Figure 145: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.**

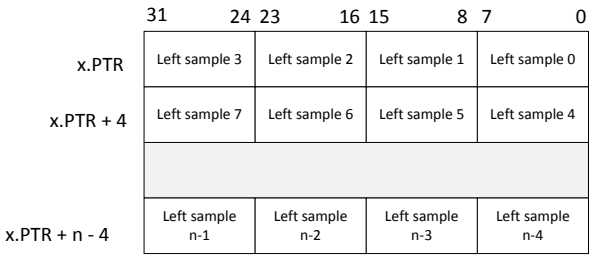



**Figure 146: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.**

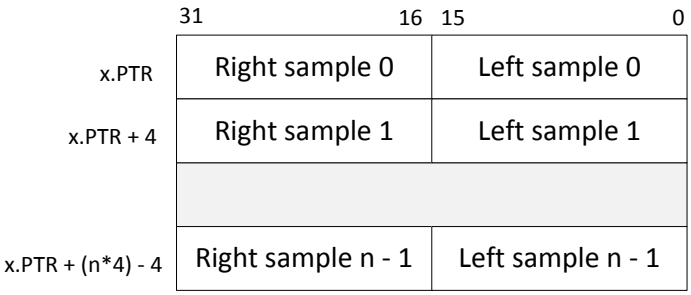



**Figure 147: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.**

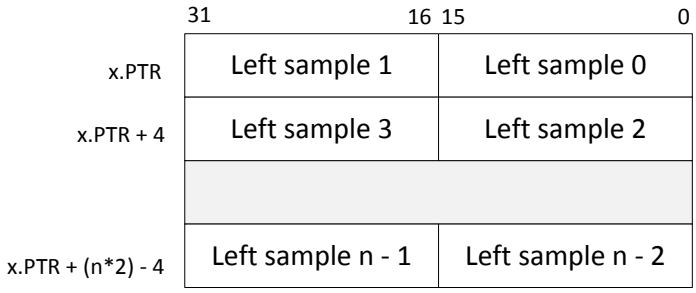



**Figure 148: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.**

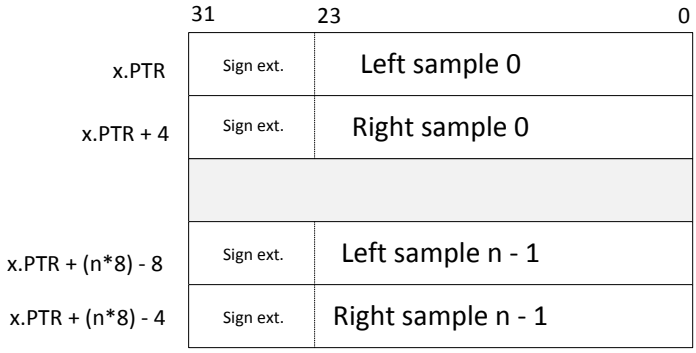



**Figure 149: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.**

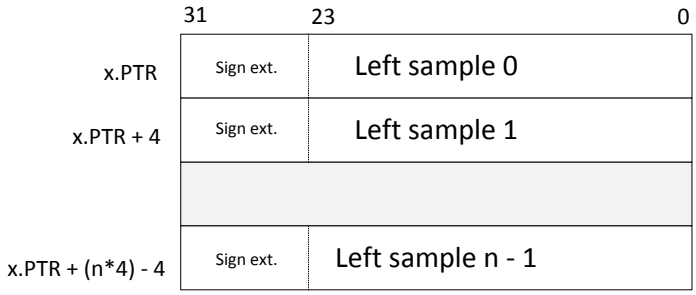



**Figure 150: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.**

## 43.8 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
// Enable reception
NRF_I2S->CONFIG.RXEN = (I2S_CONFIG_RXEN_RXEN_Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF_I2S->CONFIG.TXEN = (I2S_CONFIG_TXEN_TXEN_Enabled <<
                                        I2S_CONFIG_TXEN_TXEN_Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<
                                        I2S_CONFIG_MCKEN_MCKEN_Pos);
// MCKFREQ = 4 MHz
NRF_I2S->CONFIG.MCKFREQ = I2S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        I2S_CONFIG_MCKFREQ_MCKFREQ_Pos;
// Ratio = 256
NRF_I2S->CONFIG.RATIO = I2S_CONFIG_RATIO_RATIO_256X <<
                                        I2S_CONFIG_RATIO_RATIO_Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF_I2S->CONFIG.SWIDTH = I2S_CONFIG_SWIDTH_SWIDTH_16Bit <<
                                        I2S_CONFIG_SWIDTH_SWIDTH_Pos;
// Alignment = Left
NRF_I2S->CONFIG.ALIGN = I2S_CONFIG_ALIGN_ALIGN_Left <<
                                        I2S_CONFIG_ALIGN_ALIGN_Pos;
// Format = I2S
NRF_I2S->CONFIG.FORMAT = I2S_CONFIG_FORMAT_FORMAT_I2S <<
                                        I2S_CONFIG_FORMAT_FORMAT_Pos;
// Use stereo
NRF_I2S->CONFIG.CHANNELS = I2S_CONFIG_CHANNELS_CHANNELS_Stereo <<
                                        I2S_CONFIG_CHANNELS_CHANNELS_Pos;
```

2. Map IO pins using the PINSEL registers

```
// MCK routed to pin 0
NRF_I2S->PSEL.MCK = (0 << I2S_PSEL_MCK_PIN_Pos) |
                    (I2S_PSEL_MCK_CONNECT_Connected <<
                                                I2S_PSEL_MCK_CONNECT_Pos);
// SCK routed to pin 1
NRF_I2S->PSEL.SCK = (1 << I2S_PSEL_SCK_PIN_Pos) |
                    (I2S_PSEL_SCK_CONNECT_Connected <<

 I2S_PSEL_SCK_CONNECT_Pos);
// LRCK routed to pin 2
NRF_I2S->PSEL.LRCK = (2 << I2S_PSEL_LRCK_PIN_Pos) |
                     (I2S_PSEL_LRCK_CONNECT_Connected <<
```

```
 I2S_PSEL_LRCK_CONNECT_Pos);
// SDOUT routed to pin 3
NRF_I2S->PSEL.SDOUT = (3 << I2S_PSEL_SDOUT_PIN_Pos) |
                      (I2S_PSEL_SDOUT_CONNECT_Connected <<

 I2S_PSEL_SDOUT_CONNECT_Pos);
// SDIN routed on pin 4
NRF_I2S->PSEL.SDIN = (4 << I2S_PSEL_SDIN_PIN_Pos) |
                     (I2S_PSEL_SDIN_CONNECT_Connected <<

 I2S_PSEL_SDIN_CONNECT_Pos);
```

3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I2S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if(NRF_I2S->EVENTS_TXPTRUPD  != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if(NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

## 43.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I2S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I2S module is enabled through the register *ENABLE* on page 518.

When a pin is acquired by the I2S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I2S pins are shown below in *Table 98: GPIO configuration before enabling peripheral (master mode)* on page 515 and *Table 99: GPIO configuration before enabling peripheral (slave mode)* on page 516.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I2S module is disabled, these pins must be configured in the GPIO peripheral directly.

**Table 98: GPIO configuration before enabling peripheral (master mode)**

| I2S signal | I2S pin | Direction | Output value | Comment |
|---|---|---|---|---|
| MCK | As specified in PSEL.MCK | Output | 0 | |
| LRCK | As specified in PSEL.LRCK | Output | 0 | |

| I²S signal | I²S pin | Direction | Output value | Comment |
|---|---|---|---|---|
| SCK | As specified in PSEL.SCK | Output | 0 | |
| SDIN | As specified in PSEL.SDIN | Input | Not applicable | |
| SDOUT | As specified in PSEL.SDOUT | Output | 0 | |

### Table 99: GPIO configuration before enabling peripheral (slave mode)

| I²S signal | I²S pin | Direction | Output value | Comment |
|---|---|---|---|---|
| MCK | As specified in PSEL.MCK | Output | 0 | |
| LRCK | As specified in PSEL.LRCK | Input | Not applicable | |
| SCK | As specified in PSEL.SCK | Input | Not applicable | |
| SDIN | As specified in PSEL.SDIN | Input | Not applicable | |
| SDOUT | As specified in PSEL.SDOUT | Output | 0 | |

## 43.10 Registers

### Table 100: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40025000 | I2S | I2S | Inter-IC sound interface | |

### Table 101: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_START | 0x000 | Starts continuous I2S transfer. Also starts MCK generator when this is enabled. |
| TASKS_STOP | 0x004 | Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED} event to be generated. |
| EVENTS_RXPTRUPD | 0x104 | The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on the SDIN pin. |
| EVENTS_STOPPED | 0x108 | I2S transfer stopped. |
| EVENTS_TXPTRUPD | 0x114 | The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin. |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | Enable I2S module. |
| *CONFIG.MODE* | 0x504 | I2S mode. |
| *CONFIG.RXEN* | 0x508 | Reception (RX) enable. |
| *CONFIG.TXEN* | 0x50C | Transmission (TX) enable. |
| *CONFIG.MCKEN* | 0x510 | Master clock generator enable. |
| *CONFIG.MCKFREQ* | 0x514 | Master clock generator frequency. |
| *CONFIG.RATIO* | 0x518 | MCK / LRCK ratio. |
| *CONFIG.SWIDTH* | 0x51C | Sample width. |
| *CONFIG.ALIGN* | 0x520 | Alignment of sample within a frame. |
| *CONFIG.FORMAT* | 0x524 | Frame format. |
| *CONFIG.CHANNELS* | 0x528 | Enable channels. |
| *RXD.PTR* | 0x538 | Receive buffer RAM start address. |
| *TXD.PTR* | 0x540 | Transmit buffer RAM start address. |
| *RXTXD.MAXCNT* | 0x550 | Size of RXD and TXD buffers. |
| *PSEL.MCK* | 0x560 | Pin select for MCK signal. |
| *PSEL.SCK* | 0x564 | Pin select for SCK signal. |
| *PSEL.LRCK* | 0x568 | Pin select for LRCK signal. |
| *PSEL.SDIN* | 0x56C | Pin select for SDIN signal. |
| *PSEL.SDOUT* | 0x570 | Pin select for SDOUT signal. |

### 43.10.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RXPTRUPD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | TXPTRUPD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RXPTRUPD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | TXPTRUPD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RXPTRUPD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | See *EVENTS_STOPPED* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | TXPTRUPD | | | | | | | | | | Write '1' to Disable interrupt for TXPTRUPD event<br><br>See *EVENTS_TXPTRUPD* | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.4 ENABLE

Address offset: 0x500

Enable I2S module.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | Enable I2S module. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Enable | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.5 CONFIG.MODE

Address offset: 0x504

I2S mode.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MODE | | | | | | | | | | I2S mode. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Master | 0 | | | | | | | | Master mode. SCK and LRCK generated from internal master clcok (MCK) and output on pins defined by PSEL.xxx. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Slave | 1 | | | | | | | | Slave mode. SCK and LRCK generated by external master and received on pins defined by PSEL.xxx | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.6 CONFIG.RXEN

Address offset: 0x508

Reception (RX) enable.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RXEN | | | | | | | | | | Reception (RX) enable. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Reception disabled and now data will be written to the RXD.PTR address. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Reception enabled. | | | | | | | | | | | | | | | | | | | | | | | |

## 43.10.7 CONFIG.TXEN

Address offset: 0x50C

Transmission (TX) enable.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | TXEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Transmission (TX) enable. |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Transmission disabled and now data will be read from the RXD.TXD address. |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Transmission enabled. |

## 43.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | MCKEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Master clock generator enable. |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Master clock generator disabled and PSEL.MCK not connected(available as GPIO). |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Master clock generator running and MCK output on PSEL.MCK. |

## 43.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x20000000** | | | | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | MCKFREQ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Master clock generator frequency. |
| | | | 32MDIV2 | 0x80000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 2 = 16.0 MHz |
| | | | 32MDIV3 | 0x50000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 3 = 10.6666667 MHz |
| | | | 32MDIV4 | 0x40000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 4 = 8.0 MHz |
| | | | 32MDIV5 | 0x30000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 5 = 6.4 MHz |
| | | | 32MDIV6 | 0x28000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 6 = 5.3333333 MHz |
| | | | 32MDIV8 | 0x20000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 8 = 4.0 MHz |
| | | | 32MDIV10 | 0x18000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 10 = 3.2 MHz |
| | | | 32MDIV11 | 0x16000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 11 = 2.9090909 MHz |
| | | | 32MDIV15 | 0x11000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 15 = 2.1333333 MHz |
| | | | 32MDIV16 | 0x10000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 16 = 2.0 MHz |
| | | | 32MDIV21 | 0x0C000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 21 = 1.5238095 |
| | | | 32MDIV23 | 0x0B000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 23 = 1.3913043 MHz |
| | | | 32MDIV30 | 0x08800000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 30 = 1.0666667 MHz |
| | | | 32MDIV31 | 0x08400000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 31 = 1.0322581 MHz |
| | | | 32MDIV32 | 0x08000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 32 = 1.0 MHz |
| | | | 32MDIV42 | 0x06000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 42 = 0.7619048 MHz |
| | | | 32MDIV63 | 0x04100000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 63 = 0.5079365 MHz |
| | | | 32MDIV125 | 0x020C0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 32 MHz / 125 = 0.256 MHz |

## 43.10.10 CONFIG.RATIO

Address offset: 0x518

MCK / LRCK ratio.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000006** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | RATIO | | | | | | | | | | | | | | | | | | | | | | | | | MCK / LRCK ratio. | | | | | | | |
| | | | 32X | | | | | | | | 0 | | | | | | | | | | | | | | | | LRCK = MCK / 32 | | | | | | | |
| | | | 48X | | | | | | | | 1 | | | | | | | | | | | | | | | | LRCK = MCK / 48 | | | | | | | |
| | | | 64X | | | | | | | | 2 | | | | | | | | | | | | | | | | LRCK = MCK / 64 | | | | | | | |
| | | | 96X | | | | | | | | 3 | | | | | | | | | | | | | | | | LRCK = MCK / 96 | | | | | | | |
| | | | 128X | | | | | | | | 4 | | | | | | | | | | | | | | | | LRCK = MCK / 128 | | | | | | | |
| | | | 192X | | | | | | | | 5 | | | | | | | | | | | | | | | | LRCK = MCK / 192 | | | | | | | |
| | | | 256X | | | | | | | | 6 | | | | | | | | | | | | | | | | LRCK = MCK / 256 | | | | | | | |
| | | | 384X | | | | | | | | 7 | | | | | | | | | | | | | | | | LRCK = MCK / 384 | | | | | | | |
| | | | 512X | | | | | | | | 8 | | | | | | | | | | | | | | | | LRCK = MCK / 512 | | | | | | | |

## 43.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000001** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | SWIDTH | | | | | | | | | | | | | | | | | | | | | | | | | Sample width. | | | | | | | |
| | | | 8Bit | | | | | | | | 0 | | | | | | | | | | | | | | | | 8 bit. | | | | | | | |
| | | | 16Bit | | | | | | | | 1 | | | | | | | | | | | | | | | | 16 bit. | | | | | | | |
| | | | 24Bit | | | | | | | | 2 | | | | | | | | | | | | | | | | 24 bit. | | | | | | | |

## 43.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | ALIGN | | | | | | | | | | | | | | | | | | | | | | | | | Alignment of sample within a frame. | | | | | | | |
| | | | Left | | | | | | | | 0 | | | | | | | | | | | | | | | | Left-aligned. | | | | | | | |
| | | | Right | | | | | | | | 1 | | | | | | | | | | | | | | | | Right-aligned. | | | | | | | |

## 43.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | FORMAT | | | | | | | | | | | | | | | | | | | | | | | | | Frame format. | | | | | | | |
| | | | I2S | | | | | | | | 0 | | | | | | | | | | | | | | | | Original I2S format. | | | | | | | |
| | | | Aligned | | | | | | | | 1 | | | | | | | | | | | | | | | | Alternate (left- or right-aligned) format. | | | | | | | |

## 43.10.14 CONFIG.CHANNELS

Address offset: 0x528

Enable channels.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CHANNELS | | | Enable channels. |
| | | | Stereo | 0 | Stereo. |
| | | | Left | 1 | Left only. |
| | | | Right | 2 | Right only. |

## 43.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Receive buffer Data RAM start address. When receiving, words containing samples will be written to this address. This address is a word aligned Data RAM address. |

## 43.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Transmit buffer Data RAM start address. When transmitting, words containing samples will be fetched from this address. This address is a word aligned Data RAM address. |

## 43.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Size of RXD and TXD buffers in number of 32 bit words. |

## 43.10.18 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 43.10.19 PSEL.SCK

Address offset: 0x564

Pin select for SCK signal.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | B | | | | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | | | | | |

## 43.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | B | | | | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | | | | | |

## 43.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | B | | | | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | | | | | |

## 43.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | B | | | | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | Pin number | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | Port number | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | Disconnect | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | Connect | | | | | | | | | |

## 43.11 Electrical specification

### 43.11.1 I2S timing specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{S\_SDIN}$ | SDIN setup time before SCK rising | 20 | | | ns |
| $t_{H\_SDIN}$ | SDIN hold time after SCK rising | 15 | | | ns |
| $t_{S\_SDOUT}$ | SDOUT setup time after SCK falling | 40 | | | ns |
| $t_{H\_SDOUT}$ | SDOUT hold time before SCK falling | 6 | | | ns |
| $t_{SCK\_LRCK}$ | SCLK falling to LRCK edge | -5 | 0 | 5 | ns |
| $f_{MCK}$ | MCK frequency | | | 4000 | kHz |
| $f_{LRCK}$ | LRCK frequency | | | 48 | kHz |
| $f_{SCK}$ | SCK frequency | | | 2000 | kHz |
| $DC_{CK}$ | Clock duty cycle (MCK, LRCK, SCK) | 45 | | 55 | % |

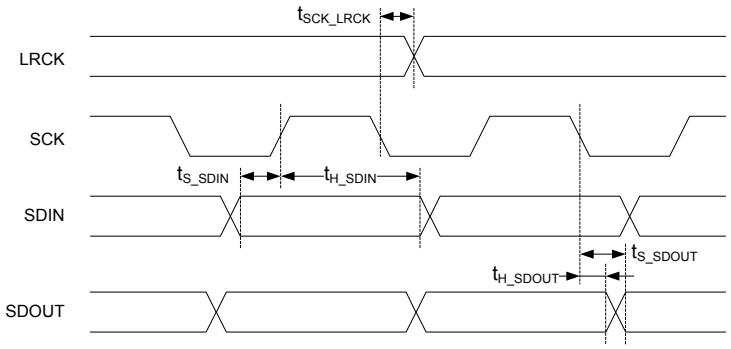



**Figure 151: I2S timing diagram**

# 44 MWU — Memory watch unit

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU. The MWU can be configured to trigger events for access to Data RAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of Data RAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

**Table 102: Memory regions**

| Memory region | START address | END address |
|---|---|---|
| REGION[0..3] | Configurable | Configurable |
| PREGION[0] | 0x40000000 | 0x4001FFFF |
| PREGION[1] | 0x40020000 | 0x4003FFFF |

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. These addresses are byte aligned and inclusive. The END register value has to be greater or equal to the START register value. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing subregions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the Data RAM and Peripheral memory segments from the CPU, see *Memory* on page 20 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

## 44.1 Registers

**Table 103: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40020000 | MWU | MWU | Memory watch unit | |

### Table 104: Register Overview

| Register | Offset | Description |
|---|---|---|
| EVENTS_REGION[0].WA | 0x100 | Write access to region 0 detected |
| EVENTS_REGION[0].RA | 0x104 | Read access to region 0 detected |
| EVENTS_REGION[1].WA | 0x108 | Write access to region 1 detected |
| EVENTS_REGION[1].RA | 0x10C | Read access to region 1 detected |
| EVENTS_REGION[2].WA | 0x110 | Write access to region 2 detected |
| EVENTS_REGION[2].RA | 0x114 | Read access to region 2 detected |
| EVENTS_REGION[3].WA | 0x118 | Write access to region 3 detected |
| EVENTS_REGION[3].RA | 0x11C | Read access to region 3 detected |
| EVENTS_PREGION[0].WA | 0x160 | Write access to peripheral region 0 detected |
| EVENTS_PREGION[0].RA | 0x164 | Read access to peripheral region 0 detected |
| EVENTS_PREGION[1].WA | 0x168 | Write access to peripheral region 1 detected |
| EVENTS_PREGION[1].RA | 0x16C | Read access to peripheral region 1 detected |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *NMIEN* | 0x320 | Enable or disable non-maskable interrupt |
| *NMIENSET* | 0x324 | Enable non-maskable interrupt |
| *NMIENCLR* | 0x328 | Disable non-maskable interrupt |
| *PERREGION[0].SUBSTAT* | 0x400 | Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching |
| *PERREGION[0].SUBSTAT* | 0x404 | Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching |
| *PERREGION[1].SUBSTAT* | 0x408 | Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching |
| *PERREGION[1].SUBSTAT* | 0x40C | Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching |
| *REGIONEN* | 0x510 | Enable/disable regions watch |
| *REGIONENSET* | 0x514 | Enable regions watch |
| *REGIONENCLR* | 0x518 | Disable regions watch |
| *REGION[0].START* | 0x600 | Start address for region 0 |
| *REGION[0].END* | 0x604 | End address of region 0 |
| *REGION[1].START* | 0x610 | Start address for region 1 |
| *REGION[1].END* | 0x614 | End address of region 1 |
| *REGION[2].START* | 0x620 | Start address for region 2 |
| *REGION[2].END* | 0x624 | End address of region 2 |
| *REGION[3].START* | 0x630 | Start address for region 3 |
| *REGION[3].END* | 0x634 | End address of region 3 |
| *PREGION[0].START* | 0x6C0 | Reserved for future use |
| *PREGION[0].END* | 0x6C4 | Reserved for future use |
| *PREGION[0].SUBS* | 0x6C8 | Subregions of region 0 |
| *PREGION[1].START* | 0x6D0 | Reserved for future use |
| *PREGION[1].END* | 0x6D4 | Reserved for future use |
| *PREGION[1].SUBS* | 0x6D8 | Subregions of region 1 |

## 44.1.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | REGION0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for REGION[0].WA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[0].WA* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | Enabled | 1 | Enable |
| B | RW | REGION0RA | | | Enable or disable interrupt for REGION[0].RA event<br><br>See *EVENTS_REGION[0].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| C | RW | REGION1WA | | | Enable or disable interrupt for REGION[1].WA event<br><br>See *EVENTS_REGION[1].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| D | RW | REGION1RA | | | Enable or disable interrupt for REGION[1].RA event<br><br>See *EVENTS_REGION[1].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| E | RW | REGION2WA | | | Enable or disable interrupt for REGION[2].WA event<br><br>See *EVENTS_REGION[2].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| F | RW | REGION2RA | | | Enable or disable interrupt for REGION[2].RA event<br><br>See *EVENTS_REGION[2].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| G | RW | REGION3WA | | | Enable or disable interrupt for REGION[3].WA event<br><br>See *EVENTS_REGION[3].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| H | RW | REGION3RA | | | Enable or disable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| I | RW | PREGION0WA | | | Enable or disable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| J | RW | PREGION0RA | | | Enable or disable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| K | RW | PREGION1WA | | | Enable or disable interrupt for PREGION[1].WA event<br><br>See *EVENTS_PREGION[1].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| L | RW | PREGION1RA | | | Enable or disable interrupt for PREGION[1].RA event<br><br>See *EVENTS_PREGION[1].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 44.1.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | REGION0WA | | | Write '1' to Enable interrupt for REGION[0].WA event<br><br>See *EVENTS_REGION[0].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | REGION0RA | | | Write '1' to Enable interrupt for REGION[0].RA event<br><br>See *EVENTS_REGION[0].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | REGION1WA | | | Write '1' to Enable interrupt for REGION[1].WA event<br><br>See *EVENTS_REGION[1].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | REGION1RA | | | Write '1' to Enable interrupt for REGION[1].RA event<br><br>See *EVENTS_REGION[1].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | REGION2WA | | | Write '1' to Enable interrupt for REGION[2].WA event<br><br>See *EVENTS_REGION[2].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | REGION2RA | | | Write '1' to Enable interrupt for REGION[2].RA event<br><br>See *EVENTS_REGION[2].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | REGION3WA | | | Write '1' to Enable interrupt for REGION[3].WA event<br><br>See *EVENTS_REGION[3].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | REGION3RA | | | Write '1' to Enable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | PREGION0WA | | | Write '1' to Enable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| J | RW | PREGION0RA | | | Write '1' to Enable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| K | RW | PREGION1WA | | | Write '1' to Enable interrupt for PREGION[1].WA event |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_PREGION[1].WA* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| L | RW | PREGION1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for PREGION[1].RA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_PREGION[1].RA* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |

## 44.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | REGION0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[0].WA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[0].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| B | RW | REGION0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[0].RA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[0].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| C | RW | REGION1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[1].WA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[1].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| D | RW | REGION1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[1].RA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[1].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| E | RW | REGION2WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[2].WA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[2].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| F | RW | REGION2RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[2].RA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[2].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| G | RW | REGION3WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[3].WA event | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_REGION[3].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| H | RW | REGION3RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| I | RW | PREGION0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| J | RW | PREGION0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| K | RW | PREGION1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for PREGION[1].WA event<br><br>See *EVENTS_PREGION[1].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| L | RW | PREGION1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable interrupt for PREGION[1].RA event<br><br>See *EVENTS_PREGION[1].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |

## 44.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | REGION0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable non-maskable interrupt for REGION[0].WA event<br><br>See *EVENTS_REGION[0].WA* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| B | RW | REGION0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable non-maskable interrupt for REGION[0].RA event<br><br>See *EVENTS_REGION[0].RA* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| C | RW | REGION1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable non-maskable interrupt for REGION[1].WA event<br><br>See *EVENTS_REGION[1].WA* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| D | RW | REGION1RA | | | Enable or disable non-maskable interrupt for REGION[1].RA event<br><br>See *EVENTS_REGION[1].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| E | RW | REGION2WA | | | Enable or disable non-maskable interrupt for REGION[2].WA event<br><br>See *EVENTS_REGION[2].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| F | RW | REGION2RA | | | Enable or disable non-maskable interrupt for REGION[2].RA event<br><br>See *EVENTS_REGION[2].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| G | RW | REGION3WA | | | Enable or disable non-maskable interrupt for REGION[3].WA event<br><br>See *EVENTS_REGION[3].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| H | RW | REGION3RA | | | Enable or disable non-maskable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| I | RW | PREGION0WA | | | Enable or disable non-maskable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| J | RW | PREGION0RA | | | Enable or disable non-maskable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| K | RW | PREGION1WA | | | Enable or disable non-maskable interrupt for PREGION[1].WA event<br><br>See *EVENTS_PREGION[1].WA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| L | RW | PREGION1RA | | | Enable or disable non-maskable interrupt for PREGION[1].RA event<br><br>See *EVENTS_PREGION[1].RA* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

### 44.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | REGION0WA | | | Write '1' to Enable non-maskable interrupt for REGION[0].WA event<br><br>See *EVENTS_REGION[0].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | REGION0RA | | | Write '1' to Enable non-maskable interrupt for REGION[0].RA event<br><br>See *EVENTS_REGION[0].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | REGION1WA | | | Write '1' to Enable non-maskable interrupt for REGION[1].WA event<br><br>See *EVENTS_REGION[1].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | REGION1RA | | | Write '1' to Enable non-maskable interrupt for REGION[1].RA event<br><br>See *EVENTS_REGION[1].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | REGION2WA | | | Write '1' to Enable non-maskable interrupt for REGION[2].WA event<br><br>See *EVENTS_REGION[2].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | REGION2RA | | | Write '1' to Enable non-maskable interrupt for REGION[2].RA event<br><br>See *EVENTS_REGION[2].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | REGION3WA | | | Write '1' to Enable non-maskable interrupt for REGION[3].WA event<br><br>See *EVENTS_REGION[3].WA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | REGION3RA | | | Write '1' to Enable non-maskable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | PREGION0WA | | | Write '1' to Enable non-maskable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| J | RW | PREGION0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable non-maskable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| K | RW | PREGION1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable non-maskable interrupt for PREGION[1].WA event<br><br>See *EVENTS_PREGION[1].WA* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| L | RW | PREGION1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable non-maskable interrupt for PREGION[1].RA event<br><br>See *EVENTS_PREGION[1].RA* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |

### 44.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | REGION0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable non-maskable interrupt for REGION[0].WA event<br><br>See *EVENTS_REGION[0].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| B | RW | REGION0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable non-maskable interrupt for REGION[0].RA event<br><br>See *EVENTS_REGION[0].RA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| C | RW | REGION1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable non-maskable interrupt for REGION[1].WA event<br><br>See *EVENTS_REGION[1].WA* | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| D | RW | REGION1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Disable non-maskable interrupt for REGION[1].RA event<br><br>See *EVENTS_REGION[1].RA* | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | REGION2WA | | | Write '1' to Disable non-maskable interrupt for REGION[2].WA event<br><br>See *EVENTS_REGION[2].WA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | REGION2RA | | | Write '1' to Disable non-maskable interrupt for REGION[2].RA event<br><br>See *EVENTS_REGION[2].RA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | REGION3WA | | | Write '1' to Disable non-maskable interrupt for REGION[3].WA event<br><br>See *EVENTS_REGION[3].WA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | REGION3RA | | | Write '1' to Disable non-maskable interrupt for REGION[3].RA event<br><br>See *EVENTS_REGION[3].RA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | PREGION0WA | | | Write '1' to Disable non-maskable interrupt for PREGION[0].WA event<br><br>See *EVENTS_PREGION[0].WA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| J | RW | PREGION0RA | | | Write '1' to Disable non-maskable interrupt for PREGION[0].RA event<br><br>See *EVENTS_PREGION[0].RA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| K | RW | PREGION1WA | | | Write '1' to Disable non-maskable interrupt for PREGION[1].WA event<br><br>See *EVENTS_PREGION[1].WA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| L | RW | PREGION1RA | | | Write '1' to Disable non-maskable interrupt for PREGION[1].RA event<br><br>See *EVENTS_PREGION[1].RA* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 44.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SR0 | | | Subregion 0 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| B | RW | SR1 | | | Subregion 1 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| C | RW | SR2 | | | Subregion 2 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| D | RW | SR3 | | | Subregion 3 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| E | RW | SR4 | | | Subregion 4 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| F | RW | SR5 | | | Subregion 5 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| G | RW | SR6 | | | Subregion 6 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| H | RW | SR7 | | | Subregion 7 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| I | RW | SR8 | | | Subregion 8 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| J | RW | SR9 | | | Subregion 9 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| K | RW | SR10 | | | Subregion 10 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| L | RW | SR11 | | | Subregion 11 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| M | RW | SR12 | | | Subregion 12 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| N | RW | SR13 | | | Subregion 13 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| O | RW | SR14 | | | Subregion 14 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| P | RW | SR15 | | | Subregion 15 in region 0 (write '1' to clear) |
| | | | NoAccess | 0 | No write access occurred in this subregion |
| | | | Access | 1 | Write access(es) occurred in this subregion |
| Q | RW | SR16 | | | Subregion 16 in region 0 (write '1' to clear) |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | SR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | SR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | SR8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | SR9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | SR10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | SR11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | SR12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | SR13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | SR14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | SR15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | SR16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | SR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | SR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | SR8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | SR9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | SR10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | SR11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | SR12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | SR13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | SR14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | SR15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | SR16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | SR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | SR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | SR8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | SR9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | SR10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | SR11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | SR12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | SR13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | SR14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | SR15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | SR16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 21 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 22 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 23 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 24 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 25 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 26 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 27 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 28 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 29 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 30 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | Subregion 31 in region 1 (write '1' to clear) | | | | | | | |
| | | | NoAccess | 0 | | | | | | | | | | | | | | | | | | | | | | | | No read access occurred in this subregion | | | | | | | |
| | | | Access | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access(es) occurred in this subregion | | | | | | | |

## 44.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | RGN0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable/disable write access watch in region[0] | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this region | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable write access watch in this region | | | | | | | |
| B | RW | RGN0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable/disable read access watch in region[0] | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in this region | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable read access watch in this region | | | | | | | |
| C | RW | RGN1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable/disable write access watch in region[1] | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this region | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable write access watch in this region | | | | | | | |
| D | RW | RGN1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Enable/disable read access watch in region[1] | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | RGN2WA | | | | | | | | | | Enable/disable write access watch in region[2] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RGN2RA | | | | | | | | | | Enable/disable read access watch in region[2] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RGN3WA | | | | | | | | | | Enable/disable write access watch in region[3] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RGN3RA | | | | | | | | | | Enable/disable read access watch in region[3] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PRGN0WA | | | | | | | | | | Enable/disable write access watch in PREGION[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PRGN0RA | | | | | | | | | | Enable/disable read access watch in PREGION[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PRGN1WA | | | | | | | | | | Enable/disable write access watch in PREGION[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PRGN1RA | | | | | | | | | | Enable/disable read access watch in PREGION[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | Disable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | Enable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.12 REGIONENSET

Address offset: 0x514

Enable regions watch

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RGN0WA | | | | | | | | | | Enable write access watch in region[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RGN0RA | | | | | | | | | | Enable read access watch in region[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RGN1WA | | | | | | | | | | Enable write access watch in region[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RGN1RA | | | | | | | | | | Enable read access watch in region[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | RGN2WA | | | | | | | | | | Enable write access watch in region[2] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RGN2RA | | | | | | | | | | Enable read access watch in region[2] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | RGN3WA | | | | | | | | | | Enable write access watch in region[3] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | RGN3RA | | | | | | | | | | Enable read access watch in region[3] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | PRGN0WA | | | | | | | | | | Enable write access watch in PREGION[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this PREGION is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this PREGION is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | PRGN0RA | | | | | | | | | | Enable read access watch in PREGION[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this PREGION is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this PREGION is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | PRGN1WA | | | | | | | | | | Enable write access watch in PREGION[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable write access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this PREGION is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this PREGION is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | PRGN1RA | | | | | | | | | | Enable read access watch in PREGION[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | Enable read access watch in this PREGION | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this PREGION is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this PREGION is enabled | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.13 REGIONENCLR

Address offset: 0x518

Disable regions watch

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | RGN0WA | | | | | | | | | | Disable write access watch in region[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RGN0RA | | | | | | | | | | Disable read access watch in region[0] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RGN1WA | | | | | | | | | | Disable write access watch in region[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable write access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Write access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Write access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | RGN1RA | | | | | | | | | | Disable read access watch in region[1] | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | Disable read access watch in this region | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | Read access watch in this region is disabled | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | Read access watch in this region is enabled | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | L | K | J | I | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| E | RW | RGN2WA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in region[2] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this region | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this region is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this region is enabled | | | | | | | |
| F | RW | RGN2RA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in region[2] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in this region | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this region is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this region is enabled | | | | | | | |
| G | RW | RGN3WA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in region[3] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this region | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this region is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this region is enabled | | | | | | | |
| H | RW | RGN3RA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in region[3] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in this region | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this region is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this region is enabled | | | | | | | |
| I | RW | PRGN0WA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in PREGION[0] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this PREGION | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this PREGION is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this PREGION is enabled | | | | | | | |
| J | RW | PRGN0RA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in PREGION[0] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in this PREGION | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this PREGION is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this PREGION is enabled | | | | | | | |
| K | RW | PRGN1WA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in PREGION[1] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable write access watch in this PREGION | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this PREGION is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Write access watch in this PREGION is enabled | | | | | | | |
| L | RW | PRGN1RA | | | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in PREGION[1] | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | Disable read access watch in this PREGION | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this PREGION is disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read access watch in this PREGION is enabled | | | | | | | |

## 44.1.14 REGION[0].START

Address offset: 0x600

Start address for region 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | START | | | | | | | | | | | | | | | | | | | | | | | | | | Start address for region | | | | | | | |

## 44.1.15 REGION[0].END

Address offset: 0x604

End address of region 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | End address of region. | | | | | | | |

### 44.1.16 REGION[1].START

Address offset: 0x610

Start address for region 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | START | | | Start address for region |

### 44.1.17 REGION[1].END

Address offset: 0x614

End address of region 1

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | END | | | End address of region. |

### 44.1.18 REGION[2].START

Address offset: 0x620

Start address for region 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | START | | | Start address for region |

### 44.1.19 REGION[2].END

Address offset: 0x624

End address of region 2

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | END | | | End address of region. |

### 44.1.20 REGION[3].START

Address offset: 0x630

Start address for region 3

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | START | | | Start address for region |

### 44.1.21 REGION[3].END

Address offset: 0x634

End address of region 3

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | End address of region. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reserved for future use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Reserved for future use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.24 PREGION[0].SUBS

Address offset: 0x6C8

Subregions of region 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | SR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | SR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | SR8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | SR9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | SR10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | SR11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | SR12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | SR13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | SR14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | SR15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | SR16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 44.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reserved for future use

## 44.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reserved for future use

## 44.1.27 PREGION[1].SUBS

Address offset: 0x6D8

Subregions of region 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SR0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SR3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SR4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SR5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | SR6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | SR7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | SR8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | SR9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | SR10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | SR11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | SR12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | SR13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | SR14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | SR15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | SR16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | SR17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | SR18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | SR19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | SR20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SR21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | SR22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | SR23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | SR24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | SR25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | RW | SR26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | RW | SR27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | RW | SR28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| d | RW | SR29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | RW | SR30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| f | RW | SR31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Exclude | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Include | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 45 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Enables SW triggering of interrupts
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Refer to *Table 105: Instances* on page 551 for a list of the various EGU instances

## 45.1 Registers

### Table 105: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40014000 | EGU | EGU0 | Event generator unit 0 | |
| 0x40015000 | EGU | EGU1 | Event generator unit 1 | |
| 0x40016000 | EGU | EGU2 | Event generator unit 2 | |
| 0x40017000 | EGU | EGU3 | Event generator unit 3 | |
| 0x40018000 | EGU | EGU4 | Event generator unit 4 | |
| 0x40019000 | EGU | EGU5 | Event generator unit 5 | |

### Table 106: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_TRIGGER[0] | 0x000 | Trigger 0 for triggering the corresponding TRIGGERED[0] event |
| TASKS_TRIGGER[1] | 0x004 | Trigger 1 for triggering the corresponding TRIGGERED[1] event |
| TASKS_TRIGGER[2] | 0x008 | Trigger 2 for triggering the corresponding TRIGGERED[2] event |
| TASKS_TRIGGER[3] | 0x00C | Trigger 3 for triggering the corresponding TRIGGERED[3] event |
| TASKS_TRIGGER[4] | 0x010 | Trigger 4 for triggering the corresponding TRIGGERED[4] event |
| TASKS_TRIGGER[5] | 0x014 | Trigger 5 for triggering the corresponding TRIGGERED[5] event |
| TASKS_TRIGGER[6] | 0x018 | Trigger 6 for triggering the corresponding TRIGGERED[6] event |
| TASKS_TRIGGER[7] | 0x01C | Trigger 7 for triggering the corresponding TRIGGERED[7] event |
| TASKS_TRIGGER[8] | 0x020 | Trigger 8 for triggering the corresponding TRIGGERED[8] event |
| TASKS_TRIGGER[9] | 0x024 | Trigger 9 for triggering the corresponding TRIGGERED[9] event |
| TASKS_TRIGGER[10] | 0x028 | Trigger 10 for triggering the corresponding TRIGGERED[10] event |
| TASKS_TRIGGER[11] | 0x02C | Trigger 11 for triggering the corresponding TRIGGERED[11] event |
| TASKS_TRIGGER[12] | 0x030 | Trigger 12 for triggering the corresponding TRIGGERED[12] event |
| TASKS_TRIGGER[13] | 0x034 | Trigger 13 for triggering the corresponding TRIGGERED[13] event |
| TASKS_TRIGGER[14] | 0x038 | Trigger 14 for triggering the corresponding TRIGGERED[14] event |
| TASKS_TRIGGER[15] | 0x03C | Trigger 15 for triggering the corresponding TRIGGERED[15] event |
| EVENTS_TRIGGERED[0] | 0x100 | Event number 0 generated by triggering the corresponding TRIGGER[0] task |
| EVENTS_TRIGGERED[1] | 0x104 | Event number 1 generated by triggering the corresponding TRIGGER[1] task |
| EVENTS_TRIGGERED[2] | 0x108 | Event number 2 generated by triggering the corresponding TRIGGER[2] task |
| EVENTS_TRIGGERED[3] | 0x10C | Event number 3 generated by triggering the corresponding TRIGGER[3] task |
| EVENTS_TRIGGERED[4] | 0x110 | Event number 4 generated by triggering the corresponding TRIGGER[4] task |
| EVENTS_TRIGGERED[5] | 0x114 | Event number 5 generated by triggering the corresponding TRIGGER[5] task |
| EVENTS_TRIGGERED[6] | 0x118 | Event number 6 generated by triggering the corresponding TRIGGER[6] task |

| Register | Offset | Description |
|---|---|---|
| EVENTS_TRIGGERED[7] | 0x11C | Event number 7 generated by triggering the corresponding TRIGGER[7] task |
| EVENTS_TRIGGERED[8] | 0x120 | Event number 8 generated by triggering the corresponding TRIGGER[8] task |
| EVENTS_TRIGGERED[9] | 0x124 | Event number 9 generated by triggering the corresponding TRIGGER[9] task |
| EVENTS_TRIGGERED[10] | 0x128 | Event number 10 generated by triggering the corresponding TRIGGER[10] task |
| EVENTS_TRIGGERED[11] | 0x12C | Event number 11 generated by triggering the corresponding TRIGGER[11] task |
| EVENTS_TRIGGERED[12] | 0x130 | Event number 12 generated by triggering the corresponding TRIGGER[12] task |
| EVENTS_TRIGGERED[13] | 0x134 | Event number 13 generated by triggering the corresponding TRIGGER[13] task |
| EVENTS_TRIGGERED[14] | 0x138 | Event number 14 generated by triggering the corresponding TRIGGER[14] task |
| EVENTS_TRIGGERED[15] | 0x13C | Event number 15 generated by triggering the corresponding TRIGGER[15] task |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |

## 45.1.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | TRIGGERED0 | | | Enable or disable interrupt for TRIGGERED[0] event<br>See *EVENTS_TRIGGERED[0]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| B | RW | TRIGGERED1 | | | Enable or disable interrupt for TRIGGERED[1] event<br>See *EVENTS_TRIGGERED[1]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| C | RW | TRIGGERED2 | | | Enable or disable interrupt for TRIGGERED[2] event<br>See *EVENTS_TRIGGERED[2]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| D | RW | TRIGGERED3 | | | Enable or disable interrupt for TRIGGERED[3] event<br>See *EVENTS_TRIGGERED[3]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| E | RW | TRIGGERED4 | | | Enable or disable interrupt for TRIGGERED[4] event<br>See *EVENTS_TRIGGERED[4]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| F | RW | TRIGGERED5 | | | Enable or disable interrupt for TRIGGERED[5] event<br>See *EVENTS_TRIGGERED[5]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| G | RW | TRIGGERED6 | | | Enable or disable interrupt for TRIGGERED[6] event<br>See *EVENTS_TRIGGERED[6]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| H | RW | TRIGGERED7 | | | Enable or disable interrupt for TRIGGERED[7] event<br>See *EVENTS_TRIGGERED[7]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| I | RW | TRIGGERED8 | | | Enable or disable interrupt for TRIGGERED[8] event |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | | | See *EVENTS_TRIGGERED[8]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| J | RW | TRIGGERED9 | | | Enable or disable interrupt for TRIGGERED[9] event<br>See *EVENTS_TRIGGERED[9]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| K | RW | TRIGGERED10 | | | Enable or disable interrupt for TRIGGERED[10] event<br>See *EVENTS_TRIGGERED[10]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| L | RW | TRIGGERED11 | | | Enable or disable interrupt for TRIGGERED[11] event<br>See *EVENTS_TRIGGERED[11]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| M | RW | TRIGGERED12 | | | Enable or disable interrupt for TRIGGERED[12] event<br>See *EVENTS_TRIGGERED[12]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| N | RW | TRIGGERED13 | | | Enable or disable interrupt for TRIGGERED[13] event<br>See *EVENTS_TRIGGERED[13]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| O | RW | TRIGGERED14 | | | Enable or disable interrupt for TRIGGERED[14] event<br>See *EVENTS_TRIGGERED[14]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| P | RW | TRIGGERED15 | | | Enable or disable interrupt for TRIGGERED[15] event<br>See *EVENTS_TRIGGERED[15]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 45.1.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | TRIGGERED0 | | | Write '1' to Enable interrupt for TRIGGERED[0] event<br>See *EVENTS_TRIGGERED[0]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | TRIGGERED1 | | | Write '1' to Enable interrupt for TRIGGERED[1] event<br>See *EVENTS_TRIGGERED[1]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | TRIGGERED2 | | | Write '1' to Enable interrupt for TRIGGERED[2] event |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | | | See *EVENTS_TRIGGERED[2]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | TRIGGERED3 | | | Write '1' to Enable interrupt for TRIGGERED[3] event<br><br>See *EVENTS_TRIGGERED[3]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | TRIGGERED4 | | | Write '1' to Enable interrupt for TRIGGERED[4] event<br><br>See *EVENTS_TRIGGERED[4]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | TRIGGERED5 | | | Write '1' to Enable interrupt for TRIGGERED[5] event<br><br>See *EVENTS_TRIGGERED[5]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | TRIGGERED6 | | | Write '1' to Enable interrupt for TRIGGERED[6] event<br><br>See *EVENTS_TRIGGERED[6]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | TRIGGERED7 | | | Write '1' to Enable interrupt for TRIGGERED[7] event<br><br>See *EVENTS_TRIGGERED[7]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | TRIGGERED8 | | | Write '1' to Enable interrupt for TRIGGERED[8] event<br><br>See *EVENTS_TRIGGERED[8]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| J | RW | TRIGGERED9 | | | Write '1' to Enable interrupt for TRIGGERED[9] event<br><br>See *EVENTS_TRIGGERED[9]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| K | RW | TRIGGERED10 | | | Write '1' to Enable interrupt for TRIGGERED[10] event<br><br>See *EVENTS_TRIGGERED[10]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| L | RW | TRIGGERED11 | | | Write '1' to Enable interrupt for TRIGGERED[11] event<br><br>See *EVENTS_TRIGGERED[11]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| M | RW | TRIGGERED12 | | | Write '1' to Enable interrupt for TRIGGERED[12] event<br><br>See *EVENTS_TRIGGERED[12]* |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| N | RW | TRIGGERED13 | | | Write '1' to Enable interrupt for TRIGGERED[13] event<br>See *EVENTS_TRIGGERED[13]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| O | RW | TRIGGERED14 | | | Write '1' to Enable interrupt for TRIGGERED[14] event<br>See *EVENTS_TRIGGERED[14]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| P | RW | TRIGGERED15 | | | Write '1' to Enable interrupt for TRIGGERED[15] event<br>See *EVENTS_TRIGGERED[15]* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

### 45.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | TRIGGERED0 | | | Write '1' to Disable interrupt for TRIGGERED[0] event<br>See *EVENTS_TRIGGERED[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | TRIGGERED1 | | | Write '1' to Disable interrupt for TRIGGERED[1] event<br>See *EVENTS_TRIGGERED[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | TRIGGERED2 | | | Write '1' to Disable interrupt for TRIGGERED[2] event<br>See *EVENTS_TRIGGERED[2]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | TRIGGERED3 | | | Write '1' to Disable interrupt for TRIGGERED[3] event<br>See *EVENTS_TRIGGERED[3]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | TRIGGERED4 | | | Write '1' to Disable interrupt for TRIGGERED[4] event<br>See *EVENTS_TRIGGERED[4]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | | | | | | | | | | | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| F | RW | TRIGGERED5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| G | RW | TRIGGERED6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| H | RW | TRIGGERED7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| I | RW | TRIGGERED8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| J | RW | TRIGGERED9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| K | RW | TRIGGERED10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| L | RW | TRIGGERED11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| M | RW | TRIGGERED12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| N | RW | TRIGGERED13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| O | RW | TRIGGERED14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| P | RW | TRIGGERED15 | | | Write '1' to Disable interrupt for TRIGGERED[15] event<br><br>See *EVENTS_TRIGGERED[15]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

# 45.2 Electrical specification

## 45.2.1 EGU Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{EGU,EVT}$ | Latency between setting an EGU event flag and the system setting an interrupt | | 1 | | cycles |

# 46 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

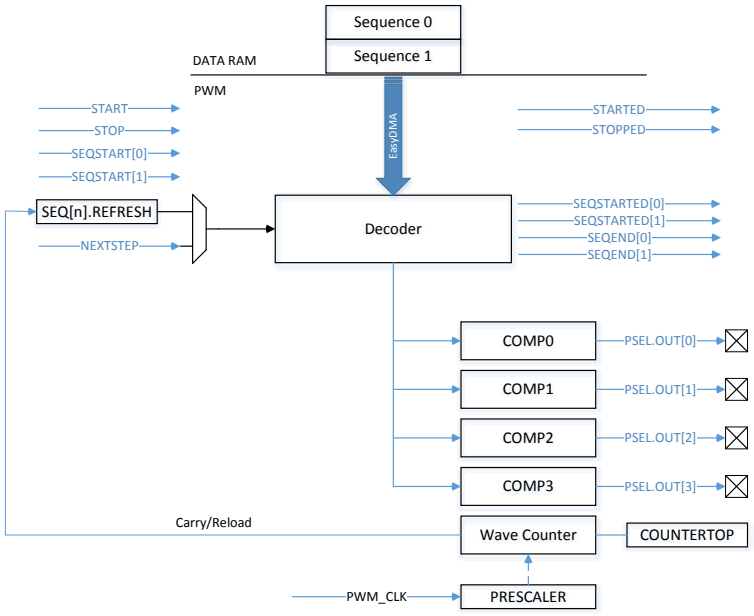



**Figure 152: PWM Module**

## 46.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 155: Decoder memory access modes* on page 561), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,

and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 561 below).

*Figure 153: PWM up counter example - FallingEdge polarity* on page 559 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY,
 PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

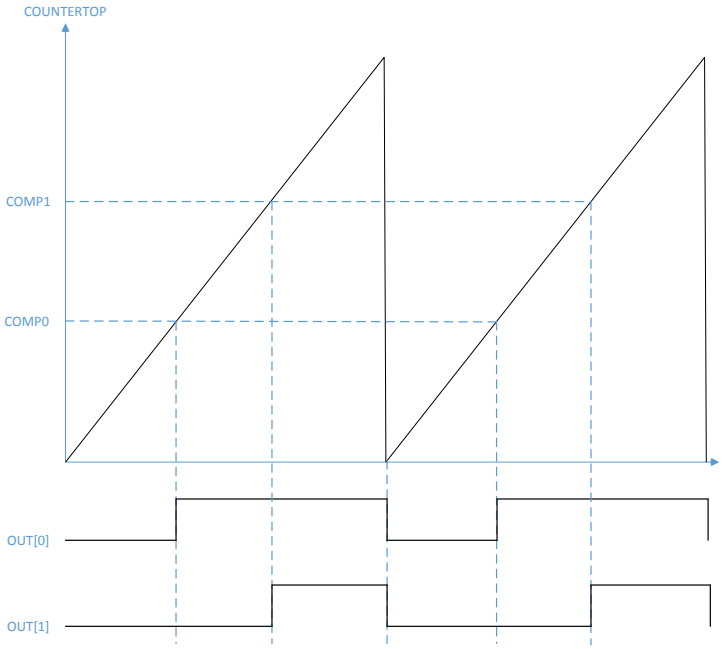



**Figure 153: PWM up counter example - FallingEdge polarity**

In up counting mode, the following formula can be used to compute PWM period and step size:

PWM period: $T_{PWM(Up)} = T_{PWM\_CLK} * COUNTERTOP$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK}$

*Figure 154: PWM up-and-down counter example* on page 560 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY,
 PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_UpAndDown << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

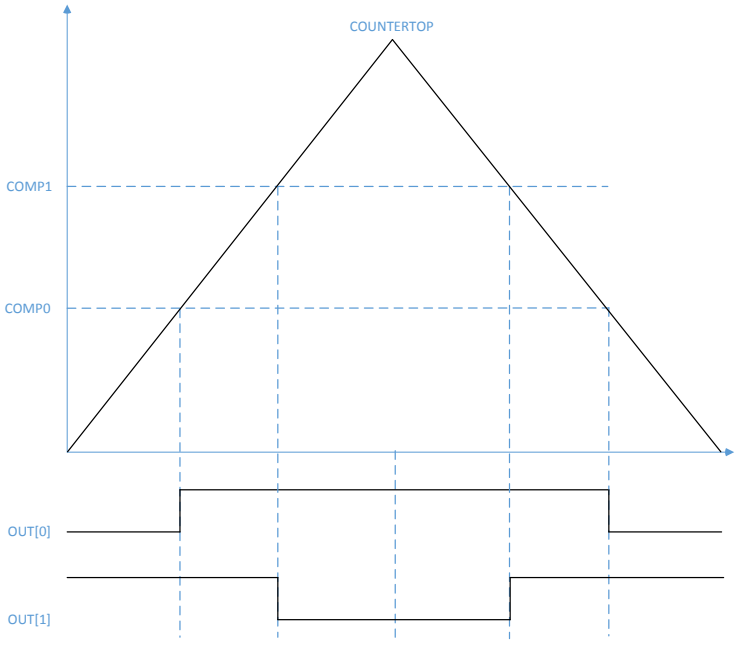



**Figure 154: PWM up-and-down counter example**

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

$T_{PWM(Up\ And\ Down)} = T_{PWM\_CLK} * 2 * COUNTERTOP$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK} * 2$

## 46.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | RW | COMPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Duty cycle setting - value loaded to internal compare register |
| B | RW | POLARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Edge polarity of GPIO. |
| | | | RisingEdge | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | First edge within the PWM period is rising |
| | | | FallingEdge | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | First edge within the PWM period is falling |

The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 155: Decoder memory access modes* on page 561 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)$^{th}$ PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

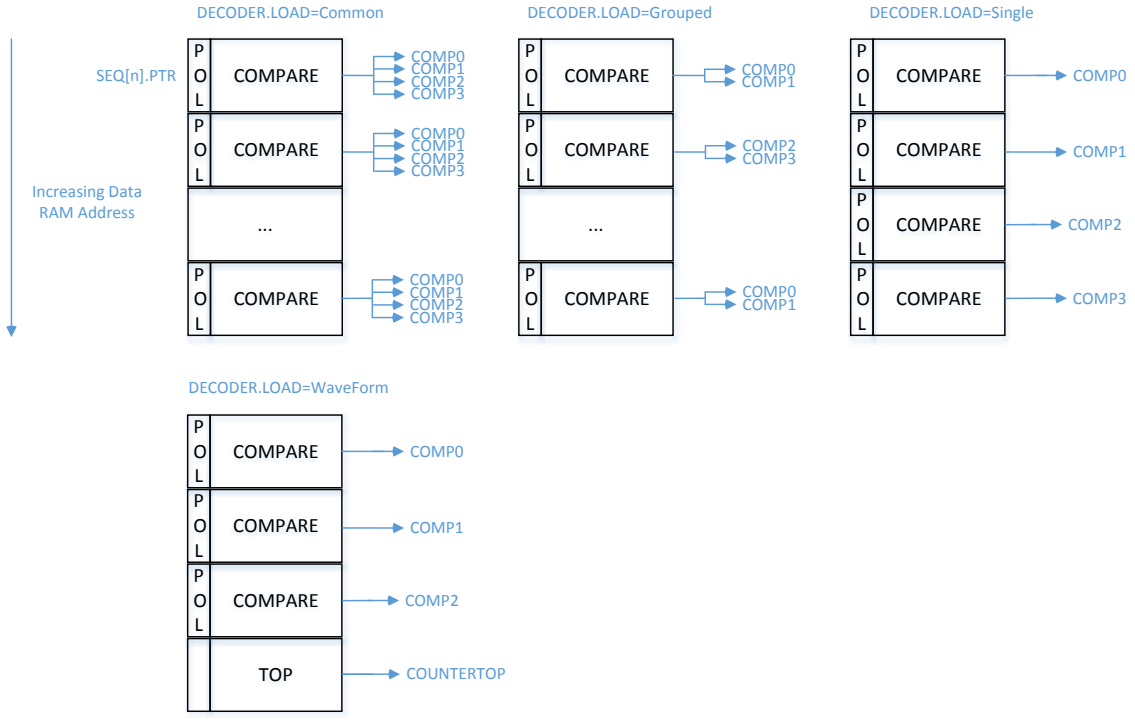



**Figure 155: Decoder memory access modes**

SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 156: Simple sequence example* on page 563 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

**Table 107: When to safely update PWM registers**

| Register | Taken into account by hardware | Recommended (safe) update |
|---|---|---|
| SEQ[n].PTR | When sending the SEQSTART[n] task | After having received the SEQSTARTED[n] event |
| SEQ[n].CNT | When sending the SEQSTART[n] task | After having received the SEQSTARTED[n] event |
| SEQ[0].ENDDELAY | When sending the SEQSTART[0] task | Before starting sequence [0] through a SEQSTART[0] task |
| | Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event) |
| | | At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired) |
| SEQ[1].ENDDELAY | When sending the SEQSTART[1] task | Before starting sequence [1] through a SEQSTART[1] task |
| | Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event) |
| | | At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired) |
| SEQ[0].REFRESH | When sending the SEQSTART[0] task | Before starting sequence [0] through a SEQSTART[0] task |
| | Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired) |
| SEQ[1].REFRESH | When sending the SEQSTART[1] task | Before starting sequence [1] through a SEQSTART[1] task |
| | Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired) |
| COUNTERTOP | In DECODER.LOAD=WaveForm: this register is ignored. | Before starting PWM generation through a SEQSTART[n] task |
| | In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event) | After a STOP task has been issued, and the STOPPED event has been received. |
| MODE | Immediately | Before starting PWM generation through a SEQSTART[n] task |
| | | After a STOP task has been issued, and the STOPPED event has been received. |
| DECODER | Immediately | Before starting PWM generation through a SEQSTART[n] task |
| | | After a STOP task has been issued, and the STOPPED event has been received. |
| PRESCALER | Immediately | Before starting PWM generation through a SEQSTART[n] task |
| | | After a STOP task has been issued, and the STOPPED event has been received. |
| LOOP | Immediately | Before starting PWM generation through a SEQSTART[n] task |
| | | After a STOP task has been issued, and the STOPPED event has been received. |
| PSEL.OUT[n] | Immediately | Before enabling the PWM instance through the ENABLE register |

**Important:** SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).

*Figure 156: Simple sequence example* on page 563 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                  PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                                                  PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

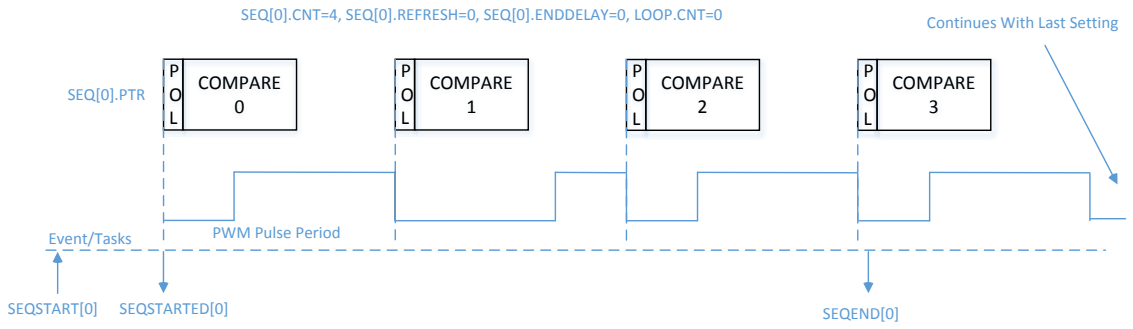



**Figure 156: Simple sequence example**

A more complex example is shown in *Figure 157: Example using two sequences* on page 564, where LOOP.CNT>0 . In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                  PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (1 << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                                                  PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 1;
NRF_PWM0->SEQ[0].ENDDELAY = 1;
NRF_PWM0->SEQ[1].PTR  = ((uint32_t)(seq1_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[1].CNT  = ((sizeof(seq1_ram) / sizeof(uint16_t)) <<
                                                  PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[1].REFRESH  = 0;
NRF_PWM0->SEQ[1].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

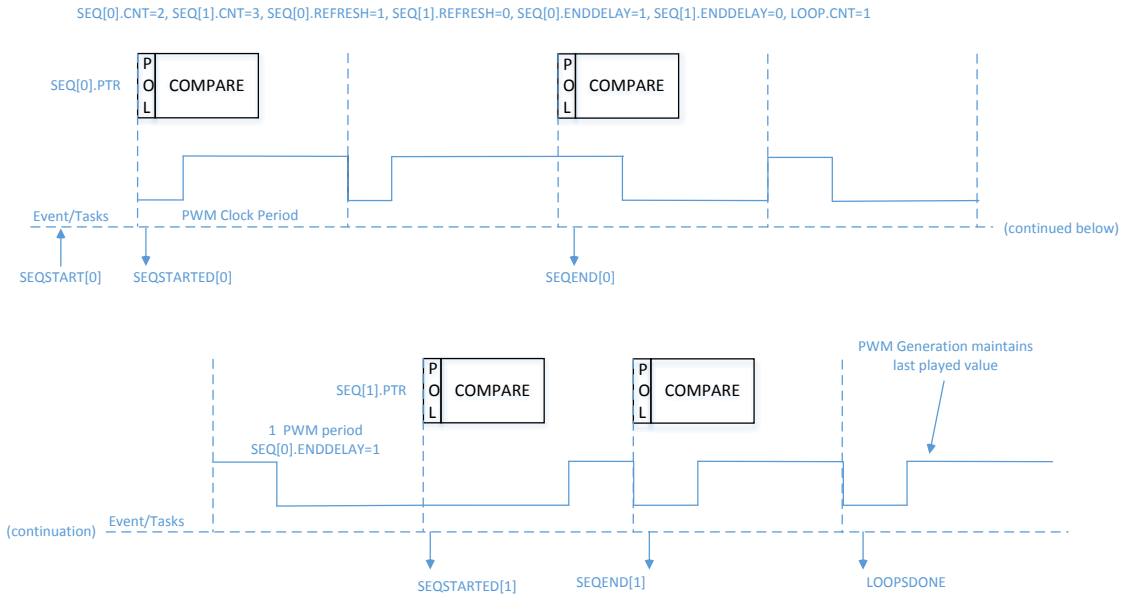



**Figure 157: Example using two sequences**

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- Influence of registers on the sequence
- Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.

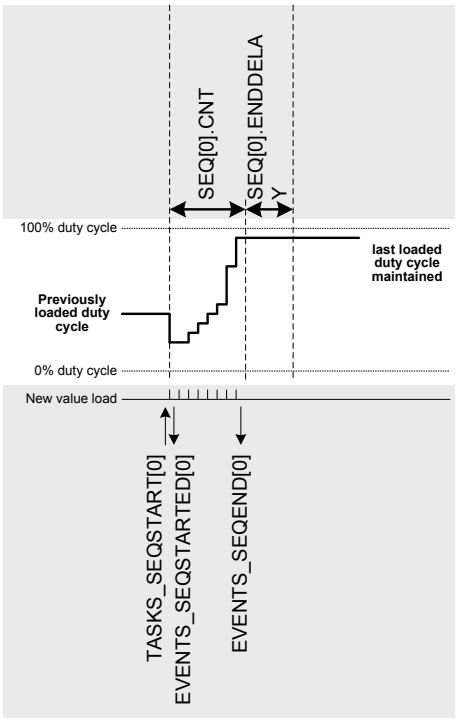



**Figure 158: Single shot (LOOP.CNT=0)**

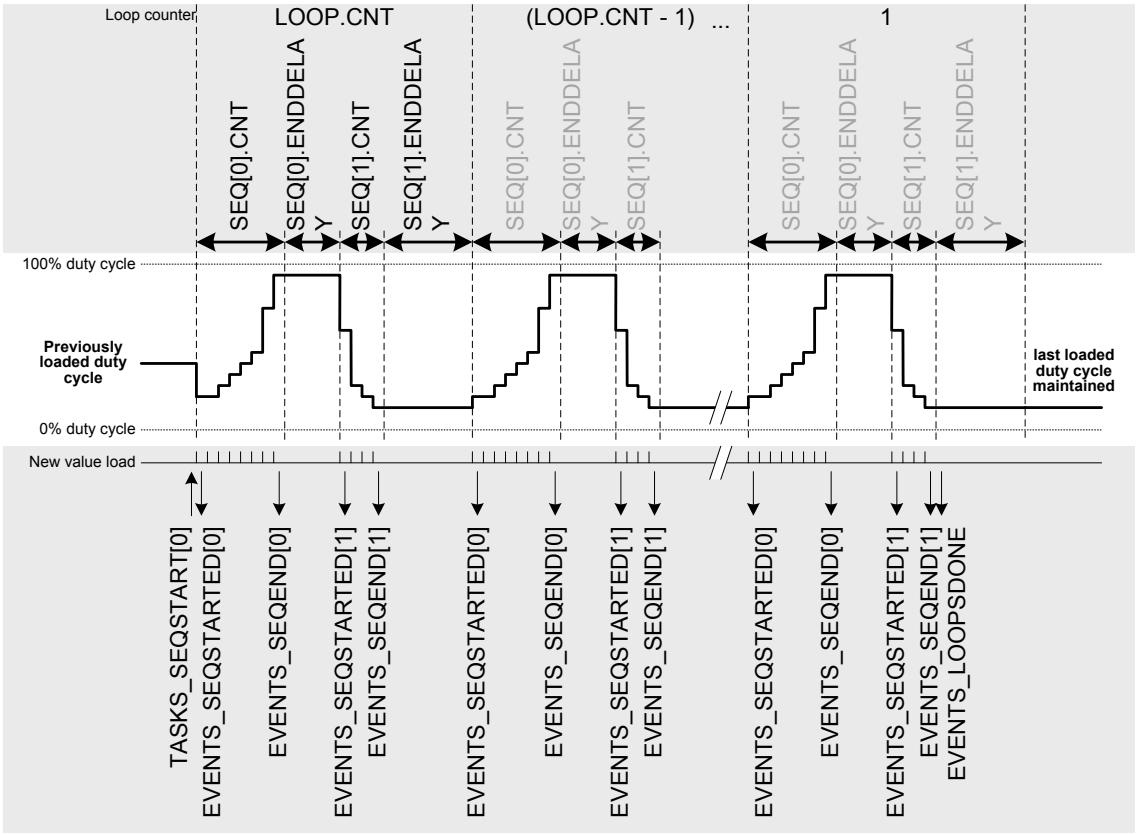



**Figure 159: Complex sequence (LOOP.CNT>0) starting with SEQ[0]**

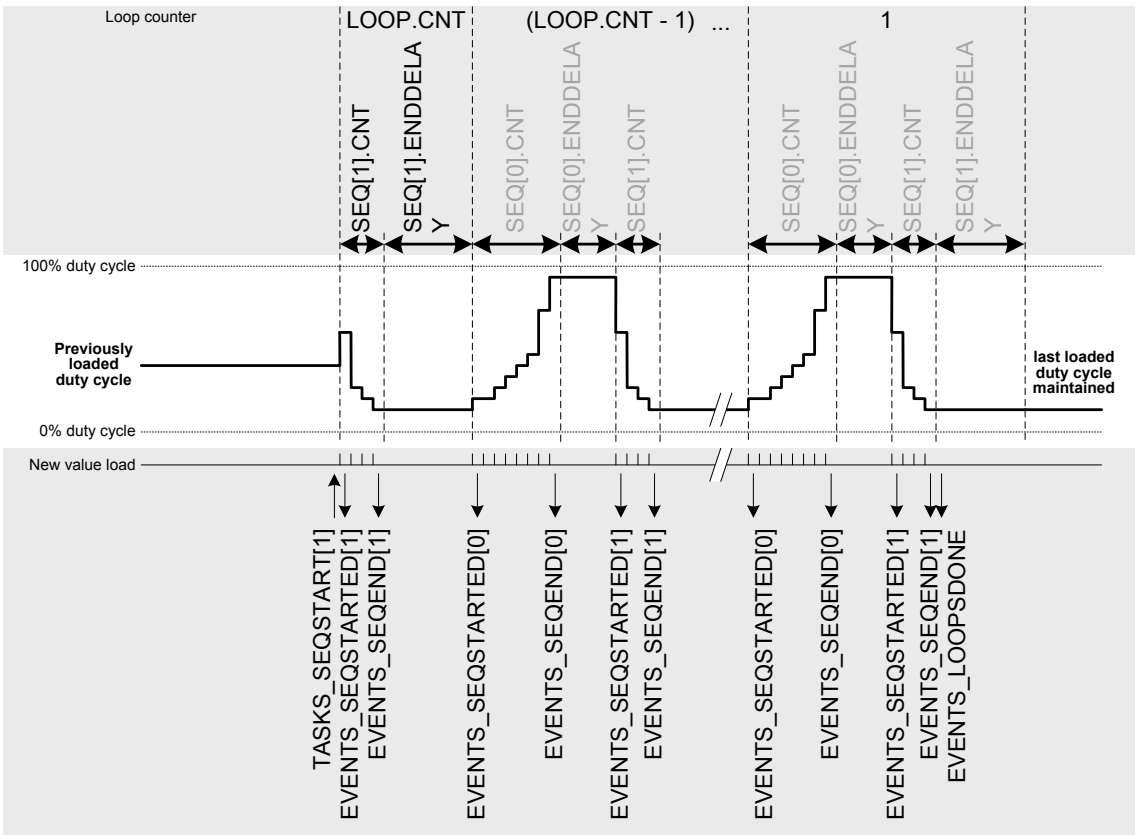



**Figure 160: Complex sequence (LOOP.CNT>0) starting with SEQ[1]**

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0 .

## 46.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

## 46.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 108: Recommended GPIO configuration before starting PWM generation* on page 567 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

### Table 108: Recommended GPIO configuration before starting PWM generation

| PWM signal | PWM pin | Direction | Output value | Comment |
|---|---|---|---|---|
| OUT[n] | As specified in PSEL.OUT[n] (n=0..3) | Output | 0 | Idle state defined in GPIO->OUT |

## 46.5 Registers

### Table 109: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4001C000 | PWM | PWM0 | Pulse width modulation unit 0 | |
| 0x40021000 | PWM | PWM1 | Pulse width modulation unit 1 | |
| 0x40022000 | PWM | PWM2 | Pulse width modulation unit 2 | |
| 0x4002D000 | PWM | PWM3 | Pulse width modulation unit 3 | |

### Table 110: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STOP | 0x004 | Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback |
| TASKS_SEQSTART[0] | 0x008 | Loads the first PWM value on all enabled channels from sequence 0, and starts playing that sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to start it was not running. |
| TASKS_SEQSTART[1] | 0x00C | Loads the first PWM value on all enabled channels from sequence 1, and starts playing that sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to start it was not running. |
| TASKS_NEXTSTEP | 0x010 | Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start it was not running. |
| EVENTS_STOPPED | 0x104 | Response to STOP task, emitted when PWM pulses are no longer generated |
| EVENTS_SEQSTARTED[0] | 0x108 | First PWM period started on sequence 0 |
| EVENTS_SEQSTARTED[1] | 0x10C | First PWM period started on sequence 1 |
| EVENTS_SEQEND[0] | 0x110 | Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter |
| EVENTS_SEQEND[1] | 0x114 | Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter |
| EVENTS_PWMPERIODEN | 0x118 | Emitted at the end of each PWM period |
| EVENTS_LOOPSDONE | 0x11C | Concatenated sequences have been played the amount of times defined in LOOP.CNT |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | PWM module enable register |
| *MODE* | 0x504 | Selects operating mode of the wave counter |
| *COUNTERTOP* | 0x508 | Value up to which the pulse generator counter counts |
| *PRESCALER* | 0x50C | Configuration for PWM_CLK |
| *DECODER* | 0x510 | Configuration of the decoder |
| *LOOP* | 0x514 | Amount of playback of a loop |
| *SEQ[0].PTR* | 0x520 | Beginning address in Data RAM of this sequence |
| *SEQ[0].CNT* | 0x524 | Amount of values (duty cycles) in this sequence |
| *SEQ[0].REFRESH* | 0x528 | Amount of additional PWM periods between samples loaded into compare register |
| *SEQ[0].ENDDELAY* | 0x52C | Time added after the sequence |
| *SEQ[1].PTR* | 0x540 | Beginning address in Data RAM of this sequence |
| *SEQ[1].CNT* | 0x544 | Amount of values (duty cycles) in this sequence |
| *SEQ[1].REFRESH* | 0x548 | Amount of additional PWM periods between samples loaded into compare register |
| *SEQ[1].ENDDELAY* | 0x54C | Time added after the sequence |
| *PSEL.OUT[0]* | 0x560 | Output pin select for PWM channel 0 |
| *PSEL.OUT[1]* | 0x564 | Output pin select for PWM channel 1 |
| *PSEL.OUT[2]* | 0x568 | Output pin select for PWM channel 2 |
| *PSEL.OUT[3]* | 0x56C | Output pin select for PWM channel 3 |

## 46.5.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SEQEND0_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SEQEND1_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | LOOPSDONE_SEQSTART0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | LOOPSDONE_SEQSTART1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | LOOPSDONE_STOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | SEQSTARTED0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | SEQSTARTED1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | SEQEND0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SEQEND1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | See *EVENTS_SEQEND[1]* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| G | RW | PWMPERIODEND | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for PWMPERIODEND event<br>See *EVENTS_PWMPERIODEND* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| H | RW | LOOPSDONE | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable interrupt for LOOPSDONE event<br>See *EVENTS_LOOPSDONE* | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |

## 46.5.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| B | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for STOPPED event<br>See *EVENTS_STOPPED* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| C | RW | SEQSTARTED0 | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for SEQSTARTED[0] event<br>See *EVENTS_SEQSTARTED[0]* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| D | RW | SEQSTARTED1 | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for SEQSTARTED[1] event<br>See *EVENTS_SEQSTARTED[1]* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| E | RW | SEQEND0 | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for SEQEND[0] event<br>See *EVENTS_SEQEND[0]* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| F | RW | SEQEND1 | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for SEQEND[1] event<br>See *EVENTS_SEQEND[1]* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| G | RW | PWMPERIODEND | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for PWMPERIODEND event<br>See *EVENTS_PWMPERIODEND* | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | Read: Disabled | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | Read: Enabled | | | | | | | |
| H | RW | LOOPSDONE | | | | | | | | | | | | | | | | | | | | | | | | | | Write '1' to Enable interrupt for LOOPSDONE event | | | | | | | |

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | H G F E D C B |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_LOOPSDONE* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 46.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | H G F E D C B |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| B | RW | STOPPED | | | Write '1' to Disable interrupt for STOPPED event |
| | | | | | See *EVENTS_STOPPED* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | SEQSTARTED0 | | | Write '1' to Disable interrupt for SEQSTARTED[0] event |
| | | | | | See *EVENTS_SEQSTARTED[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | SEQSTARTED1 | | | Write '1' to Disable interrupt for SEQSTARTED[1] event |
| | | | | | See *EVENTS_SEQSTARTED[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | SEQEND0 | | | Write '1' to Disable interrupt for SEQEND[0] event |
| | | | | | See *EVENTS_SEQEND[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | SEQEND1 | | | Write '1' to Disable interrupt for SEQEND[1] event |
| | | | | | See *EVENTS_SEQEND[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | PWMPERIODEND | | | Write '1' to Disable interrupt for PWMPERIODEND event |
| | | | | | See *EVENTS_PWMPERIODEND* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | LOOPSDONE | | | Write '1' to Disable interrupt for LOOPSDONE event |
| | | | | | See *EVENTS_LOOPSDONE* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 46.5.5 ENABLE

Address offset: 0x500

PWM module enable register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable PWM module |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disabled |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable |

## 46.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | UPDOWN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Selects up or up and down as wave counter mode |
| | | | Up | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Up counter - edge aligned PWM duty-cycle |
| | | | UpAndDown | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Up and down counter - center aligned PWM duty cycle |

## 46.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x000003FF** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | COUNTERTOP | | [3..32767] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Value up to which the pulse generator counter counts. This register is ignored when DECODER.MODE=WaveForm and only values from RAM will be used. |

## 46.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | PRESCALER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Pre-scaler of PWM_CLK |
| | | | DIV_1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 1 (16MHz) |
| | | | DIV_2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 2 ( 8MHz) |
| | | | DIV_4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 4 ( 4MHz) |
| | | | DIV_8 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 8 ( 2MHz) |
| | | | DIV_16 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 16 ( 1MHz) |
| | | | DIV_32 | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 32 ( 500kHz) |
| | | | DIV_64 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 64 ( 250kHz) |
| | | | DIV_128 | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Divide by 128 ( 125kHz) |

## 46.5.9 DECODER

Address offset: 0x510

Configuration of the decoder

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | B | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOAD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | How a sequence is read from RAM and spread to the compare register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Common | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1st half word (16-bit) used in all PWM channels 0..3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Grouped | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1st half word (16-bit) used in channel 0..1; 2nd word in channel 2..3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Individual | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in ch.3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | WaveForm | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in COUNTERTOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Selects source for advancing the active sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | RefreshCount | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | SEQ[n].REFRESH is used to determine loading internal compare registers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NextStep | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | NEXTSTEP task causes a new value to be loaded to internal compare registers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Amount of playback of pattern cycles | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Looping disabled (stop at the end of the sequence) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of this sequence

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Beginning address in Data RAM of this sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in this sequence

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Amount of values (duty cycles) in this sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sequence is disabled, and shall not be started as it is empty | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded into compare register

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000001** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | Amount of additional PWM periods between samples loaded into compare register (load every REFRESH.CNT+1 PWM periods) | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Continuous | 0 | | | | | | | Update every PWM period | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | Time added after the sequence in PWM periods | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of this sequence

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | Beginning address in Data RAM of this sequence | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in this sequence

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | Amount of values (duty cycles) in this sequence | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | Sequence is disabled, and shall not be started as it is empty | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded into compare register

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000001** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | Amount of additional PWM periods between samples loaded into compare register (load every REFRESH.CNT+1 PWM periods) | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Continuous | 0 | | | | | | | Update every PWM period | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C

Time added after the sequence

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | | Time added after the sequence in PWM periods | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | Pin number | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | Connection | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | Connect | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | Pin number | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | Connection | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | Connect | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | Pin number | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | Port number | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | Connection | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | Disconnect | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | Connect | | | | | | | | | | | | | | | | | | | | | | | |

## 46.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | | | | | | | | **Value** | | | | | | | | | | | | | | | | | | **Description** | | | | | |
| A | RW | PIN | | | | | | | | | [0..31] | | | | | | | | | | | | | | | | | | Pin number | | | | | |
| B | RW | PORT | | | | | | | | | [0..1] | | | | | | | | | | | | | | | | | | Port number | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | Connection | | | | | |
| | | | Disconnected | | | | | | | | 1 | | | | | | | | | | | | | | | | | | Disconnect | | | | | |
| | | | Connected | | | | | | | | 0 | | | | | | | | | | | | | | | | | | Connect | | | | | |

# 46.6 Electrical specification

## 46.6.1 PWM Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{PWM,16MHz}$ | PWM run current, Prescaler set to DIV_1 (16 MHz), excluding DMA and GPIO | | 200 | | µA |
| $I_{PWM,8MHz}$ | PWM run current, Prescaler set to DIV_2 (8 MHz), excluding DMA and GPIO | | 100 | | µA |
| $I_{PWM,125kHz}$ | PWM run current, Prescaler set to DIV_128 (125 kHz), excluding DMA and GPIO | | 50 | | µA |

# 47 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

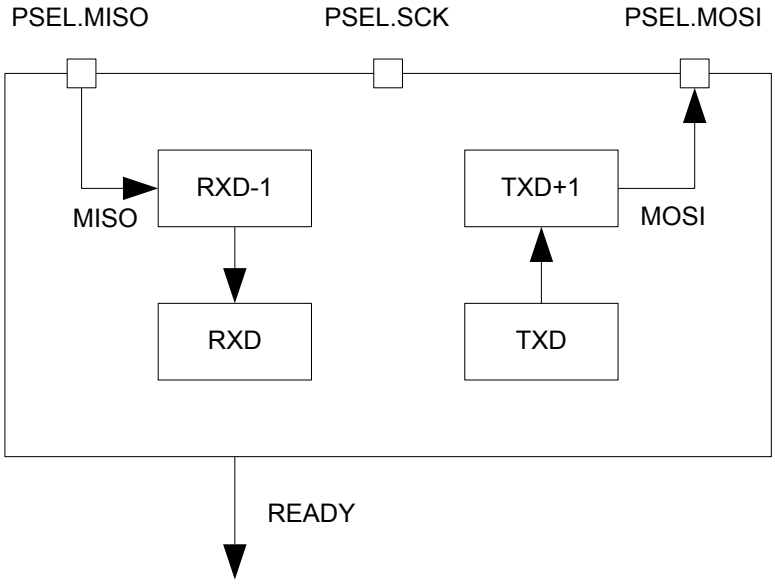



**Figure 161: SPI master**

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

## 47.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

**Table 111: SPI modes**

| Mode | Clock polarity CPOL | Clock phase CPHA |
|---|---|---|
| SPI_MODE | 0 (Leading) | 0 (Active High) |
| SPI_MODE | 0 (Leading) | 1 (Active Low) |
| SPI_MODE | 1 (Trailing) | 0 (Active High) |
| SPI_MODE | 1 (Trailing) | 1 (Active Low) |

### 47.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated SPI master signal is not connected to any physical pin. The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 112: GPIO configuration* on page 577 prior to enabling the SPI. The SCK must

always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

**Table 112: GPIO configuration**

| SPI master signal | SPI master pin | Direction | Output value |
|---|---|---|---|
| SCK | As specified in PSEL.SCK | Output | Same as CONFIG.CPOL |
| MOSI | As specified in PSEL.MOSI | Output | 0 |
| MISO | As specified in PSEL.MISO | Input | Not applicable |

### 47.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

### 47.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 162: SPI master transaction* on page 578. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.

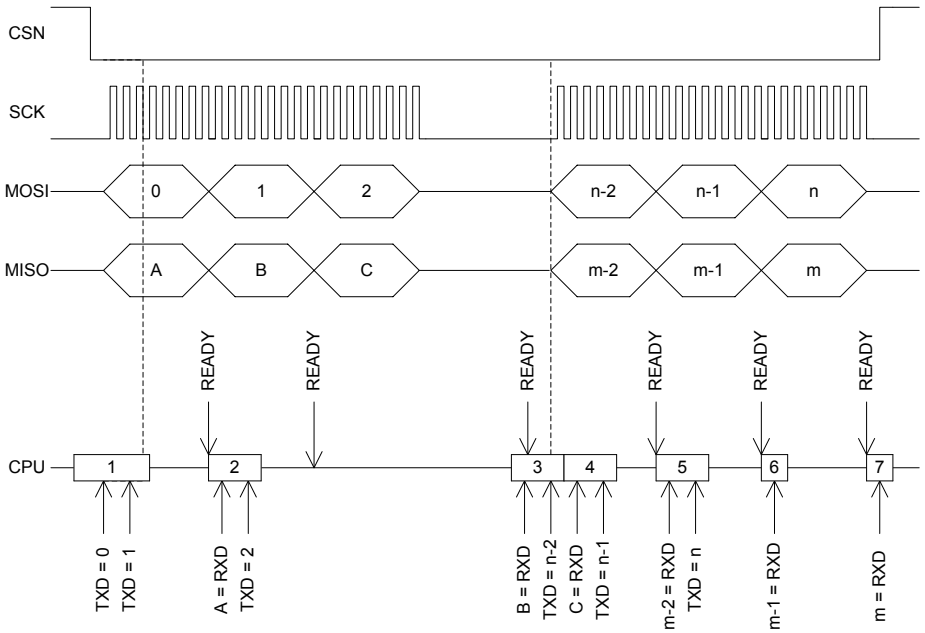



**Figure 162: SPI master transaction**

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 163: SPI master transaction* on page 578. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

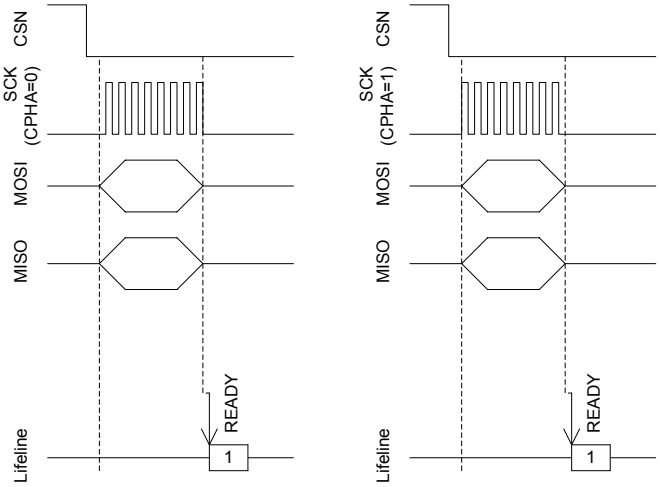



**Figure 163: SPI master transaction**

# 47.2 Registers

### Table 113: Instances

| Base address | Peripheral | Instance | Description | Configuration | |
|---|---|---|---|---|---|
| 0x40003000 | SPI | SPI0 | SPI master 0 | | Deprecated |
| 0x40004000 | SPI | SPI1 | SPI master 1 | | Deprecated |
| 0x40023000 | SPI | SPI2 | SPI master 2 | | Deprecated |

### Table 114: Register Overview

| Register | Offset | Description |
|---|---|---|
| EVENTS_READY | 0x108 | TXD byte sent and RXD byte received |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | Enable SPI |
| *PSEL.SCK* | 0x508 | Pin select for SCK |
| *PSEL.MOSI* | 0x50C | Pin select for MOSI signal |
| *PSEL.MISO* | 0x510 | Pin select for MISO signal |
| *RXD* | 0x518 | RXD register |
| *TXD* | 0x51C | TXD register |
| *FREQUENCY* | 0x524 | SPI frequency. Accuracy depends on the HFCLK source selected. |
| *CONFIG* | 0x554 | Configuration register |

## 47.2.1 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | |
| **Reset 0x00000000** | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | Write '1' to Enable interrupt for READY event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | |
| **Reset 0x00000000** | | | | | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READY | | | Write '1' to Disable interrupt for READY event | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | See *EVENTS_READY* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | Disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.2.3 ENABLE

Address offset: 0x500

Enable SPI

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ENABLE | | | Enable or disable SPI |
| | | | Disabled | 0 | Disable SPI |
| | | | Enabled | 1 | Enable SPI |

## 47.2.4 PSEL.SCK

Address offset: 0x508

Pin select for SCK

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 47.2.5 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI signal

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 47.2.6 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 47.2.7 RXD

Address offset: 0x518

RXD register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | RX data received. Double buffered | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.2.8 TXD

Address offset: 0x51C

TXD register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TXD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | TX data to send. Double buffered | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.2.9 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x04000000** | | | | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | FREQUENCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | SPI master data rate | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K125 | 0x02000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 125 kbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K250 | 0x04000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 250 kbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K500 | 0x08000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 500 kbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M1 | 0x10000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1 Mbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M2 | 0x20000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 2 Mbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M4 | 0x40000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 4 Mbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | M8 | 0x80000000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 8 Mbps | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.2.10 CONFIG

Address offset: 0x554

Configuration register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ORDER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Bit order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | MsbFirst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Most significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LsbFirst | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Least significant bit shifted out first | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | CPHA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) phase | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Leading | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on leading edge of clock, shift serial data on trailing edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Trailing | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Sample on trailing edge of clock, shift serial data on leading edge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CPOL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Serial clock (SCK) polarity | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveHigh | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active high | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ActiveLow | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Active low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 47.3 Electrical specification

### 47.3.1 SPI master interface electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{SPI}$ | Bit rates for SPI[36] | | | 8[37] | Mbps |
| $I_{SPI,2Mbps}$ | Run current for SPI, 2 Mbps | | | 50 | µA |
| $I_{SPI,8Mbps}$ | Run current for SPI, 8 Mbps | | | 50 | µA |
| $I_{SPI,IDLE}$ | Idle current for SPI (STARTed, no CSN activity) | | <1 | | µA |
| $t_{SPI,START}$ | Time from writing TXD register to transmission started | | 1 | | µs |

### 47.3.2 Serial Peripheral Interface (SPI) Master timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{SPI,CSCK}$ | SCK period | 125 | | | ns |
| $t_{SPI,RSCK,LD}$ | SCK rise time, standard drive[a] | | | $t_{RF,25pF}$ | |
| $t_{SPI,RSCK,HD}$ | SCK rise time, high drive[a] | | | $t_{HRF,25pF}$ | |
| $t_{SPI,FSCK,LD}$ | SCK fall time, standard drive[a] | | | $t_{RF,25pF}$ | |
| $t_{SPI,FSCK,HD}$ | SCK fall time, high drive[a] | | | $t_{HRF,25pF}$ | |
| $t_{SPI,WHSCK}$ | SCK high time[a] | $(0.5*t_{CSCK})$ – $t_{RSCK}$ | | | |
| $t_{SPI,WLSCK}$ | SCK low time[a] | $(0.5*t_{CSCK})$ – $t_{FSCK}$ | | | |
| $t_{SPI,SUMI}$ | MISO to CLK edge setup time | 19 | | | ns |
| $t_{SPI,HMI}$ | CLK edge to MISO hold time | 18 | | | ns |
| $t_{SPI,VMO}$ | CLK edge to MOSI valid | | | 59 | ns |
| $t_{SPI,HMO}$ | MOSI hold time after CLK edge | 20 | | | ns |

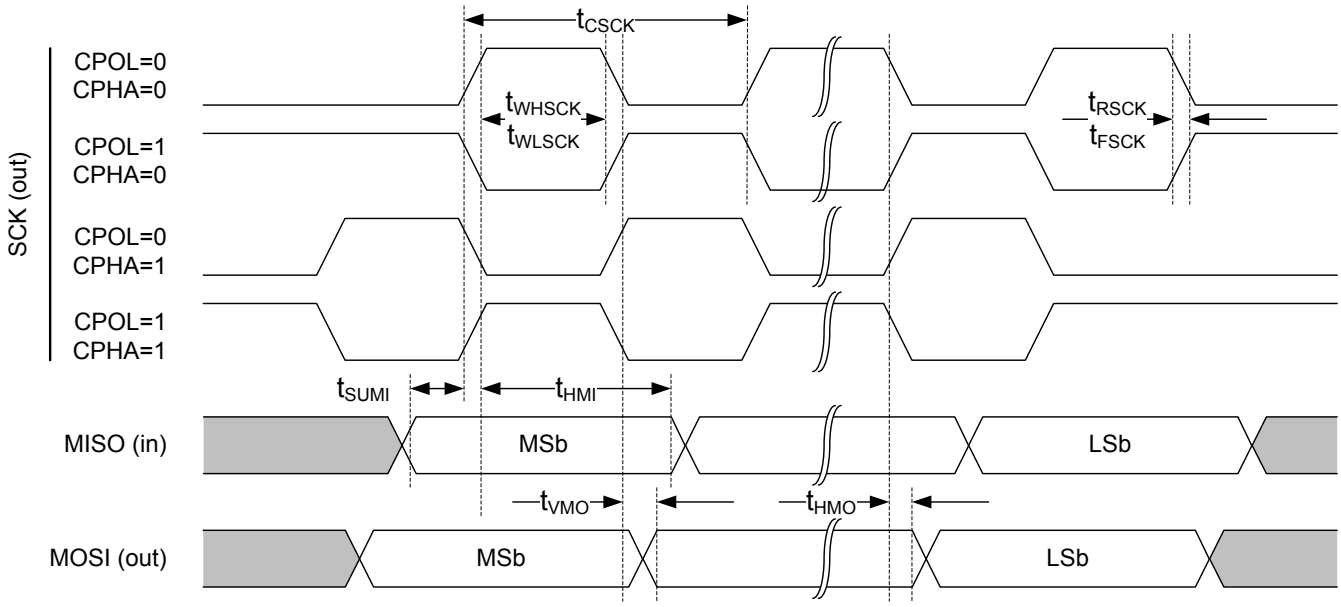



**Figure 164: SPI master timing diagram**

[36] High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
[37] The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.
[a] At 25pF load, including GPIO capacitance, see GPIO spec.

# 48 TWI — I2C compatible two-wire interface

The TWI master is compatible with I2C operating at 100 kHz and 400 kHz.

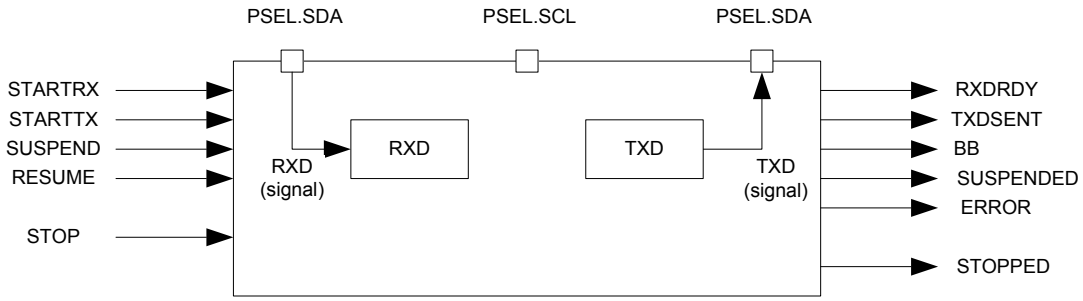



**Figure 165: TWI master's main features**

## 48.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, *Figure 165: TWI master's main features* on page 583.

A TWI setup comprising one master and three slaves is illustrated in *Figure 166: A typical TWI setup comprising one master and three slaves* on page 583. This TWI master is only able to operate as the only master on the TWI bus.

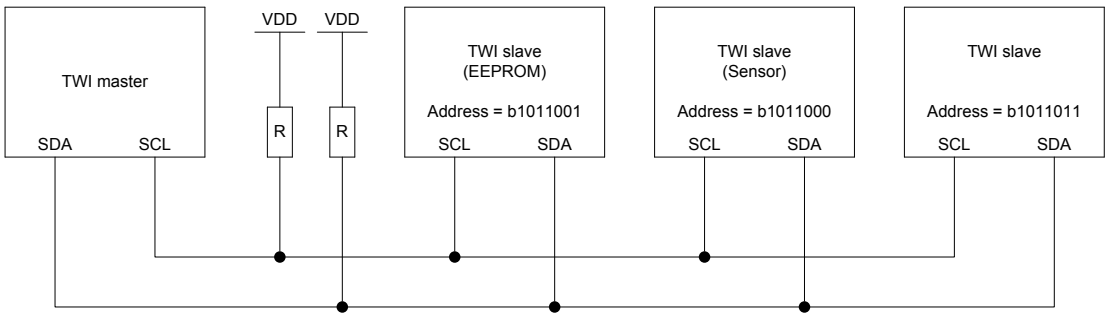



**Figure 166: A typical TWI setup comprising one master and three slaves**

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

## 48.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated TWI signal is not connected to any physical pin. The PSEL.SCL and PSEL.SDA registers and their configurations are

only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCL and PSEL.SDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 115: GPIO configuration* on page 584.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

**Table 115: GPIO configuration**

| TWI master signal | TWI master pin | Direction | Drive strength | Output value |
|---|---|---|---|---|
| SCL | As specified in PSEL.SCL | Input | S0D1 | Not applicable |
| SDA | As specified in PSEL.SDA | Input | S0D1 | Not applicable |

## 48.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI.

## 48.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 167: The TWI master writing data to a slave* on page 585. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.

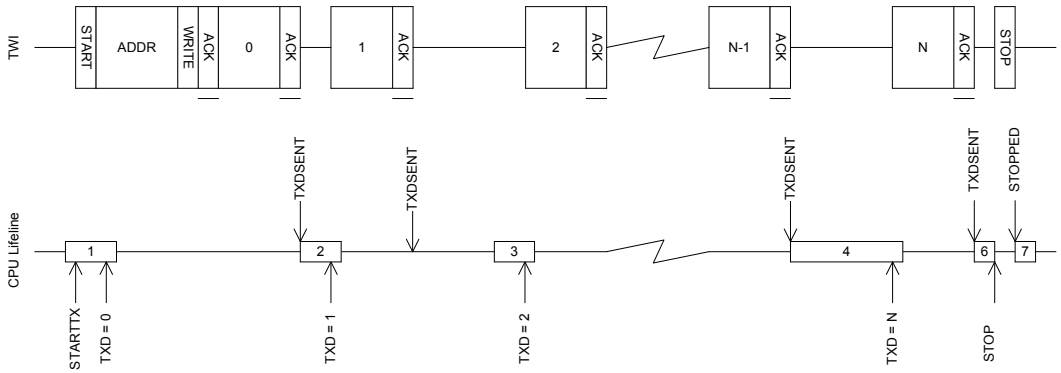



**Figure 167: The TWI master writing data to a slave**

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

## 48.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 168: The TWI master reading data from a slave* on page 586. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.

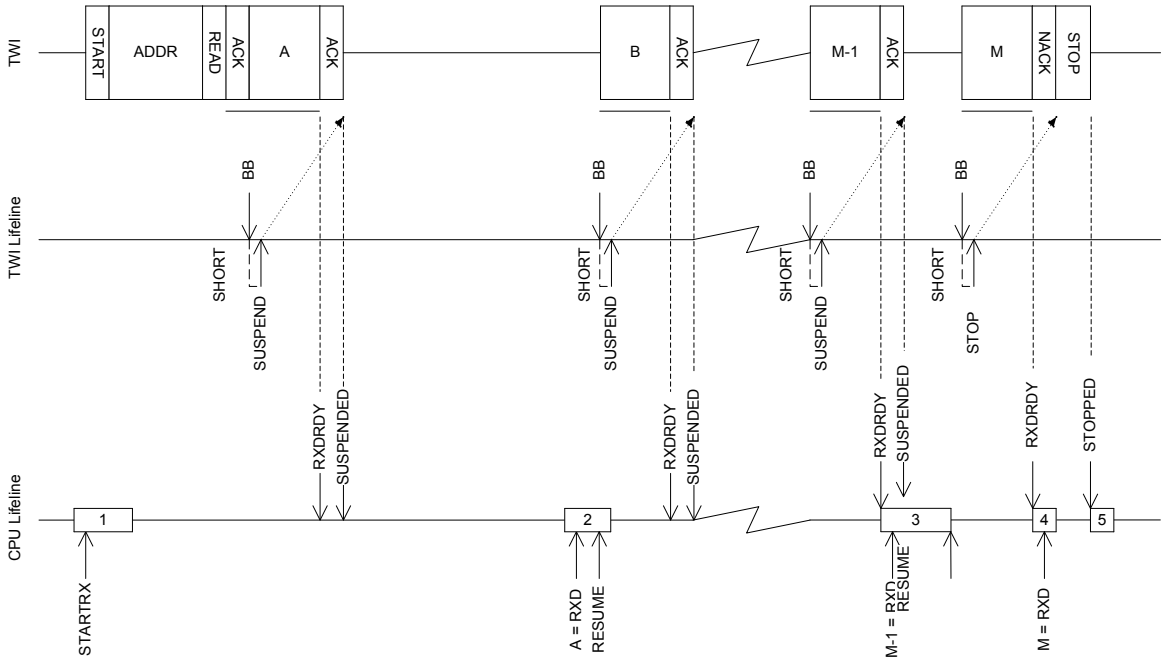



**Figure 168: The TWI master reading data from a slave**

## 48.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

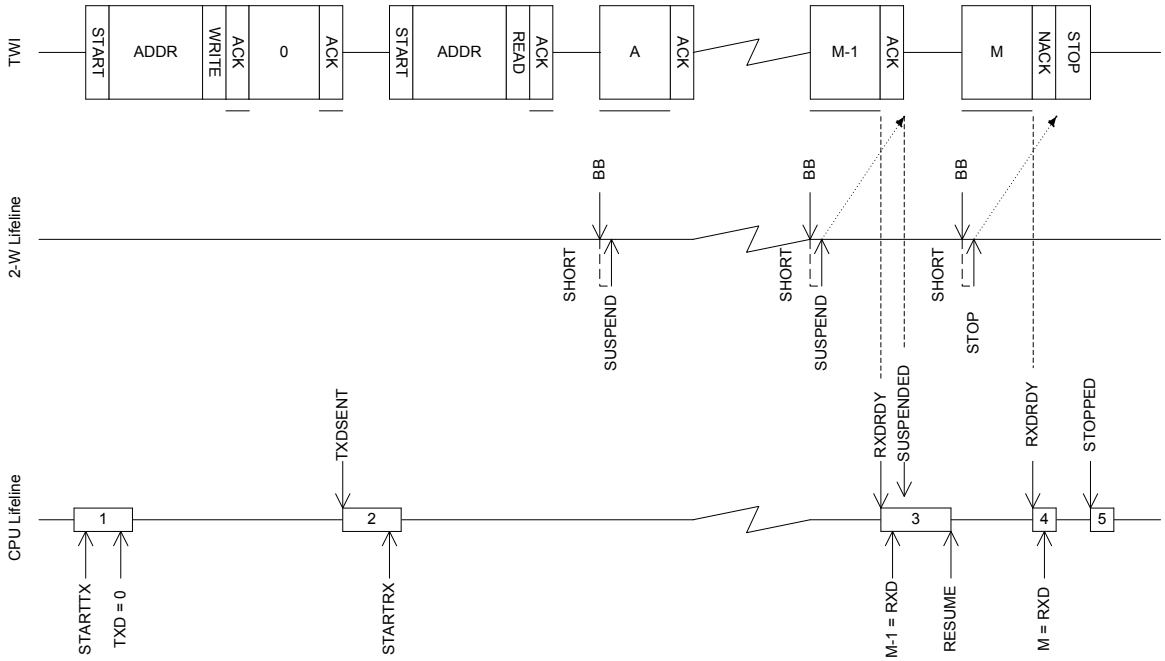



**Figure 169: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between**

To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

## 48.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

## 48.8 Registers

### Table 116: Instances

| Base address | Peripheral | Instance | Description | Configuration | |
|---|---|---|---|---|---|
| 0x40003000 | TWI | TWI0 | Two-wire interface master 0 | | Deprecated |
| 0x40004000 | TWI | TWI1 | Two-wire interface master 1 | | Deprecated |

### Table 117: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTRX | 0x000 | Start TWI receive sequence |
| TASKS_STARTTX | 0x008 | Start TWI transmit sequence |
| TASKS_STOP | 0x014 | Stop TWI transaction |
| TASKS_SUSPEND | 0x01C | Suspend TWI transaction |
| TASKS_RESUME | 0x020 | Resume TWI transaction |
| EVENTS_STOPPED | 0x104 | TWI stopped |
| EVENTS_RXDREADY | 0x108 | TWI RXD byte received |
| EVENTS_TXDSENT | 0x11C | TWI TXD byte sent |
| EVENTS_ERROR | 0x124 | TWI error |
| EVENTS_BB | 0x138 | TWI byte boundary, generated before each byte that is sent or received |
| EVENTS_SUSPENDED | 0x148 | TWI entered the suspended state |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSRC* | 0x4C4 | Error source |
| *ENABLE* | 0x500 | Enable TWI |
| *PSEL.SCL* | 0x508 | Pin select for SCL |
| *PSEL.SDA* | 0x50C | Pin select for SDA |
| *RXD* | 0x518 | RXD register |
| *TXD* | 0x51C | TXD register |
| *FREQUENCY* | 0x524 | TWI frequency. Accuracy depends on the HFCLK source selected. |
| *ADDRESS* | 0x588 | Address used in the TWI transfer |

### 48.8.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | BB_SUSPEND | | | Shortcut between BB event and SUSPEND task |

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | B A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_BB* and *TASKS_SUSPEND* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | BB_STOP | | | Shortcut between BB event and STOP task<br><br>See *EVENTS_BB* and *TASKS_STOP* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 48.8.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | F E D C B A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | STOPPED | | | Write '1' to Enable interrupt for STOPPED event<br><br>See *EVENTS_STOPPED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW | RXDREADY | | | Write '1' to Enable interrupt for RXDREADY event<br><br>See *EVENTS_RXDREADY* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW | TXDSENT | | | Write '1' to Enable interrupt for TXDSENT event<br><br>See *EVENTS_TXDSENT* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW | ERROR | | | Write '1' to Enable interrupt for ERROR event<br><br>See *EVENTS_ERROR* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| E | RW | BB | | | Write '1' to Enable interrupt for BB event<br><br>See *EVENTS_BB* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | SUSPENDED | | | Write '1' to Enable interrupt for SUSPENDED event<br><br>See *EVENTS_SUSPENDED* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 48.8.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | F | | | | E | | | | | D | | C | | | | | | B | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | RXDREADY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | TXDSENT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | BB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | SUSPENDED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 48.8.4 ERRORSRC

Address offset: 0x4C4

Error source

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OVERRUN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | ANACK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | DNACK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 48.8.5 ENABLE

Address offset: 0x500

Enable TWI

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 48.8.6 PSEL.SCL

Address offset: 0x508

Pin select for SCL

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 48.8.7 PSEL.SDA

Address offset: 0x50C

Pin select for SDA

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 48.8.8 RXD

Address offset: 0x518

RXD register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 48.8.9 TXD

Address offset: 0x51C

TXD register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | TXD | | | | | | | | | | | | | | | | | | | | | | | | | | TXD register | | | | | | | |

## 48.8.10 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x04000000** | | | | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | FREQUENCY | | | | | | | | | | | | | | | | | | | | | | | | | | TWI master clock frequency | | | | | | | |
| | | | K100 | 0x01980000 | | | | | | | | | | | | | | | | | | | | | | | | 100 kbps | | | | | | | |
| | | | K250 | 0x04000000 | | | | | | | | | | | | | | | | | | | | | | | | 250 kbps | | | | | | | |
| | | | K400 | 0x06680000 | | | | | | | | | | | | | | | | | | | | | | | | 400 kbps (actual rate 410.256 kbps) | | | | | | | |

## 48.8.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | ADDRESS | | | | | | | | | | | | | | | | | | | | | | | | | | Address used in the TWI transfer | | | | | | | |

# 48.9 Electrical specification

## 48.9.1 TWI interface electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{TWI,SCL}$ | Bit rates for TWI[38] | 100 | | 400 | kbps |
| $I_{TWI,100kbps}$ | Run current for TWI, 100 kbps | | 50 | | µA |
| $I_{TWI,400kbps}$ | Run current for TWI, 400 kbps | | 50 | | µA |
| $t_{TWI,START}$ | Time from STARTRX/STARTTX task to transmission started | | 1.5 | | µs |

## 48.9.2 Two Wire Interface (TWI) timing specifications

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWI,SU\_DAT}$ | Data setup time before positive edge on SCL – all modes | 300 | | | ns |
| $t_{TWI,HD\_DAT}$ | Data hold time after negative edge on SCL – all modes | 500 | | | ns |
| $t_{TWI,HD\_STA,100kbps}$ | TWI master hold time for START and repeated START condition, 100 kbps | 10000 | | | ns |
| $t_{TWI,HD\_STA,250kbps}$ | TWI master hold time for START and repeated START condition, 250kbps | 4000 | | | ns |
| $t_{TWI,HD\_STA,400kbps}$ | TWI master hold time for START and repeated START condition, 400 kbps | 2500 | | | ns |
| $t_{TWI,SU\_STO,100kbps}$ | TWI master setup time from SCL high to STOP condition, 100 kbps | 5000 | | | ns |
| $t_{TWI,SU\_STO,250kbps}$ | TWI master setup time from SCL high to STOP condition, 250 kbps | 2000 | | | ns |

[38] High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{TWI,SU\_STO,400kbps}$ | TWI master setup time from SCL high to STOP condition, 400 kbps | 1250 | | | ns |
| $t_{TWI,BUF,100kbps}$ | TWI master bus free time between STOP and START conditions, 100 kbps | 5800 | | | ns |
| $t_{TWI,BUF,250kbps}$ | TWI master bus free time between STOP and START conditions, 250 kbps | 2700 | | | ns |
| $t_{TWI,BUF,400kbps}$ | TWI master bus free time between STOP and START conditions, 400 kbps | 2100 | | | ns |

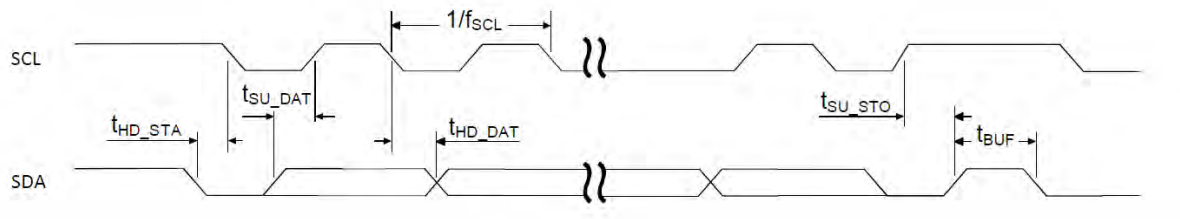



**Figure 170: TWI timing diagram, 1 byte transaction**

# 49 UART — Universal asynchronous receiver/ transmitter

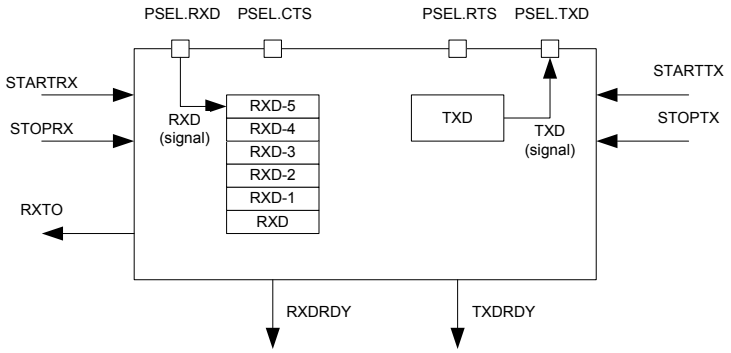



**Figure 171: UART configuration**

## 49.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in *Figure 171: UART configuration* on page 593, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

## 49.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated UART signal will not be connected to any physical pin. The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.CTS, PSEL.RTS and PSEL.TXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 593.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

**Table 118: GPIO configuration**

| UART pin | Direction | Output value |
|---|---|---|
| RXD | Input | Not applicable |
| CTS | Input | Not applicable |
| RTS | Output | 1 |
| TXD | Output | 1 |

## 49.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

## 49.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 172: UART transmission* on page 594.
A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see *Suspending the UART* on page 595.

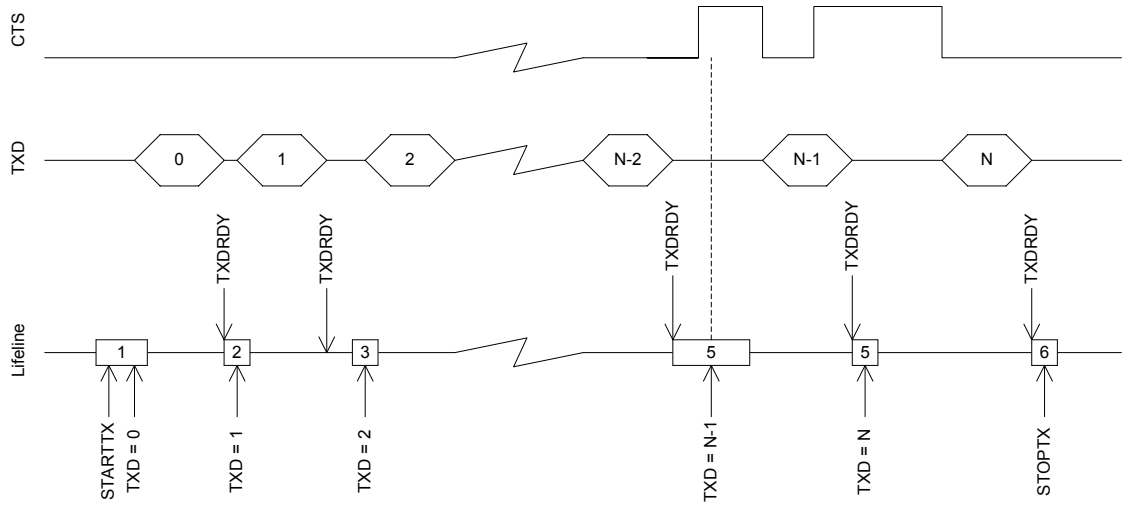



**Figure 172: UART transmission**

## 49.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.

The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 173: UART reception* on page 595.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 173: UART reception* on page 595. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

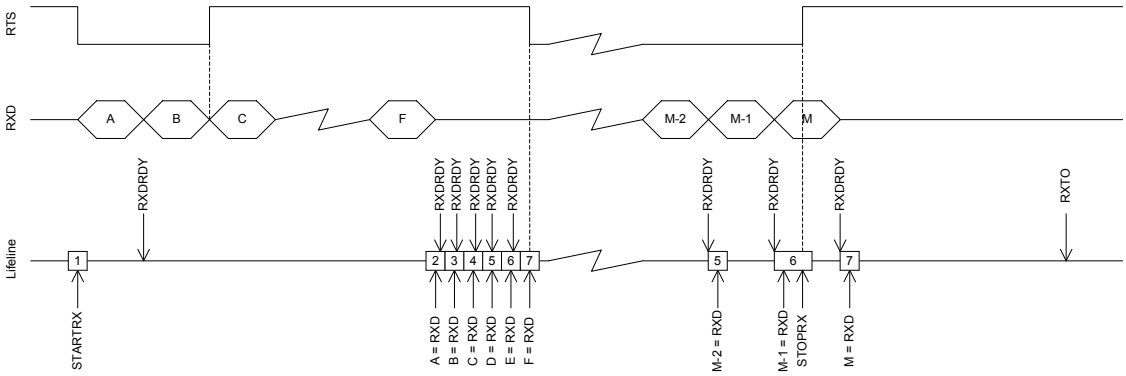



**Figure 173: UART reception**

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

## 49.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

## 49.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

## 49.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

## 49.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

## 49.10 Registers

### Table 119: Instances

| Base address | Peripheral | Instance | Description | Configuration | |
|---|---|---|---|---|---|
| 0x40002000 | UART | UART0 | Universal asynchronous receiver/ transmitter | | Deprecated |

### Table 120: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTRX | 0x000 | Start UART receiver |
| TASKS_STOPRX | 0x004 | Stop UART receiver |
| TASKS_STARTTX | 0x008 | Start UART transmitter |
| TASKS_STOPTX | 0x00C | Stop UART transmitter |
| TASKS_SUSPEND | 0x01C | Suspend UART |
| EVENTS_CTS | 0x100 | CTS is activated (set low). Clear To Send. |
| EVENTS_NCTS | 0x104 | CTS is deactivated (set high). Not Clear To Send. |
| EVENTS_RXDRDY | 0x108 | Data received in RXD |
| EVENTS_TXDRDY | 0x11C | Data sent from TXD |
| EVENTS_ERROR | 0x124 | Error detected |
| EVENTS_RXTO | 0x144 | Receiver timeout |
| *SHORTS* | 0x200 | Shortcut register |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ERRORSRC* | 0x480 | Error source |
| *ENABLE* | 0x500 | Enable UART |
| *PSEL.RTS* | 0x508 | Pin select for RTS |
| *PSEL.TXD* | 0x50C | Pin select for TXD |
| *PSEL.CTS* | 0x510 | Pin select for CTS |
| *PSEL.RXD* | 0x514 | Pin select for RXD |
| *RXD* | 0x518 | RXD register |
| *TXD* | 0x51C | TXD register |
| *BAUDRATE* | 0x524 | Baud rate. Accuracy depends on the HFCLK source selected. |
| *CONFIG* | 0x56C | Configuration of parity and hardware flow control |

### 49.10.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | | | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CTS_STARTRX | | | Shortcut between CTS event and STARTRX task |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NCTS_STOPRX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | F | | | | | | | | E | | D | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NCTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | TXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RXTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | F | | | | | | | | E | | D | | | | | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | NCTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | TXDRDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | RXTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.4 ERRORSRC

Address offset: 0x480

Error source

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OVERRUN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PARITY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotPresent | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Present | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | FRAMING | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | | | A valid stop bit is not detected on the serial data input after all bits in a character have been received. |
| | | | NotPresent | 0 | Read: error not present |
| | | | Present | 1 | Read: error present |
| D | RW | BREAK | | | Break condition<br>The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.). |
| | | | NotPresent | 0 | Read: error not present |
| | | | Present | 1 | Read: error present |

## 49.10.5 ENABLE

Address offset: 0x500

Enable UART

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ENABLE | | | Enable or disable UART |
| | | | Disabled | 0 | Disable UART |
| | | | Enabled | 4 | Enable UART |

## 49.10.6 PSEL.RTS

Address offset: 0x508

Pin select for RTS

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 49.10.7 PSEL.TXD

Address offset: 0x50C

Pin select for TXD

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B A A A A A |
| **Reset 0xFFFFFFFF** | | | | **1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | PIN | | [0..31] | Pin number |
| B | RW | PORT | | [0..1] | Port number |
| C | RW | CONNECT | | | Connection |
| | | | Disconnected | 1 | Disconnect |
| | | | Connected | 0 | Connect |

## 49.10.8 PSEL.CTS

Address offset: 0x510

Pin select for CTS

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | Pin number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | Connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | Connect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.9 PSEL.RXD

Address offset: 0x514

Pin select for RXD

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | Pin number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | Port number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | Connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | Disconnect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | Connect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.10 RXD

Address offset: 0x518

RXD register

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RXD | | | RX data received in previous transfers, double buffered | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.11 TXD

Address offset: 0x51C

TXD register

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | TXD | | | TX data to be transferred | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 49.10.12 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x04000000** | | | **0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | BAUDRATE | | | Baud rate |
| | | | Baud1200 | 0x0004F000 | 1200 baud (actual rate: 1205) |
| | | | Baud2400 | 0x0009D000 | 2400 baud (actual rate: 2396) |
| | | | Baud4800 | 0x0013B000 | 4800 baud (actual rate: 4808) |
| | | | Baud9600 | 0x00275000 | 9600 baud (actual rate: 9598) |
| | | | Baud14400 | 0x003B0000 | 14400 baud (actual rate: 14414) |
| | | | Baud19200 | 0x004EA000 | 19200 baud (actual rate: 19208) |
| | | | Baud28800 | 0x0075F000 | 28800 baud (actual rate: 28829) |
| | | | Baud31250 | 0x00800000 | 31250 baud |
| | | | Baud38400 | 0x009D5000 | 38400 baud (actual rate: 38462) |
| | | | Baud56000 | 0x00E50000 | 56000 baud (actual rate: 55944) |
| | | | Baud57600 | 0x00EBF000 | 57600 baud (actual rate: 57762) |
| | | | Baud76800 | 0x013A9000 | 76800 baud (actual rate: 76923) |
| | | | Baud115200 | 0x01D7E000 | 115200 baud (actual rate: 115942) |
| | | | Baud230400 | 0x03AFB000 | 230400 baud (actual rate: 231884) |
| | | | Baud250000 | 0x04000000 | 250000 baud |
| | | | Baud460800 | 0x075F7000 | 460800 baud (actual rate: 470588) |
| | | | Baud921600 | 0x0EBED000 | 921600 baud (actual rate: 941176) |
| | | | Baud1M | 0x10000000 | 1Mega baud |

### 49.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

| Bit number | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| Id | | | B B B A |
| **Reset 0x00000000** | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | HWFC | | | Hardware flow control |
| | | | Disabled | 0 | Disabled |
| | | | Enabled | 1 | Enabled |
| B | RW | PARITY | | | Parity |
| | | | Excluded | 0x0 | Exclude parity bit |
| | | | Included | 0x7 | Include parity bit |

## 49.11 Electrical specification

### 49.11.1 UART electrical specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{UART}$ | Baud rate for UART[39]. | | | 1000 | kbps |
| $I_{UART1M}$ | Run current at max baud rate. | | 55 | | µA |
| $I_{UART115k}$ | Run current at 115200 bps. | | 55 | | µA |
| $I_{UART1k2}$ | Run current at 1200 bps. | | 55 | | µA |
| $I_{UART,IDLE}$ | Idle current for UART | | 1 | | µA |
| $t_{UART,CTSH}$ | CTS high time | 1 | | | µs |
| $t_{UART,START}$ | Time from STARTRX/STARTTX task to transmission started | | 1 | | µs |

[39] High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

# 50 ACL — Access control lists

The Access control lists (ACL) peripheral is designed to assign and enforce access permissions to different regions of the on-chip flash memory map.

Flash memory regions can be assigned individual ACL permission schemes. The following registers are involved:

- PERM register, where the permissions are configured.
- ADDR register, where the word-aligned start address for the flash page is defined.
- SIZE register, where the size of the region the permissions are applied to is determined.

**Important:** The size of the region in bytes is restricted to a multiple of the flash page size. See the *Memory* on page 20 chapter for more information.

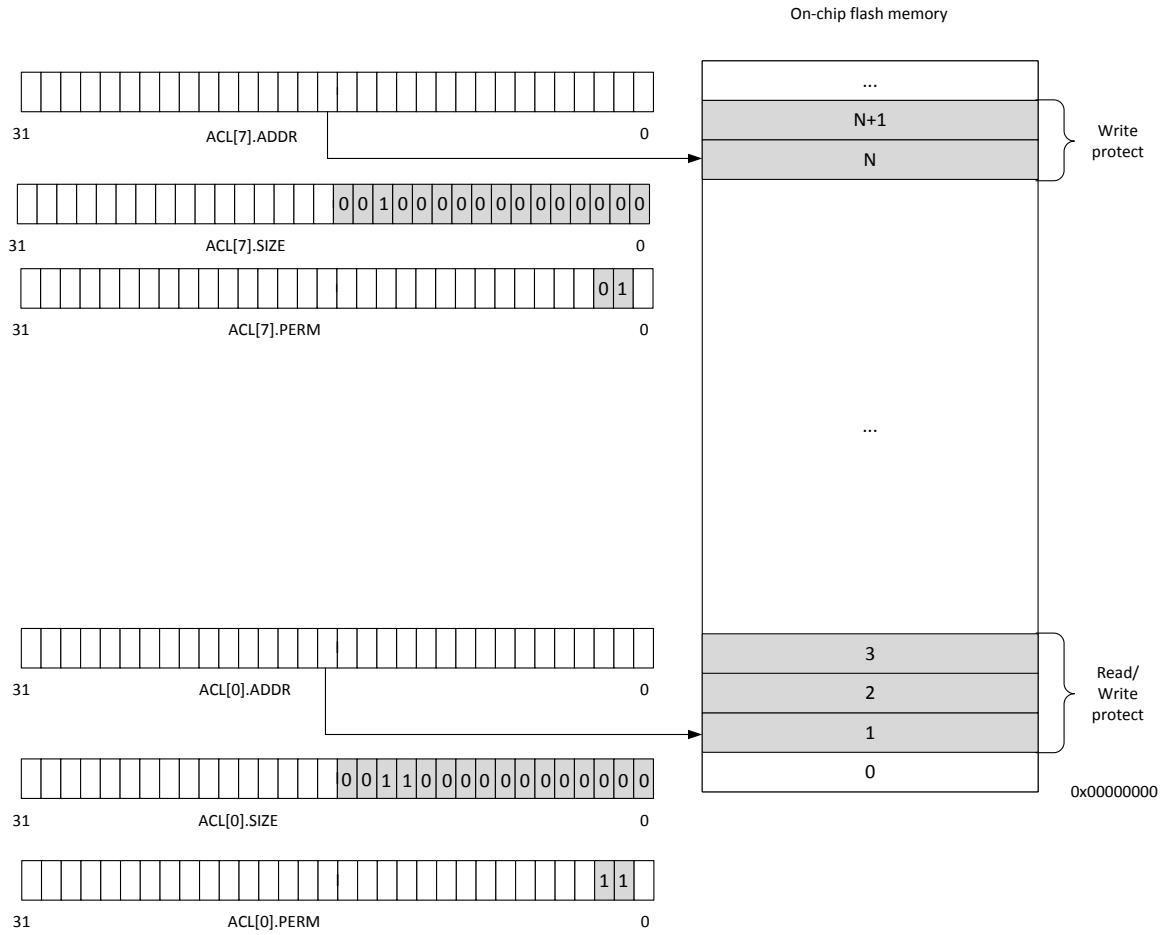



**Figure 174: Protected regions of on-chip flash memory**

There are four defined ACL permission schemes, with different combinations of read/write permissions:

**Table 121: Permission schemes**

| Read | Write | Protection description |
|---|---|---|
| 0 | 0 | No protection. Entire region can be executed, read, written or erased. |
| 0 | 1 | Region can be executed and read, but not written or erased. |
| 1 | 0 | Region can be written and erased, but not executed or read. |
| 1 | 1 | Region is locked for all access until next reset. |

**Important:** If a permission violation to a protected region is detected by the ACL peripheral, the request is blocked and a Bus Fault exception is triggered.

Access control to a configured region is enforced by the hardware two CPU clock cycles after the ADDR, SIZE, and PERM registers for an ACL instance have been successfully written. The protection is only enforced if a valid start address of the flash page boundary is written into the ADDR register, and the values of the SIZE and PERM registers are not zero.

The ADDR, SIZE, and PERM registers can only be written once. All ACL configuration registers are cleared on reset (by resetting the device from any reset source), which is also the only way of clearing the configuration registers. To ensure that the desired permission schemes are always enforced by the ACL peripheral, the device boot sequence must perform the necessary configuration.

Debugger read access to a read-protected region will be Read-As-Zero (RAZ), while debugger write access to a write-protected region will be Write-Ignored (WI).

## 50.1 Registers

### Table 122: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x4001E000 | ACL | ACL | Access control lists | |

### Table 123: Register Overview

| Register | Offset | Description | |
|---|---|---|---|
| *ACL[0].ADDR* | 0x800 | Configure the word-aligned start address of region 0 to protect | |
| *ACL[0].SIZE* | 0x804 | Size of region to protect counting from address ACL[0].ADDR. Write '0' as no effect. | |
| *ACL[0].PERM* | 0x808 | Access permissions for region 0 as defined by start address ACL[0].ADDR and size ACL[0].SIZE | |
| | 0x80C | | Reserved |
| *ACL[1].ADDR* | 0x810 | Configure the word-aligned start address of region 1 to protect | |
| *ACL[1].SIZE* | 0x814 | Size of region to protect counting from address ACL[1].ADDR. Write '0' as no effect. | |
| *ACL[1].PERM* | 0x818 | Access permissions for region 1 as defined by start address ACL[1].ADDR and size ACL[1].SIZE | |
| | 0x81C | | Reserved |
| *ACL[2].ADDR* | 0x820 | Configure the word-aligned start address of region 2 to protect | |
| *ACL[2].SIZE* | 0x824 | Size of region to protect counting from address ACL[2].ADDR. Write '0' as no effect. | |
| *ACL[2].PERM* | 0x828 | Access permissions for region 2 as defined by start address ACL[2].ADDR and size ACL[2].SIZE | |
| | 0x82C | | Reserved |
| *ACL[3].ADDR* | 0x830 | Configure the word-aligned start address of region 3 to protect | |
| *ACL[3].SIZE* | 0x834 | Size of region to protect counting from address ACL[3].ADDR. Write '0' as no effect. | |
| *ACL[3].PERM* | 0x838 | Access permissions for region 3 as defined by start address ACL[3].ADDR and size ACL[3].SIZE | |
| | 0x83C | | Reserved |
| *ACL[4].ADDR* | 0x840 | Configure the word-aligned start address of region 4 to protect | |
| *ACL[4].SIZE* | 0x844 | Size of region to protect counting from address ACL[4].ADDR. Write '0' as no effect. | |
| *ACL[4].PERM* | 0x848 | Access permissions for region 4 as defined by start address ACL[4].ADDR and size ACL[4].SIZE | |
| | 0x84C | | Reserved |
| *ACL[5].ADDR* | 0x850 | Configure the word-aligned start address of region 5 to protect | |
| *ACL[5].SIZE* | 0x854 | Size of region to protect counting from address ACL[5].ADDR. Write '0' as no effect. | |
| *ACL[5].PERM* | 0x858 | Access permissions for region 5 as defined by start address ACL[5].ADDR and size ACL[5].SIZE | |
| | 0x85C | | Reserved |
| *ACL[6].ADDR* | 0x860 | Configure the word-aligned start address of region 6 to protect | |
| *ACL[6].SIZE* | 0x864 | Size of region to protect counting from address ACL[6].ADDR. Write '0' as no effect. | |
| *ACL[6].PERM* | 0x868 | Access permissions for region 6 as defined by start address ACL[6].ADDR and size ACL[6].SIZE | |
| | 0x86C | | Reserved |
| *ACL[7].ADDR* | 0x870 | Configure the word-aligned start address of region 7 to protect | |
| *ACL[7].SIZE* | 0x874 | Size of region to protect counting from address ACL[7].ADDR. Write '0' as no effect. | |
| *ACL[7].PERM* | 0x878 | Access permissions for region 7 as defined by start address ACL[7].ADDR and size ACL[7].SIZE | |
| | 0x87C | | Reserved |

### 50.1.1 ACL[0].ADDR

Address offset: 0x800

Configure the word-aligned start address of region 0 to protect

This register can only be written once.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ADDR | | | Valid word-aligned start address of region 0 to protect. Address must point to a flash page boundary. |

## 50.1.2 ACL[0].SIZE

Address offset: 0x804

Size of region to protect counting from address ACL[0].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Size of flash region 0 in bytes. Must be a multiple of the flash page size. |

## 50.1.3 ACL[0].PERM

Address offset: 0x808

Access permissions for region 0 as defined by start address ACL[0].ADDR and size ACL[0].SIZE

This register can only be written once.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| B | RW | WRITE | | | Configure write and erase permissions for region 0. Write '0' has no effect. |
| | | | Enable | 0 | Allow write and erase instructions to region 0 |
| | | | Disable | 1 | Block write and erase instructions to region 0 |
| C | RW | READ | | | Configure read permissions for region 0. Write '0' has no effect. |
| | | | Enable | 0 | Allow read instructions to region 0 |
| | | | Disable | 1 | Block read instructions to region 0 |

## 50.1.4 ACL[1].ADDR

Address offset: 0x810

Configure the word-aligned start address of region 1 to protect

This register can only be written once.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ADDR | | | Valid word-aligned start address of region 1 to protect. Address must point to a flash page boundary. |

## 50.1.5 ACL[1].SIZE

Address offset: 0x814

Size of region to protect counting from address ACL[1].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Size of flash region 1 in bytes. Must be a multiple of the flash page size. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.6 ACL[1].PERM

Address offset: 0x818

Access permissions for region 1 as defined by start address ACL[1].ADDR and size ACL[1].SIZE

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure write and erase permissions for region 1. Write '0' has no effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Allow write and erase instructions to region 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Block write and erase instructions to region 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure read permissions for region 1. Write '0' has no effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Allow read instructions to region 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Block read instructions to region 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.7 ACL[2].ADDR

Address offset: 0x820

Configure the word-aligned start address of region 2 to protect

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Valid word-aligned start address of region 2 to protect. Address must point to a flash page boundary. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.8 ACL[2].SIZE

Address offset: 0x824

Size of region to protect counting from address ACL[2].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Size of flash region 2 in bytes. Must be a multiple of the flash page size. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.9 ACL[2].PERM

Address offset: 0x828

Access permissions for region 2 as defined by start address ACL[2].ADDR and size ACL[2].SIZE

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.10 ACL[3].ADDR

Address offset: 0x830

Configure the word-aligned start address of region 3 to protect

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.11 ACL[3].SIZE

Address offset: 0x834

Size of region to protect counting from address ACL[3].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 50.1.12 ACL[3].PERM

Address offset: 0x838

Access permissions for region 3 as defined by start address ACL[3].ADDR and size ACL[3].SIZE

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 50.1.13 ACL[4].ADDR

Address offset: 0x840

Configure the word-aligned start address of region 4 to protect

This register can only be written once.

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR | | | Valid word-aligned start address of region 4 to protect. Address must point to a flash page boundary. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 50.1.14 ACL[4].SIZE

Address offset: 0x844

Size of region to protect counting from address ACL[4].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | Size of flash region 4 in bytes. Must be a multiple of the flash page size. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 50.1.15 ACL[4].PERM

Address offset: 0x848

Access permissions for region 4 as defined by start address ACL[4].ADDR and size ACL[4].SIZE

This register can only be written once.

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITE | | | Configure write and erase permissions for region 4. Write '0' has no effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | Allow write and erase instructions to region 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | Block write and erase instructions to region 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | READ | | | Configure read permissions for region 4. Write '0' has no effect. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | Allow read instructions to region 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | Block read instructions to region 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 50.1.16 ACL[5].ADDR

Address offset: 0x850

Configure the word-aligned start address of region 5 to protect

This register can only be written once.

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR | | | Valid word-aligned start address of region 5 to protect. Address must point to a flash page boundary. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### 50.1.17 ACL[5].SIZE

Address offset: 0x854

Size of region to protect counting from address ACL[5].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Size of flash region 5 in bytes. Must be a multiple of the flash page size.

### 50.1.18 ACL[5].PERM

Address offset: 0x858

Access permissions for region 5 as defined by start address ACL[5].ADDR and size ACL[5].SIZE

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Configure write and erase permissions for region 5. Write '0' has no effect.

| | | | |
|---|---|---|---|
| | Enable | 0 | Allow write and erase instructions to region 5 |
| | Disable | 1 | Block write and erase instructions to region 5 |
| C | RW READ | | Configure read permissions for region 5. Write '0' has no effect. |
| | Enable | 0 | Allow read instructions to region 5 |
| | Disable | 1 | Block read instructions to region 5 |

### 50.1.19 ACL[6].ADDR

Address offset: 0x860

Configure the word-aligned start address of region 6 to protect

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ADDR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Valid word-aligned start address of region 6 to protect. Address must point to a flash page boundary.

### 50.1.20 ACL[6].SIZE

Address offset: 0x864

Size of region to protect counting from address ACL[6].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Size of flash region 6 in bytes. Must be a multiple of the flash page size.

### 50.1.21 ACL[6].PERM

Address offset: 0x868

Access permissions for region 6 as defined by start address ACL[6].ADDR and size ACL[6].SIZE

This register can only be written once.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| B | RW | WRITE | | | Configure write and erase permissions for region 6. Write '0' has no effect. |
| | | | Enable | 0 | Allow write and erase instructions to region 6 |
| | | | Disable | 1 | Block write and erase instructions to region 6 |
| C | RW | READ | | | Configure read permissions for region 6. Write '0' has no effect. |
| | | | Enable | 0 | Allow read instructions to region 6 |
| | | | Disable | 1 | Block read instructions to region 6 |

### 50.1.22 ACL[7].ADDR

Address offset: 0x870

Configure the word-aligned start address of region 7 to protect

This register can only be written once.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | ADDR | | | Valid word-aligned start address of region 7 to protect. Address must point to a flash page boundary. |

### 50.1.23 ACL[7].SIZE

Address offset: 0x874

Size of region to protect counting from address ACL[7].ADDR. Write '0' as no effect.

This register can only be written once.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | SIZE | | | Size of flash region 7 in bytes. Must be a multiple of the flash page size. |

### 50.1.24 ACL[7].PERM

Address offset: 0x878

Access permissions for region 7 as defined by start address ACL[7].ADDR and size ACL[7].SIZE

This register can only be written once.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | C B |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| B | RW | WRITE | | | Configure write and erase permissions for region 7. Write '0' has no effect. |
| | | | Enable | 0 | Allow write and erase instructions to region 7 |
| | | | Disable | 1 | Block write and erase instructions to region 7 |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | READ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 51 USBD — Universal serial bus device

The USB device controller (USBD) implements a full speed USB device function that meets 2.0 revision of the USB specification.

Listed here are the main features for USBD:

- Fully compliant to *Universal Serial Bus Specification Revision 2.0* Full Speed part, including following Engineering Change Notices (ECNs) issued by USB Implementers Forum:
  - Pull-up/pull-down Resistors ECN
  - 5V Short Circuit Withstand Requirement Change ECN
- Implements a USB FS (full speed, 12 Mbps) device
- USB device stack available in the Nordic SDK
- On-chip transceiver
- Software controlled on-chip pull-up on D+
- 2 control (1 IN , 1 OUT), 14 bulk/interrupt (7 IN , 7 OUT) and 2 ISO (1 IN, 1 OUT) endpoints
- Supports double buffering for isochronous endpoint (IN/OUT)
- EasyDMA for all data transfers
- 64 bytes buffer size for each bulk/interrupt endpoint
- Up to 1023 bytes buffer size for ISO endpoints

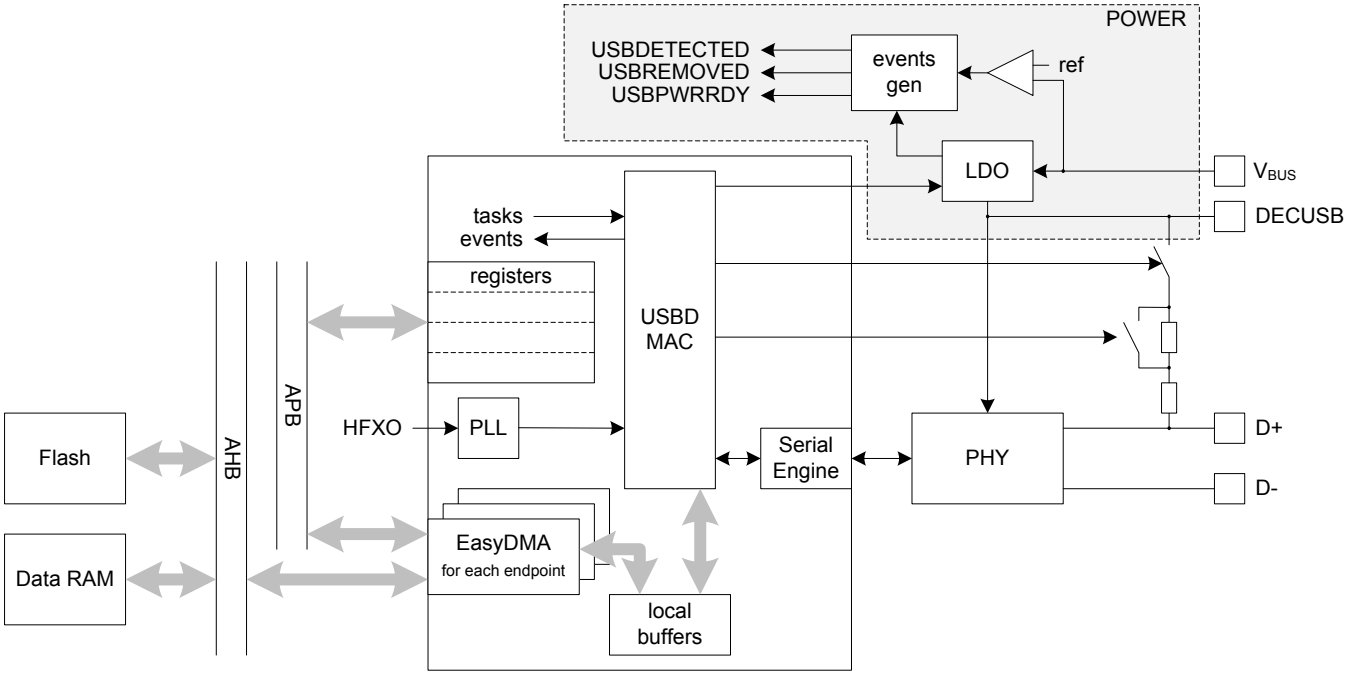



**Figure 175: USB block diagram**

## 51.1 USB device states

The behaviour of a USB device can be modelled through a state diagram.

**Chapter 9 USB Device Framework** in the USB specification revision 2.0 defines a number of states for a USB device, illustrated below.

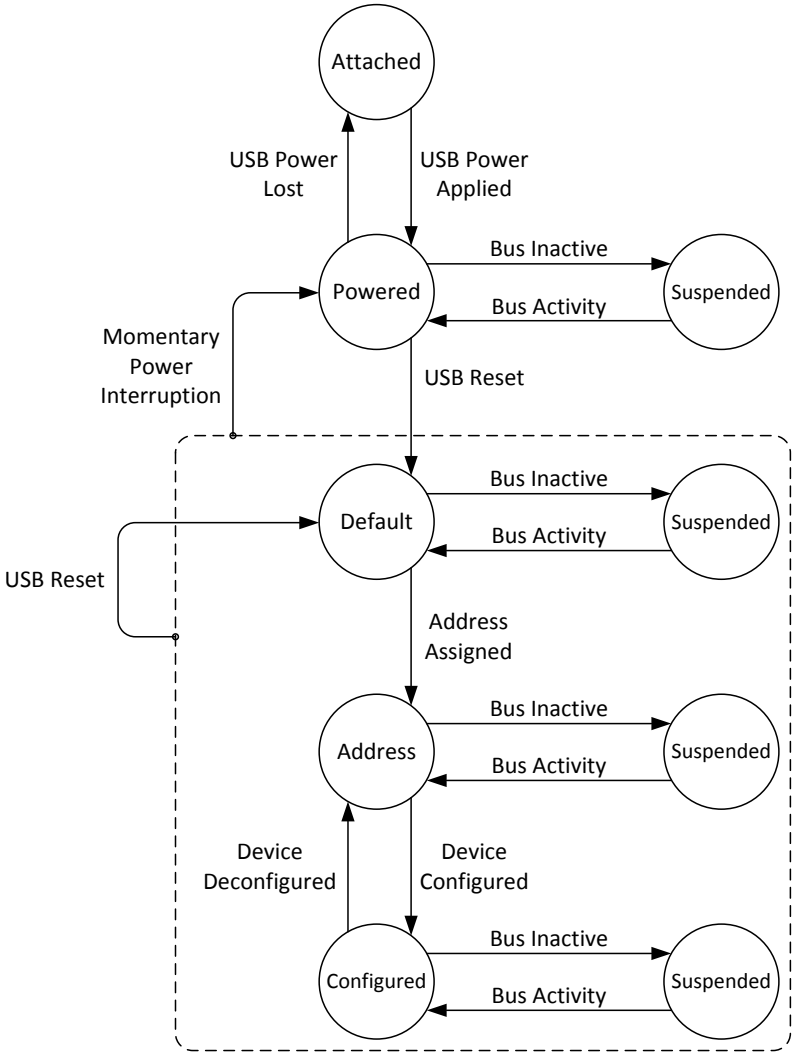



**Figure 176: Device state diagram**

The device must change state according to host-initiated traffic and USB bus states.

It is up to the software to implement a state machine that matches the above definition.

To detect the presence or absence of USB supply ($V_{BUS}$), the *POWER* chapter defines two events USBDETECTED and USBREMOVED, they can be used to implement the state machine.

As a general rule when implementing the software, the host behavior shall never be assumed to be predictable, in particular the sequence of commands received during an enumeration. The software shall always react to the current bus conditions or commands sent by the host.

## 51.2 USB terminology

The USB specification defines bus states, rather than logic levels on the D+ and D- lines.

For a full speed device, the bus state where the D+ line is high and the D- line is low is defined as the J state. The bus state where D+ is low and D- high is called the K state.

An idle bus, where D+ and D- lines are only polarized through the pull-up on D+ and pull-downs on the host side, will be in J state.

Both lines low are called SE0 (single-ended 0), and both lines high SE1 (single-ended 1).

## 51.3 USB pins

The USBD peripheral features a number of dedicated pins.

For more information about the pinout, please refer to *Pin assignments* on page 13.

The dedicated USB pins can be grouped in two categories: signal and power.

For details on the USB power supply and $V_{BUS}$ detection, refer to the *POWER* chapter.

The signal pins consist of the D+ and D- pins, which are to be connected to the USB host. They are dedicated pins, and not available as standard GPIOs.

The USBD implements the "5V Short Circuit Withstand ECN", which amends the original USB 2.0 Specification. This means that these two pins are not 5 V tolerant.

The signal pins and the pull-up will operate only while $V_{BUS}$ is in its valid voltage range, and USBD is enabled through the *ENABLE* register.

## 51.4 USBD start-up sequence

The PHY of the USBD is powered separately from the rest of the device ($V_{BUS}$ pin), which has some implications on the USBD power up sequence.

The device is not able to properly signal its presence to the USB host, and handle traffic from the host, unless the PHY's power supply is enabled and stable.

The turning on or off of the PHY's power supply is directly linked to the *ENABLE* register. The device provides events that help synchronizing software to the various steps during the power up sequence.

It is recommended to enable USBD only after $V_{BUS}$ has been detected, and turn on the USB pull-up after a USBPWRRDY event has occurred, and after a USBEVENT has occurred with the READY condition flagged in *EVENTCAUSE*. This ensures that all resources in USBD are available and the dedicated USB voltage regulator has stabilized.

Below sequence chart illustrates a typical handling of $V_{BUS}$ power up.

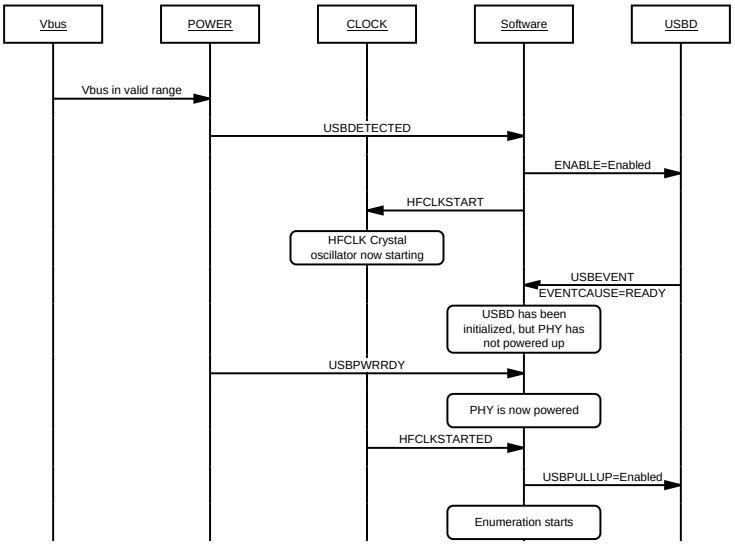



**Figure 177: $V_{BUS}$ power up sequence**

Upon detection of $V_{BUS}$ removal, signalled by the USBREMOVED event described in the *POWER* chapter, it is recommended to let on-going EasyDMA transfers finish (wait for the relevant ENDEPIN[n], ENDISOIN, ENDEPOUT[n] or ENDISOOUT event, see *EasyDMA* on page 616), then to disable USBD through writing ENABLE = Disabled .

## 51.5 USB pull-up

The USB pull-up serves two purposes: it indicates to the host that the device is connected to the USB bus, and indicates the device's speed grade.

When no pull-up is connected to the USB bus, the host sees both D+ and D- lines low, as they are pulled down on the host side by 15 kOhm resistors. The device is not seen by the host, and hence defined to be in detached state, even though it could be physically connected to the host. USB spec does not allow to draw any current on $V_{BUS}$ in that situation.

When a full-speed device connects its 1.5 kOhm pull-up to D+, the host sees the corresponding line high. The device is then in attached state. The host may attempt to determine if the device supports higher speeds (which it does not), and will then initiate communication with the device to further identify it; this process is called enumeration.

If the host supports higher speed grades and the device is full-speed, the host may attempt to determine if that device is capable of higher speeds. The USBD peripheral implemented in this device supports only full-speed (12 Mbps), and will ignore the negotiation for higher speeds, in accordance with the USB specification revision 2.0, full speed part.

The *USBPULLUP* register provides means to connect or disconnect the pull-up on D+ under software control. This allows the software to control when USB enumeration takes place. It also allows to emulate a physical disconnect from the USB bus, for instance when re-enumeration is required.

*USBPULLUP* has to be set to Enabled to allow the USBD to handle USB traffic and generate appropriate events. This forbids the use of an external pull-up.

Note that disconnecting the pull-up through the *USBPULLUP* register while connected to a host will result in both D+ and D- lines to be pulled low by the host's pull-down resistors. However, as mentioned above, this will also inhibit the generation of the USBRESET event.

The pull-up is disabled by default after a chip reset.

The pull-up shall only get connected after USBD has been enabled through the *ENABLE* register. Attempting to access the *USBPULLUP* register prior to that will lead to an ACCESSFAULT event to get generated.

The USB pull-up value is automatically changed depending on bus activity, as specified in the "Resistor ECN" which amends the original USB Specification v2.0 . The user does not have access to this function, it is handled in hardware.

While they should never be used in normal traffic activity, the task DPDMDRIVE allows at any time to force the D+ and D- lines to the state specified in the *DPDMVALUE* register. The DPDMNODRIVE task stops driving them, and the PHY returns to normal operation.

## 51.6 USB reset

The USB specification defines a USB reset, which shall not be confused with a chip reset.

The USB reset results from a single-ended low state (SE0) on the D+ / D- lines for a time $T_{DETRST}$, as specified in the USB specification chapter 7. Only the host is allowed to drive a USB reset condition on the bus.

The USB reset is a normal USB bus condition, and is used as part of the enumeration sequence, it does not reset the chip.

The UBSD peripheral automatically interprets a SE0 longer than $t_{USB,DETRST}$ as a USB reset. When the device detects a USB reset and generates a USBRESET event, the device USB stack and related parts of the application shall re-initialize themselves, and go back to the **Default** state.

Some of the registers in the USBD peripheral get automatically reset to a known state, in particular all data endpoints will get disabled, and the *USBADDR* will be reset to 0.

After having been connected to the USB bus (i.e. after $V_{BUS}$ gets applied), the device shall not respond to any traffic from the time the pull-up is enabled until it has seen a USB reset condition. This is automatically ensured by the USBD.

After a USB reset, the device shall be fully responsive after at most $T_{RSTRCY}$ (as per USB specification chapter 7). Software shall take into account that it takes $t_{USB,RSTRCY}$ for the hardware to recover from a USB reset condition.

## 51.7 USB suspend and resume

Normally, the host will maintain activity on the USB at least every millisecond per USB specification.

To signal that the device shall go into low power mode, the host stops activity on the USB bus, which becomes idle, only the device pull-up and host pull-downs act on D+ and D-, and the bus is thus kept at a constant J state. It is up to the device to detect this lack of activity, and enter into a low power mode within a specified time.

The USB host can decide at any moment to suspend USB activity. When this happens, the device is obligated per USB specification to enter a low power mode. The host can decide at any moment to resume USB activity, on its own initiative. If Remote WakeUp has been enabled by the host, the device may also issue a RESUME request to wake up the host.

### 51.7.1 Entering suspend

The USBD peripheral automatically detects a lack of activity for more than $t_{USB,SUSPEND}$ and will generate the corresponding USBEVENT event, with SUSPEND bit set in the *EVENTCAUSE* register. The software shall ensure that the current drawn from the USB supply line $V_{BUS}$ is within the specified limits before $T_{2SUSP}$ as defined in chapter 7 of the USB specification.

In order to save power, and provided that no other peripheral needs it, the crystal oscillator (HFXO) in CLOCK may be disabled by software during USB suspend, while the USB pull-up is disconnected, or when $V_{BUS}$ is not present. Software must explicitly enable it at any other time. The USBD will not be able to respond to USB traffic unless HFXO is enabled and stable.

### 51.7.2 Host-initiated resume

If the host resumes bus activity with or without a RESUME condition (in other words: bus activity is defined as any non-J state), the USBD peripheral will generate a USBEVENT event, with RESUME bit set in the *EVENTCAUSE* register, and the device has to be responsive to any incoming request on the USB bus within the time $T_{RSMRCY}$ defined in chapter 7 of the USB specification. It is also allowed to revert to normal power consumption mode.

If the host resumes bus activity simply by restarting sending frames, the USBD peripheral will generate SOF events. Also here the device has to be responsive to any incoming request on the USB bus, and can be in normal power consumption mode.

### 51.7.3 Device-initiated remote wake-up

Assuming that remote wake-up is supported by the device and has been enabled by the host, if the device meets a wake-up condition while the device is suspended, the device can request the host to resume.

To do so, the software shall first make sure that HFXO gets enabled.

It can then instruct the USBD peripheral to drive a RESUME condition (K state) on the USB bus through the DPDMDRIVE task, and hence attempt to wake up the host. By choosing Resume in *DPDMVALUE*, the duration of the RESUME state is under hardware control ($T_{USB,DRIVEK}$). By choosing J or K, the duration of that state is under software control (the J or K state is maintained until a DPDMNODRIVE task is issued), and has to meet $T_{DRSMUP}$ from USB specification chapter 7.

The value in the *DPDMVALUE* on page 648 register will only be captured and used when the DPDMDRIVE task is sent.

Note that the device shall ensure that it does not initiate such a remote wake-up request before $T_{WTRSM}$ (as per USB specification chapter 7) after the bus has entered idle state. Using the recommended Resume value in *DPDMVALUE*, rather than K, takes care of this, and postpones the RESUME state accordingly.

As just explained, the *DPDMVALUE* register contains the value at which the bus shall be forced after a DPDMDRIVE task. If the software needs to read back the actual D+ and D- lines state, it can do so at any time by reading the *BUSSTATE* register.

## 51.8 EasyDMA

The USBD peripheral includes EasyDMA so that USB buffers are located in Data RAM .

Each endpoint has an associated set of tasks, events and registers.

The *EPIN[n].PTR*, *EPOUT[n].PTR* (n=0..7), *ISOIN.PTR* and *ISOOUT.PTR* registers define the address of the buffer in Data RAM for a specific IN or OUT endpoint.

The *EPIN[n].MAXCNT* and *ISOIN.MAXCNT* registers define the amount of bytes to be sent on USB for next transaction.

The *EPOUT[n].MAXCNT* (n=1..7) and *ISOOUT.MAXCNT* registers define the length of the buffer, in bytes, for next transfer of incoming data. Since the host decides how many bytes are being sent over USB, the MAXCNT value can be copied from the respective *SIZE.EPOUT[n]* (n=1..7) or *SIZE.ISOOUT* register.

The *EPOUT[0].MAXCNT* register defines the length of the control endpoint OUT buffer, in bytes. If the USB host does not misbehave, the *SIZE.EPOUT[0]* register will indicate the same value than MaxPacketSize from the device descriptor or wLength from the SETUP command, whichever is the smallest.

The *.AMOUNT* registers indicate how many bytes have actually been transferred over EasyDMA during last transfer.

The STARTEPIN[n], STARTEPOUT[n] (n=0..7), STARTISOIN and STARTISOOUT tasks capture the .PTR and .MAXCNT registers values; for IN endpoints, a transaction over USB gets automatically triggered when the EasyDMA transfer is complete; for OUT endpoints, it is up to software to allow the next transaction over USB, see the examples in *Control transfers* on page 617, *Bulk and interrupt transactions* on page 620 and *Isochronous transactions* on page 622.

The STARTED event confirms that the .PTR, .MAXCNT and .CONFIG registers values of the endpoints flagged in the *EPSTATUS* register have been captured; those can then be modified by software for the next transfer.

The ENDEPIN[n], ENDEPOUT[n] (n=0..7), ENDISOIN and ENDISOOUT events indicate that the whole buffer in Data RAM has been consumed. The buffer can be accessed safely by software.

Only a single EasyDMA transfer can take place in USBD at any time. It is up to the software to ensure that no STARTEPIN[n], STARTISOIN, STARTEPOUT[n] or STARTISOOUT task is sent before having received the ENDEPIN[n], ENDISOIN, ENDEPOUT[n] or ENDISOOUT event from an on-going transfer.

EasyDMA and traffic on USB are tightly related. A number of events provide insight of what is happening on the USB bus, and a number of tasks allow to somewhat automate response to traffic.

The EPDATA event indicates that a successful (acknowledged) data transaction has occurred on the data endpoint(s) flagged in the *EPDATASTATUS* register.

In the particular case of the control endpoint 0, OUT transactions are allowed through the EP0RCVOUT task. A successful (acknowledged) data transaction on endpoint 0 is signalled by the EP0DATADONE event. The EP0STATUS task allows a status stage to be initiated, and the EP0STALL task allows stalling further traffic (data or status stage) on the control endpoint.

The EP0SETUP event indicates that a SETUP token has been received on the control endpoint 0. EasyDMA will not copy the SETUP data to Data RAM (it will only transfer data from the data stage), they are available as separate registers in the USBD peripheral: *BMREQUESTTYPE*, *BREQUEST*, *WVALUEL*, *WVALUEH*, *WINDEXL*, *WINDEXH*, *WLENGTHL* and *WLENGTHH*.

At any time, the USBEVENT event may be sent, and the *EVENTCAUSE* register provides details on what happened, for instance if a CRC error is detected during a transaction, or if bus activity stops or resumes.

Enabling endpoints is controlled through the *EPINEN* and *EPOUTEN* registers.

Stalling bulk/interrupt endpoints is controlled through the *EPSTALL* register.

Note that due to USB specification requirements, the effect of the stalling control endpoint 0 may be overridden by hardware, in particular when a new SETUP token is received.

## 51.9 Control transfers

The USB specification mandates every USB device to implement endpoint 0 IN and OUT as control endpoints.

A control transfer consists of two or three stages:

- Setup stage
- Data stage (optional)
- Status stage

Each control transfer can be of following type:

- Control read
- Control read no data
- Control write
- Control write no data

An EP0SETUP event indicates that the data in the setup stage (i.e. following the SETUP token) is available in the *BREQUEST*, *BMREQUESTTYPE*, *WVALUEL*, *WVALUEH*, *WINDEXL*, *WINDEXH*, *WLENGTHL* and *WLENGTHH* registers.

The data in the data stage( i.e. following the IN or OUT token) is transferred from or to the desired location in Data RAM using EasyDMA.

Note: the control endpoint buffer size in Data RAM can be of any size in bytes, and there is no constraint to keep it 32-bit aligned.

After receiving the SETUP token, the USB controller will NAK any incoming IN or OUT token until software has finished decoding the command, determined the type of transfer, and prepared the next stage (data or status) appropriately.

The software can choose to STALL the command (both data and status stages) through the EP0STALL task, for instance if the command is not supported, or its wValue, wIndex or wLength parameters are wrong. A stalled Control Read transfer is depicted below, but the same mechanism (same tasks) applies to stalling a Control Write transfer (not depicted).

Refer to the chapter 9 of the USB Specification v2.0 and relevant Class specifications for rules on when to STALL a command.

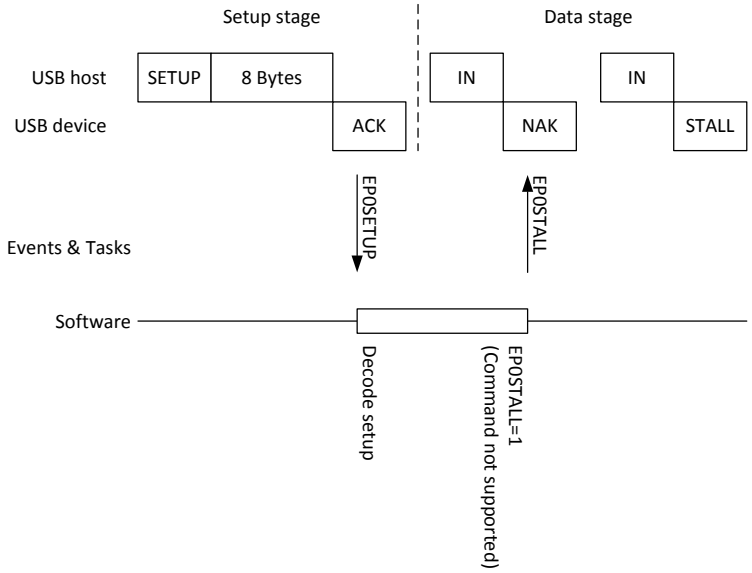



**Figure 178: Control read gets STALLed**

Important: the USBD peripheral handles the SetAddress transfer by itself. As a consequence, the software shall not process this command, other than updating its state machine (see *Device state diagram*), nor initiate a status stage. If necessary, the address assigned by the host can be read out from the USBADDR register after the command has been processed.

### 51.9.1 Control Read transfer

This section describes how the software behaves to respond to a Control Read transfer.

As mentioned earlier, the USB controller will NAK any incoming IN token until software has finished decoding the command, determined the type of transfer, and prepared the next stage (data or status) appropriately.

For a control-read, transferring the data from Data RAM memory into USBD will trigger a valid, ACKed IN transaction on USB.

The software has to prepare EasyDMA by pointing to the buffer containing the data to be transferred. If no other EasyDMA transfer is on-going with USBD, software can send the STARTEPIN0 task, which will initiate the data transfer and transaction on USB.

A STARTED event (with EPIN0 bit set in the *EPSTATUS* register) will get fired as soon as the EPIN[0].PTR and .MAXCNT registers have been captured. Software may then prepare them for next data transaction.

A ENDEPIN[0] event will get fired when the data has been transferred from memory to the USBD peripheral.

Finally, an EP0DATADONE event will get fired when the data has been transmitted over USB and acknowledged by the host.

The software can then either prepare and transmit the next data transaction by repeating the above sequence, or initiate the status stage through the EP0STATUS task.

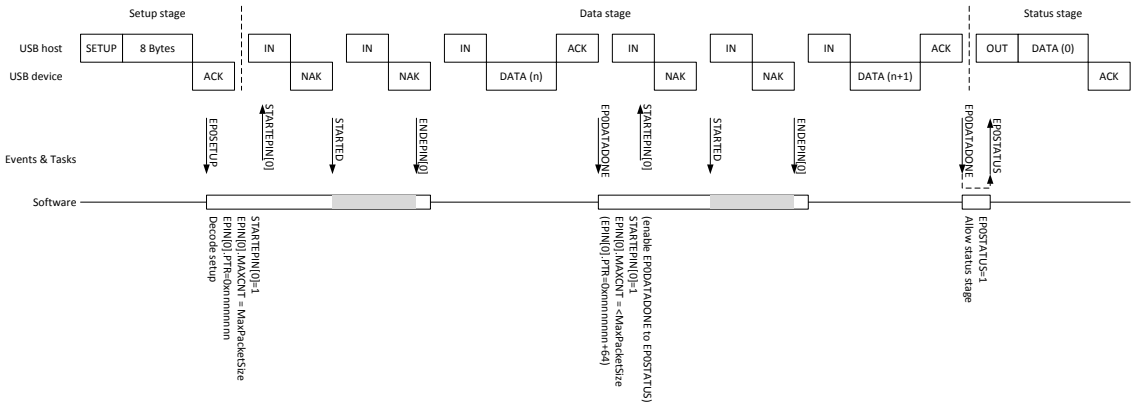



**Figure 179: Control read transfer**

Note the possibility to enable a shortcut from the EP0DATADONE event to the EP0STATUS task, typically if the data stage is expected to take a single transfer.

If there is no data stage, the software can initiate the status stage through the EP0STATUS task right away, as depicted below.

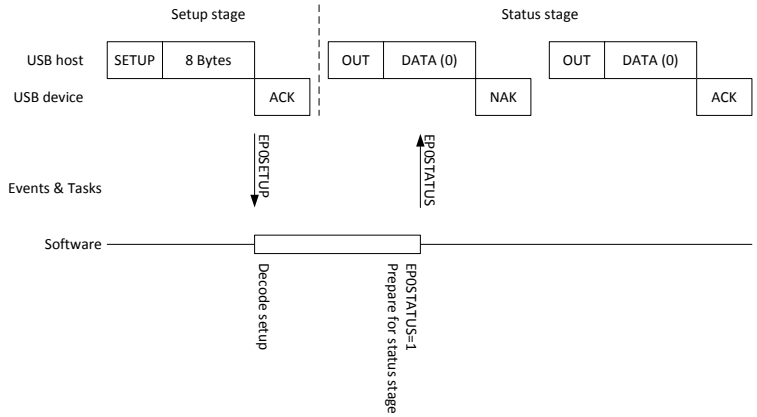



**Figure 180: Control read no data transfer**

## 51.9.2 Control Write transfer

This section describes how the software behaves to respond to a Control Write transfer.

The software has to prepare EasyDMA by pointing to the buffer in Data RAM that shall contain the incoming data. If no other EasyDMA transfer is on-going with USBD, software can then send the EP0RCVOUT task, which will make the USBD to accept (ACK) the first OUT+DATA transaction from the host.

An EP0DATADONE event will get fired when a new OUT+DATA has been transmitted over USB, and is about to get acknowledged by the device.

A STARTED event (with EPOUT0 bit set in the *EPSTATUS* register) will get fired as soon as the EPOUT[0].PTR and .MAXCNT registers have been captured, after receiving the first transaction. Software may then prepare them for next data transaction.

A ENDEPOUT[0] event will get fired when the data has been transferred from the USBD peripheral to Data RAM.

The software can then either prepare to receive the next data transaction by repeating the above sequence, or initiate the status stage through the EP0STATUS task. Until then, further incoming OUT + DATA transactions get a NAK response by the device.

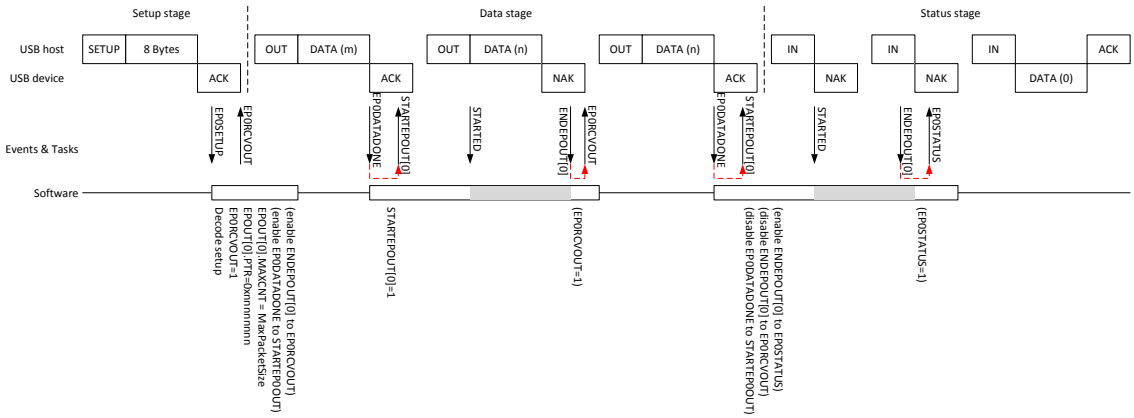



**Figure 181: Control write transfer**

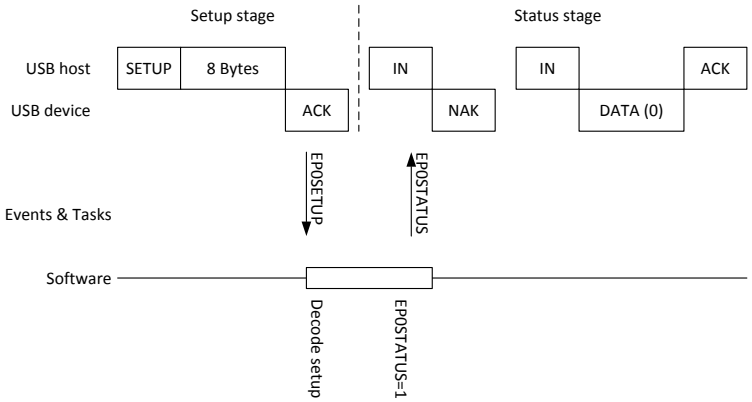



**Figure 182: Control write no data transfer**

## 51.10 Bulk and interrupt transactions

The USBD peripheral implements seven pairs of bulk/interrupt endpoints.

The bulk/interrupt endpoints have a fixed USB endpoint number, summarized in the table below.

**Table 124: Bulk/interrupt endpoint numbering**

| Bulk endpoint # | USB IN endpoint | USB OUT endpoint |
|---|---|---|
| [1] | 0x81 | 0x01 |
| [2] | 0x82 | 0x02 |
| [3] | 0x83 | 0x03 |
| [4] | 0x84 | 0x04 |
| [5] | 0x85 | 0x05 |
| [6] | 0x86 | 0x06 |
| [7] | 0x87 | 0x07 |

A bulk/interrupt transaction consists of a single data stage. Two consecutive, successful transactions are distinguished through alternating leading PID: DATA0 follows DATA1, DATA1 follows DATA0, etc.

A repeated transaction is detected by re-using the same PID as previous transaction, i.e DATA0 follows DATA0, or DATA1 follows DATA1.

The USBD controller automatically toggles DATA0/DATA1 PIDs for every bulk/interrupt transaction, and in general software does not need to care about it.

If an incoming data is corrupted (CRC does not match), the USBD controller automatically prevents DATA0/DATA1 from toggling, to request the host to resend the data.

In specific cases, the software may want to force data toggle (usually reset) on a specific IN endpoint, or force the expected toggle on an OUT endpoint, for instance as a consequence of the host issuing a

ClearFeature, SetInterface or selecting an alternate setting. Controlling the data toggle of data IN or OUT endpoint n=1..7 is done through the *DTOGGLE* register.

The maximum size of a bulk/interrupt transaction in USB Full Speed is 64 Bytes, and has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of DATA bytes transmitted on the USB data endpoint can be of any size (up to 64 bytes).

When the transaction is done over USB, a EPDATA event is sent, and the hardware will automatically NAK further IN tokens, until software is ready to send more data and has finished configuring EasyDMA, has started it, and the whole buffer content has been moved to the USB controller (signalled by the ENDEPIN[n] event).

Each IN or OUT data endpoint has to be explicitly enabled by software through the *EPINEN* or *EPOUTEN* register, according to the configuration declared by the device and selected by the host through the SetConfig command.

A disabled data endpoint will not respond to any traffic from the host.

An enabled data endpoint will normally respond NAK or ACK (depending on the readiness of the buffers), or STALL if configured so through the *EPSTALL* register (in which case the endpoint is said to be halted).

The halted (or not) state of a given endpoint can be read back from the *HALTED.EPIN[n]* or *HALTED.EPOUT[n]* register. The format of the returned 16 bit value can be copied as is as response to a GetStatusEndpoint request from the host.

Note that enabling or disabling an endpoint will not change its halted state. However, a USB reset will disable and clear the halted state of all data endpoints.

The control endpoint 0 IN and OUT can also get enabled and/or halted through the same mechanisms, but due to USB specification, receiving a SETUP will override its state.

### 51.10.1 Bulk and interrupt IN transaction

The host issues IN tokens to receive bulk/interrupt data. In order to send data, the software has to enable the endpoint and prepare an EasyDMA transfer on the desired endpoint, as illustrated below.

Bulk/interrupt IN endpoints are enabled or disabled through their respective INn bit (n=1..7) in *EPINEN* register.

It is also possible to stall or un-stall an endpoint through the *EPSTALL* register.

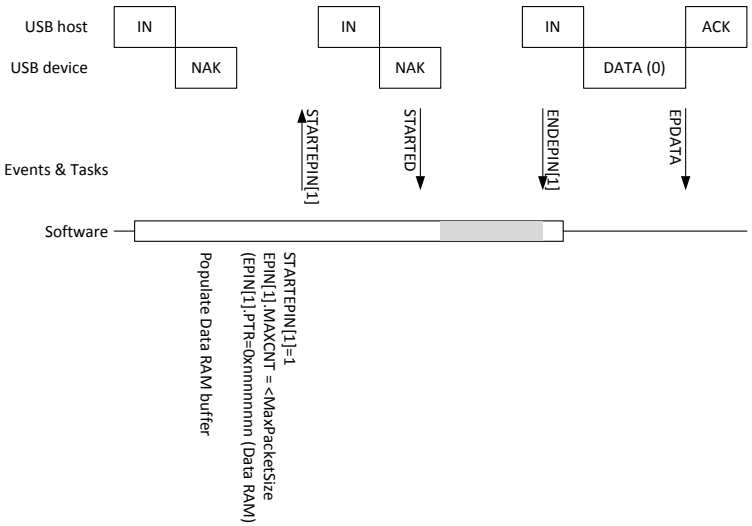



**Figure 183: Bulk/interrupt IN transaction**

It is possible (and some situations mandate it) to respond to an IN with a zero-length data packet.

Note: on many USB hosts, not responding (DATA+ACK or NAK) to three IN tokens on a interrupt endpoint would have the host disable that endpoint as a consequence. Re-enumerating the device (unplug-replug)

may be required to restore functionality. Make sure the relevant data endpoints are enabled for normal operation as soon as the device gets configured through a SetConfig request.

### 51.10.2 Bulk and interrupt OUT transaction

When the host wants to transmit bulk/interrupt data, it issues an OUT Token packet followed by a DATA packet on a given endpoint n.

A NAK handshake is returned until the software writes any value to *SIZE.EPOUT[n]*, indicating that the local buffer's content can be overwritten. Upon receiving the next OUT + DATA transaction, an ACK handshake is returned to the host while a EPDATA event is sent (and *EPSTATUS* register flags set to indicate on which endpoint this happened), and once the EasyDMA is prepared and enabled through writing the *EPOUT[n]* registers and sending the STARTEPOUT[n] task, the incoming data will be transferred to Data RAM. Until that transfer is finished, the hardware will automatically NAK further incoming OUT+DATA packets. Only when the EasyDMA transfer is done (signalled by the ENDEPOUT[n] event) and the software has written any value to *SIZE.EPOUT[n]*, the endpoint n will accept incoming OUT + DATA again.

It is allowed for the host to send out a zero-length data packet.

Bulk/interrupt OUT endpoints are enabled or disabled through their respective OUTn bit (n=1..7) in the *EPOUTEN* register. It is also possible to stall or un-stall an endpoint through the *EPSTALL* register.

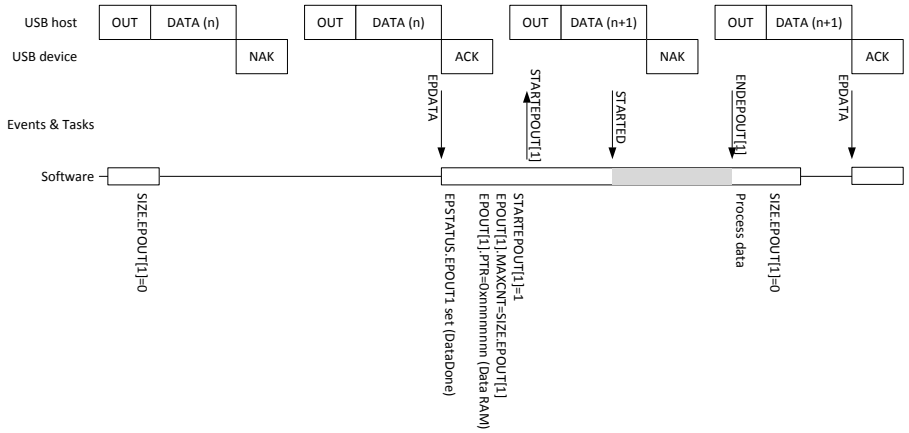



**Figure 184: Bulk/interrupt OUT transaction**

## 51.11 Isochronous transactions

The USBD peripheral implements isochronous (iso) endpoints.

The iso endpoints have a fixed USB endpoint number, summarized in the table below.

**Table 125: Isochronous endpoint numbering**

| Iso endpoint # | USB IN endpoint | USB OUT endpoint |
|---|---|---|
| [0] | 0x88 | 0x08 |

A isochronous transaction consists of a single, non-acknowledged data stage. The host sends out a start of frame at a regular interval (1ms), and data follows IN or OUT tokens within each frame.

EasyDMA allows transferring iso data directly from and to Data RAM; EasyDMA transfers must be initiated by software, which can synchronize to the SOF events.

Because the timing of the start of frame is very accurate, the SOF event can be used for instance to synchronize a local timer through the SOF event and PPI. The SOF event gets synchronized to the 16 MHz clock prior to being made available to PPI.

Every Start of Frame increments a free-running counter, which can be read by software through the *FRAMECNTR* register.

Each IN or OUT iso data endpoint has to be explicitly enabled by software through the *EPINEN* or *EPOUTEN* register, according to the configuration declared by the device and selected by the host through the SetConfig command.

A disabled iso IN data endpoint will not respond to any traffic from the host.

A disabled iso OUT data endpoint will ignore any incoming traffic from the host.

The USBD peripheral has an internal 1 kByte buffer associated with iso endpoints. The user can either allocate the full amount to the IN or the OUT endpoint, or split the buffer allocation between the two. This is done through the *ISOSPLIT* register, which provides a number of pre-determined splits.

### 51.11.1 Isochronous IN transaction

When the host wants to receive isochronous (iso) data, it issues an IN token on the isochronous endpoint.

On the isochronous IN endpoint, after the data has been transferred using the EasyDMA, the USB controller responds to the IN token with the data that had been transferred, using the *ISOIN.MAXCNT* for the size of the packet.

The iso IN data endpoint has to be explicitly enabled by software through the ISOIN0 bit in the *EPINEN* register.

When the iso IN endpoint is enabled, and if no data had been transferred with EasyDMA, the response of the USBD depends on the setting of the RESPONSE field in the *ISOINCONFIG* register. If set to NoResp, no response to an IN token will be provided. If set to ZeroData, the USBD responds with a zero-length data.

Note: the maximum size of an isochronous IN transfer in USB Full Speed is 1023 Bytes, and the data buffer in RAM has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 Byte if not shared with an OUT iso endpoint).

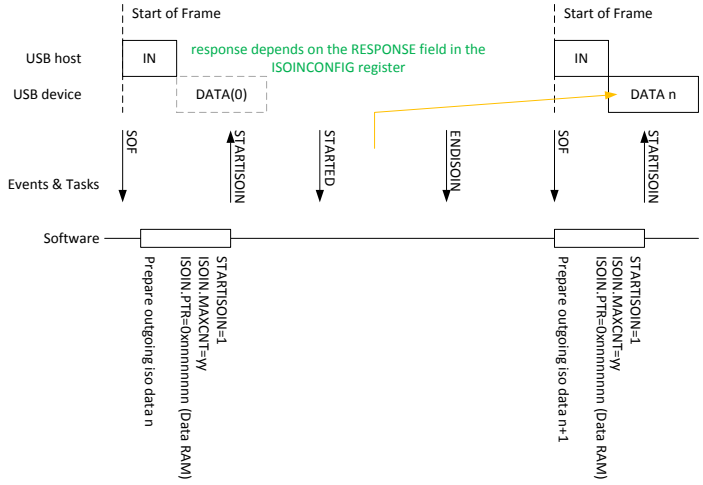



**Figure 185: Isochronous IN transfer**

### 51.11.2 Isochronous OUT transaction

When the host wants to send isochronous (iso) data, it issues an OUT token on the isochronous endpoint, followed by data.

The iso OUT data endpoint has to be explicitly enabled by software through the ISOOUT0 bit in the *EPOUTEN* register.

The amount of last received iso OUT data is provided in the *SIZE.ISOOUT* register.

Software shall interpret the ZERO and SIZE fields as follows:

**Table 126: Iso OUT incoming data size**

| ZERO | SIZE | last received data size |
|---|---|---|
| Normal | 0 | No data received at all |

| ZERO | SIZE | last received data size |
|---|---|---|
| Normal | 1..1023 | 1..1023 bytes of data received |
| ZeroData | (don't care) | Zero-length data packet received |

When the EasyDMA is prepared and started, sending a STARTISOOUT task initiates an EasyDMA transfer to Data RAM. Software shall synchronize iso OUT transfers to the SOF events. If OUT data is not consumed and processed until next SOF, it will be overwritten by more recent data.

EasyDMA uses the address in *ISOOUT.PTR* and size in *ISOOUT.MAXCNT* for every new transfer.

Note: the maximum size of an isochronous OUT transfer in USB Full Speed is 1023 Bytes, and the data buffer in RAM has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 Byte if not shared with an IN iso endpoint).

If the last received iso data packet is corrupted (wrong CRC), the USB controller sends an USBEVENT event (at the same time as SOF) and indicates a CRC error on ISOOUTCRC in the *EVENTCAUSE* register. EasyDMA will transfer the data anyway if it has been set up properly.

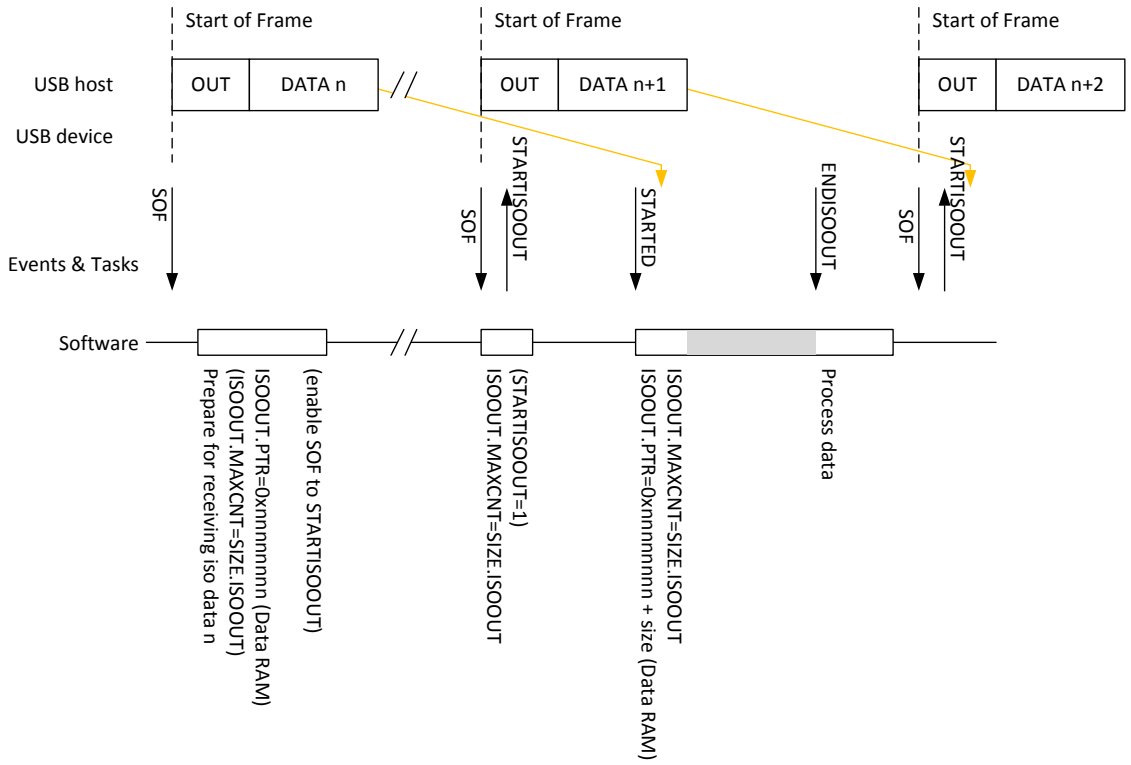



**Figure 186: Isochronous OUT transfer**

## 51.12 USB register access limitations

Some of the registers in USBD cannot get accessed in specific conditions.

This is the case while USBD is not enabled (through the *ENABLE* register) and ready (signalled by the READY bit in *EVENTCAUSE* after the USBEVENT event), or when USBD has been placed in low power while the USB bus is suspended.

If any of the register listed below gets accessed (read or write) by software of through the debugger, an ACCESSFAULT event will get fired, and if the associated interrupt has been enabled through the *INTEN* or *INTENSET* register in USBD, an interrupt will be taken.

Following registers are affected by this behaviour:

- firing any task, including through PPI
- BUSSTATE

- HALTED.EPIN[0..7]
- HALTED.EPOUT[0..7]
- USBADDR
- BMREQUESTTYPE
- BREQUEST
- WVALUEL
- WVALUEH
- WINDEXL
- WINDEXH
- WLENGTHL
- WLENGTHH
- SIZE.EPOUT[0..7]
- SIZE.ISOOUT
- USBPULLUP
- DTOGGLE
- EPINEN
- EPOUTEN
- EPSTALL
- ISOSPLIT
- FRAMECNTR

## 51.13 Registers

### Table 127: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40027000 | USBD | USBD | Universal serial bus device | |

### Table 128: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTEPIN[0] | 0x004 | Captures the EPIN[0].PTR, EPIN[0].MAXCNT and EPIN[0].CONFIG registers values, and enables endpoint IN 0 to respond to traffic from host |
| TASKS_STARTEPIN[1] | 0x008 | Captures the EPIN[1].PTR, EPIN[1].MAXCNT and EPIN[1].CONFIG registers values, and enables endpoint IN 1 to respond to traffic from host |
| TASKS_STARTEPIN[2] | 0x00C | Captures the EPIN[2].PTR, EPIN[2].MAXCNT and EPIN[2].CONFIG registers values, and enables endpoint IN 2 to respond to traffic from host |
| TASKS_STARTEPIN[3] | 0x010 | Captures the EPIN[3].PTR, EPIN[3].MAXCNT and EPIN[3].CONFIG registers values, and enables endpoint IN 3 to respond to traffic from host |
| TASKS_STARTEPIN[4] | 0x014 | Captures the EPIN[4].PTR, EPIN[4].MAXCNT and EPIN[4].CONFIG registers values, and enables endpoint IN 4 to respond to traffic from host |
| TASKS_STARTEPIN[5] | 0x018 | Captures the EPIN[5].PTR, EPIN[5].MAXCNT and EPIN[5].CONFIG registers values, and enables endpoint IN 5 to respond to traffic from host |
| TASKS_STARTEPIN[6] | 0x01C | Captures the EPIN[6].PTR, EPIN[6].MAXCNT and EPIN[6].CONFIG registers values, and enables endpoint IN 6 to respond to traffic from host |
| TASKS_STARTEPIN[7] | 0x020 | Captures the EPIN[7].PTR, EPIN[7].MAXCNT and EPIN[7].CONFIG registers values, and enables endpoint IN 7 to respond to traffic from host |
| TASKS_STARTISOIN | 0x024 | Captures the ISOIN.PTR, ISOIN.MAXCNT and ISOIN.CONFIG registers values, and enables sending data on iso endpoint |
| TASKS_STARTEPOUT[0] | 0x028 | Captures the EPOUT[0].PTR, EPOUT[0].MAXCNT and EPOUT[0].CONFIG registers values, and enables endpoint 0 to respond to traffic from host |
| TASKS_STARTEPOUT[1] | 0x02C | Captures the EPOUT[1].PTR, EPOUT[1].MAXCNT and EPOUT[1].CONFIG registers values, and enables endpoint 1 to respond to traffic from host |
| TASKS_STARTEPOUT[2] | 0x030 | Captures the EPOUT[2].PTR, EPOUT[2].MAXCNT and EPOUT[2].CONFIG registers values, and enables endpoint 2 to respond to traffic from host |

| Register | Offset | Description |
|---|---|---|
| TASKS_STARTEPOUT[3] | 0x034 | Captures the EPOUT[3].PTR, EPOUT[3].MAXCNT and EPOUT[3].CONFIG registers values, and enables endpoint 3 to respond to traffic from host |
| TASKS_STARTEPOUT[4] | 0x038 | Captures the EPOUT[4].PTR, EPOUT[4].MAXCNT and EPOUT[4].CONFIG registers values, and enables endpoint 4 to respond to traffic from host |
| TASKS_STARTEPOUT[5] | 0x03C | Captures the EPOUT[5].PTR, EPOUT[5].MAXCNT and EPOUT[5].CONFIG registers values, and enables endpoint 5 to respond to traffic from host |
| TASKS_STARTEPOUT[6] | 0x040 | Captures the EPOUT[6].PTR, EPOUT[6].MAXCNT and EPOUT[6].CONFIG registers values, and enables endpoint 6 to respond to traffic from host |
| TASKS_STARTEPOUT[7] | 0x044 | Captures the EPOUT[7].PTR, EPOUT[7].MAXCNT and EPOUT[7].CONFIG registers values, and enables endpoint 7 to respond to traffic from host |
| TASKS_STARTISOOUT | 0x048 | Captures the ISOOUT.PTR, ISOOUT.MAXCNT and ISOOUT.CONFIG registers values, and enables receiving of data on iso endpoint |
| TASKS_EP0RCVOUT | 0x04C | Allows OUT data stage on control endpoint 0 |
| TASKS_EP0STATUS | 0x050 | Allows status stage on control endpoint 0 |
| TASKS_EP0STALL | 0x054 | STALLs data and status stage on control endpoint 0 |
| TASKS_DPDMDRIVE | 0x058 | Forces D+ and D-lines to the state defined in the DPDMVALUE register |
| TASKS_DPDMNODRIVE | 0x05C | Stops forcing D+ and D- lines to any state (USB engine takes control) |
| EVENTS_USBRESET | 0x100 | Signals that a USB reset condition has been detected on the USB lines |
| EVENTS_STARTED | 0x104 | Confirms that the EPIN[n].PTR, EPIN[n].MAXCNT, EPIN[n].CONFIG, or EPOUT[n].PTR, EPOUT[n].MAXCNT and EPOUT[n].CONFIG registers have been captured on all endpoints reported in the EPSTATUS register |
| EVENTS_ENDEPIN[0] | 0x108 | The whole EPIN[0] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[1] | 0x10C | The whole EPIN[1] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[2] | 0x110 | The whole EPIN[2] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[3] | 0x114 | The whole EPIN[3] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[4] | 0x118 | The whole EPIN[4] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[5] | 0x11C | The whole EPIN[5] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[6] | 0x120 | The whole EPIN[6] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPIN[7] | 0x124 | The whole EPIN[7] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_EP0DATADONE | 0x128 | An acknowledged data transfer has taken place on the control endpoint |
| EVENTS_ENDISOIN | 0x12C | The whole ISOIN buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[0] | 0x130 | The whole EPOUT[0] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[1] | 0x134 | The whole EPOUT[1] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[2] | 0x138 | The whole EPOUT[2] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[3] | 0x13C | The whole EPOUT[3] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[4] | 0x140 | The whole EPOUT[4] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[5] | 0x144 | The whole EPOUT[5] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[6] | 0x148 | The whole EPOUT[6] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDEPOUT[7] | 0x14C | The whole EPOUT[7] buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_ENDISOOUT | 0x150 | The whole ISOOUT buffer has been consumed. The RAM buffer can be accessed safely by software. |
| EVENTS_SOF | 0x154 | Signals that a SOF (start of frame) condition has been detected on the USB lines |
| EVENTS_USBEVENT | 0x158 | An event or an error not covered by specific events has occurred, check EVENTCAUSE register to find the cause |
| EVENTS_EP0SETUP | 0x15C | A valid SETUP token has been received (and acknowledged) on the control endpoint |
| EVENTS_EPDATA | 0x160 | A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register |
| EVENTS_ACCESSFAULT | 0x164 | Access to an unavailable USB register has been attempted (software or EasyDMA). This event can get fired even when USBD is not ENABLEd. |
| *SHORTS* | 0x200 | Shortcut register |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |

| Register | Offset | Description |
|---|---|---|
| INTENCLR | 0x308 | Disable interrupt |
| EVENTCAUSE | 0x400 | Details on event that caused the USBEVENT event |
| BUSSTATE | 0x404 | Provides the logic state of the D+ and D- lines |
| HALTED.EPIN[0] | 0x420 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[1] | 0x424 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[2] | 0x428 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[3] | 0x42C | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[4] | 0x430 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[5] | 0x434 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[6] | 0x438 | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPIN[7] | 0x43C | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[0] | 0x444 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[1] | 0x448 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[2] | 0x44C | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[3] | 0x450 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[4] | 0x454 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[5] | 0x458 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[6] | 0x45C | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| HALTED.EPOUT[7] | 0x460 | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| EPSTATUS | 0x468 | Provides information on which endpoint's EasyDMA registers have been captured |
| EPDATASTATUS | 0x46C | Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event) |
| USBADDR | 0x470 | Device USB address |
| BMREQUESTTYPE | 0x480 | SETUP data, byte 0, bmRequestType |
| BREQUEST | 0x484 | SETUP data, byte 1, bRequest |
| WVALUEL | 0x488 | SETUP data, byte 2, LSB of wValue |
| WVALUEH | 0x48C | SETUP data, byte 3, MSB of wValue |
| WINDEXL | 0x490 | SETUP data, byte 4, LSB of wIndex |
| WINDEXH | 0x494 | SETUP data, byte 5, MSB of wIndex |
| WLENGTHL | 0x498 | SETUP data, byte 6, LSB of wLength |
| WLENGTHH | 0x49C | SETUP data, byte 7, MSB of wLength |
| SIZE.EPOUT[0] | 0x4A0 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[1] | 0x4A4 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[2] | 0x4A8 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[3] | 0x4AC | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[4] | 0x4B0 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[5] | 0x4B4 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[6] | 0x4B8 | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.EPOUT[7] | 0x4BC | Amount of bytes received last in the data stage of this OUT endpoint |
| SIZE.ISOOUT | 0x4C0 | Amount of bytes received last on this iso OUT data endpoint |
| ENABLE | 0x500 | Enable USB |
| USBPULLUP | 0x504 | Control of the USB pull-up |
| DPDMVALUE | 0x508 | State at which the DPDMDRIVE task will force D+ and D-. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing). |
| DTOGGLE | 0x50C | Data toggle control and status. |
| EPINEN | 0x510 | Endpoint IN enable |
| EPOUTEN | 0x514 | Endpoint OUT enable |
| EPSTALL | 0x518 | STALL endpoints |
| ISOSPLIT | 0x51C | Controls the split of ISO buffers |
| FRAMECNTR | 0x520 | Returns the current value of the start of frame counter |
| LOWPOWER | 0x52C | Controls USBD peripheral low-power mode during USB suspend |
| ISOINCONFIG | 0x530 | Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent |
| EPIN[0].PTR | 0x600 | Data pointer |
| EPIN[0].MAXCNT | 0x604 | Maximum number of bytes to transfer |
| EPIN[0].AMOUNT | 0x608 | Number of bytes transferred in the last transaction |
| EPIN[1].PTR | 0x614 | Data pointer |
| EPIN[1].MAXCNT | 0x618 | Maximum number of bytes to transfer |
| EPIN[1].AMOUNT | 0x61C | Number of bytes transferred in the last transaction |

| Register | Offset | Description |
|---|---|---|
| EPIN[2].PTR | 0x628 | Data pointer |
| EPIN[2].MAXCNT | 0x62C | Maximum number of bytes to transfer |
| EPIN[2].AMOUNT | 0x630 | Number of bytes transferred in the last transaction |
| EPIN[3].PTR | 0x63C | Data pointer |
| EPIN[3].MAXCNT | 0x640 | Maximum number of bytes to transfer |
| EPIN[3].AMOUNT | 0x644 | Number of bytes transferred in the last transaction |
| EPIN[4].PTR | 0x650 | Data pointer |
| EPIN[4].MAXCNT | 0x654 | Maximum number of bytes to transfer |
| EPIN[4].AMOUNT | 0x658 | Number of bytes transferred in the last transaction |
| EPIN[5].PTR | 0x664 | Data pointer |
| EPIN[5].MAXCNT | 0x668 | Maximum number of bytes to transfer |
| EPIN[5].AMOUNT | 0x66C | Number of bytes transferred in the last transaction |
| EPIN[6].PTR | 0x678 | Data pointer |
| EPIN[6].MAXCNT | 0x67C | Maximum number of bytes to transfer |
| EPIN[6].AMOUNT | 0x680 | Number of bytes transferred in the last transaction |
| EPIN[7].PTR | 0x68C | Data pointer |
| EPIN[7].MAXCNT | 0x690 | Maximum number of bytes to transfer |
| EPIN[7].AMOUNT | 0x694 | Number of bytes transferred in the last transaction |
| ISOIN.PTR | 0x6A0 | Data pointer |
| ISOIN.MAXCNT | 0x6A4 | Maximum number of bytes to transfer |
| ISOIN.AMOUNT | 0x6A8 | Number of bytes transferred in the last transaction |
| EPOUT[0].PTR | 0x700 | Data pointer |
| EPOUT[0].MAXCNT | 0x704 | Maximum number of bytes to transfer |
| EPOUT[0].AMOUNT | 0x708 | Number of bytes transferred in the last transaction |
| EPOUT[1].PTR | 0x714 | Data pointer |
| EPOUT[1].MAXCNT | 0x718 | Maximum number of bytes to transfer |
| EPOUT[1].AMOUNT | 0x71C | Number of bytes transferred in the last transaction |
| EPOUT[2].PTR | 0x728 | Data pointer |
| EPOUT[2].MAXCNT | 0x72C | Maximum number of bytes to transfer |
| EPOUT[2].AMOUNT | 0x730 | Number of bytes transferred in the last transaction |
| EPOUT[3].PTR | 0x73C | Data pointer |
| EPOUT[3].MAXCNT | 0x740 | Maximum number of bytes to transfer |
| EPOUT[3].AMOUNT | 0x744 | Number of bytes transferred in the last transaction |
| EPOUT[4].PTR | 0x750 | Data pointer |
| EPOUT[4].MAXCNT | 0x754 | Maximum number of bytes to transfer |
| EPOUT[4].AMOUNT | 0x758 | Number of bytes transferred in the last transaction |
| EPOUT[5].PTR | 0x764 | Data pointer |
| EPOUT[5].MAXCNT | 0x768 | Maximum number of bytes to transfer |
| EPOUT[5].AMOUNT | 0x76C | Number of bytes transferred in the last transaction |
| EPOUT[6].PTR | 0x778 | Data pointer |
| EPOUT[6].MAXCNT | 0x77C | Maximum number of bytes to transfer |
| EPOUT[6].AMOUNT | 0x780 | Number of bytes transferred in the last transaction |
| EPOUT[7].PTR | 0x78C | Data pointer |
| EPOUT[7].MAXCNT | 0x790 | Maximum number of bytes to transfer |
| EPOUT[7].AMOUNT | 0x794 | Number of bytes transferred in the last transaction |
| ISOOUT.PTR | 0x7A0 | Data pointer |
| ISOOUT.MAXCNT | 0x7A4 | Maximum number of bytes to transfer |
| ISOOUT.AMOUNT | 0x7A8 | Number of bytes transferred in the last transaction |

### 51.13.1 SHORTS

Address offset: 0x200

Shortcut register

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | EP0DATADONE_STARTEPI | | | Shortcut between EP0DATADONE event and STARTEPIN[0] task<br>See *EVENTS_EP0DATADONE* and *TASKS_STARTEPIN[0]* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| B | RW | EP0DATADONE_STARTEPO | | | Shortcut between EP0DATADONE event and STARTEPOUT[0] task<br>See *EVENTS_EP0DATADONE* and *TASKS_STARTEPOUT[0]* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| C | RW | EP0DATADONE_EP0STATU | | | Shortcut between EP0DATADONE event and EP0STATUS task<br>See *EVENTS_EP0DATADONE* and *TASKS_EP0STATUS* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| D | RW | ENDEPOUT0_EP0STATUS | | | Shortcut between ENDEPOUT[0] event and EP0STATUS task<br>See *EVENTS_ENDEPOUT[0]* and *TASKS_EP0STATUS* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |
| E | RW | ENDEPOUT0_EP0RCVOUT | | | Shortcut between ENDEPOUT[0] event and EP0RCVOUT task<br>See *EVENTS_ENDEPOUT[0]* and *TASKS_EP0RCVOUT* |
| | | | Disabled | 0 | Disable shortcut |
| | | | Enabled | 1 | Enable shortcut |

## 51.13.2 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | Z Y X W V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | RW | USBRESET | | | Enable or disable interrupt for USBRESET event<br>See *EVENTS_USBRESET* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| B | RW | STARTED | | | Enable or disable interrupt for STARTED event<br>See *EVENTS_STARTED* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| C | RW | ENDEPIN0 | | | Enable or disable interrupt for ENDEPIN[0] event<br>See *EVENTS_ENDEPIN[0]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| D | RW | ENDEPIN1 | | | Enable or disable interrupt for ENDEPIN[1] event<br>See *EVENTS_ENDEPIN[1]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| E | RW | ENDEPIN2 | | | Enable or disable interrupt for ENDEPIN[2] event<br>See *EVENTS_ENDEPIN[2]* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | ENDEPIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | ENDEPIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ENDEPIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | ENDEPIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | ENDEPIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | EP0DATADONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | ENDISOIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | ENDEPOUT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | ENDEPOUT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | ENDEPOUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | ENDEPOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | ENDEPOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | ENDEPOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | ENDEPOUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | ENDEPOUT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | ENDISOOUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | USBEVENT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | EP0SETUP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | EPDATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | ACCESSFAULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.3 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | USBRESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ENDEPIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[0]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ENDEPIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[1]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ENDEPIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[2]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | ENDEPIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[3]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | ENDEPIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[4]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | ENDEPIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[5]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | ENDEPIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[6]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | ENDEPIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[7]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | EP0DATADONE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EP0DATADONE* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | ENDISOIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDISOIN* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | ENDEPOUT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[0]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | ENDEPOUT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[1]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | ENDEPOUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[2]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | ENDEPOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[3]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | ENDEPOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[4]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | ENDEPOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[5]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | ENDEPOUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[6]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | ENDEPOUT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[7]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | ENDISOOUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDISOOUT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_SOF* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | USBEVENT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_USBEVENT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | EP0SETUP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EP0SETUP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | EPDATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EPDATA* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | ACCESSFAULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ACCESSFAULT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.4 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
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| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | USBRESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_USBRESET* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_STARTED* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ENDEPIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[0]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | ENDEPIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPIN[1]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | ENDEPIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
|---|---|---|---|---|---|
| | | | | | See *EVENTS_ENDEPIN[2]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| F | RW | ENDEPIN3 | | | Write '1' to Disable interrupt for ENDEPIN[3] event<br><br>See *EVENTS_ENDEPIN[3]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| G | RW | ENDEPIN4 | | | Write '1' to Disable interrupt for ENDEPIN[4] event<br><br>See *EVENTS_ENDEPIN[4]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| H | RW | ENDEPIN5 | | | Write '1' to Disable interrupt for ENDEPIN[5] event<br><br>See *EVENTS_ENDEPIN[5]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| I | RW | ENDEPIN6 | | | Write '1' to Disable interrupt for ENDEPIN[6] event<br><br>See *EVENTS_ENDEPIN[6]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| J | RW | ENDEPIN7 | | | Write '1' to Disable interrupt for ENDEPIN[7] event<br><br>See *EVENTS_ENDEPIN[7]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| K | RW | EP0DATADONE | | | Write '1' to Disable interrupt for EP0DATADONE event<br><br>See *EVENTS_EP0DATADONE* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| L | RW | ENDISOIN | | | Write '1' to Disable interrupt for ENDISOIN event<br><br>See *EVENTS_ENDISOIN* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| M | RW | ENDEPOUT0 | | | Write '1' to Disable interrupt for ENDEPOUT[0] event<br><br>See *EVENTS_ENDEPOUT[0]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| N | RW | ENDEPOUT1 | | | Write '1' to Disable interrupt for ENDEPOUT[1] event<br><br>See *EVENTS_ENDEPOUT[1]* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| O | RW | ENDEPOUT2 | | | Write '1' to Disable interrupt for ENDEPOUT[2] event<br><br>See *EVENTS_ENDEPOUT[2]* |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | ENDEPOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[3]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | ENDEPOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[4]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | ENDEPOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[5]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| S | RW | ENDEPOUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[6]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | RW | ENDEPOUT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDEPOUT[7]* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | RW | ENDISOOUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ENDISOOUT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | RW | SOF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_SOF* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | RW | USBEVENT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_USBEVENT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | RW | EP0SETUP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EP0SETUP* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | RW | EPDATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_EPDATA* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | RW | ACCESSFAULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | See *EVENTS_ACCESSFAULT* | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.5 EVENTCAUSE

Address offset: 0x400

Details on event that caused the USBEVENT event

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | E | | C | B | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ISOOUTCRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | SUSPEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | RESUME | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Detected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | READY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDetected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Ready | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.6 BUSSTATE

Address offset: 0x404

Provides the logic state of the D+ and D- lines

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | DM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | DP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.7 HALTED.EPIN[0]

Address offset: 0x420

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.8 HALTED.EPIN[1]

Address offset: 0x424

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.9 HALTED.EPIN[2]

Address offset: 0x428

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.10 HALTED.EPIN[3]

Address offset: 0x42C

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.11 HALTED.EPIN[4]

Address offset: 0x430

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.12 HALTED.EPIN[5]

Address offset: 0x434

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.13 HALTED.EPIN[6]

Address offset: 0x438

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.14 HALTED.EPIN[7]

Address offset: 0x43C

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.15 HALTED.EPOUT[0]

Address offset: 0x444

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.16 HALTED.EPOUT[1]

Address offset: 0x448

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.17 HALTED.EPOUT[2]

Address offset: 0x44C

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.18 HALTED.EPOUT[3]

Address offset: 0x450

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | **Description** | | | | | | | | | | | | | | | |
| A | R | GETSTATUS | | | | | | | | | | | | | | | | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. | | | | | | | | | | | | | | | |
| | | | NotHalted | 0 | | | | | | | | | | | | | | | | Endpoint is not halted | | | | | | | | | | | | | | | |
| | | | Halted | 1 | | | | | | | | | | | | | | | | Endpoint is halted | | | | | | | | | | | | | | | |

## 51.13.19 HALTED.EPOUT[4]

Address offset: 0x454

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.20 HALTED.EPOUT[5]

Address offset: 0x458

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.21 HALTED.EPOUT[6]

Address offset: 0x45C

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.22 HALTED.EPOUT[7]

Address offset: 0x460

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | GETSTATUS | | | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |
| | | | NotHalted | 0 | Endpoint is not halted |
| | | | Halted | 1 | Endpoint is halted |

## 51.13.23 EPSTATUS

Address offset: 0x468

Provides information on which endpoint's EasyDMA registers have been captured

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | R | Q | P | O | N | M | L | K | J | | | | | | | | | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EPIN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | EPIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | EPIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | EPIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | EPIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | EPIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | EPIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | EPIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | EPIN8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | EPOUT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | EPOUT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | EPOUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | EPOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | EPOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O | RW | EPOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | RW | EPOUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | RW | EPOUT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | RW | EPOUT8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoData | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.24 EPDATASTATUS

Address offset: 0x46C

Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | N | M | L | K | J | I | H | | | | | | | | | | G | F | E | D | C | B | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EPIN1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | EPIN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | EPIN3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | EPIN4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | EPIN5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | EPIN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | EPIN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotDone | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DataDone | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | EPOUT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | EPOUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RW | EPOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | RW | EPOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | RW | EPOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | RW | EPOUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | N | M | L | K | J | I | H | | | | | | | | | | G | F | E | D | C | B | A | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | No acknowledged data transfer on this endpoint | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | Acknowledged data transfer on this endpoint has occurred | | | | | | | | | | | | | | | | | | | | | | | |
| N | RW | EPOUT7 | | | | | | | | | | Acknowledged data transfer on this OUT endpoint. Write '1' to clear. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NotStarted | 0 | | | | | | | | No acknowledged data transfer on this endpoint | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Started | 1 | | | | | | | | Acknowledged data transfer on this endpoint has occurred | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.25 USBADDR

Address offset: 0x470

Device USB address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | ADDR | | | | | | | | | | Device USB address | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.26 BMREQUESTTYPE

Address offset: 0x480

SETUP data, byte 0, bmRequestType

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | B | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | RECIPIENT | | | | | | | | | | Data transfer type | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Device | 0 | | | | | | | | Device | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Interface | 1 | | | | | | | | Interface | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Endpoint | 2 | | | | | | | | Endpoint | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Other | 3 | | | | | | | | Other | | | | | | | | | | | | | | | | | | | | | | | |
| B | R | TYPE | | | | | | | | | | Data transfer type | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Standard | 0 | | | | | | | | Standard | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Class | 1 | | | | | | | | Class | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Vendor | 2 | | | | | | | | Vendor | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | DIRECTION | | | | | | | | | | Data transfer direction | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HostToDevice | 0 | | | | | | | | Host-to-device | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DeviceToHost | 1 | | | | | | | | Device-to-host | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.27 BREQUEST

Address offset: 0x484

SETUP data, byte 1, bRequest

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | BREQUEST | | | | | | | | | | SETUP data, byte 1, bRequest. Values provides for standard requests only, user must implement Class and Vendor values. | | | | | | | | | | | | | | | | | | | | | | | |
| | | | STD_GET_STATUS | 0 | | | | | | | | Standard request GET_STATUS | | | | | | | | | | | | | | | | | | | | | | | |
| | | | STD_CLEAR_FEATURE | 1 | | | | | | | | Standard request CLEAR_FEATURE | | | | | | | | | | | | | | | | | | | | | | | |
| | | | STD_SET_FEATURE | 3 | | | | | | | | Standard request SET_FEATURE | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| | | | STD_SET_ADDRESS | 5 | Standard request SET_ADDRESS |
| | | | STD_GET_DESCRIPTOR | 6 | Standard request GET_DESCRIPTOR |
| | | | STD_SET_DESCRIPTOR | 7 | Standard request SET_DESCRIPTOR |
| | | | STD_GET_CONFIGURATIOI | 8 | Standard request GET_CONFIGURATION |
| | | | STD_SET_CONFIGURATION | 9 | Standard request SET_CONFIGURATION |
| | | | STD_GET_INTERFACE | 10 | Standard request GET_INTERFACE |
| | | | STD_SET_INTERFACE | 11 | Standard request SET_INTERFACE |
| | | | STD_SYNCH_FRAME | 12 | Standard request SYNCH_FRAME |

## 51.13.28 WVALUEL

Address offset: 0x488

SETUP data, byte 2, LSB of wValue

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | WVALUEL | | | SETUP data, byte 2, LSB of wValue |

## 51.13.29 WVALUEH

Address offset: 0x48C

SETUP data, byte 3, MSB of wValue

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | WVALUEH | | | SETUP data, byte 3, MSB of wValue |

## 51.13.30 WINDEXL

Address offset: 0x490

SETUP data, byte 4, LSB of wIndex

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | WINDEXL | | | SETUP data, byte 4, LSB of wIndex |

## 51.13.31 WINDEXH

Address offset: 0x494

SETUP data, byte 5, MSB of wIndex

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| Id | | | | A A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** |
| A | R | WINDEXH | | | SETUP data, byte 5, MSB of wIndex |

## 51.13.32 WLENGTHL

Address offset: 0x498

SETUP data, byte 6, LSB of wLength

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | WLENGTHL | | | | | | | | | | SETUP data, byte 6, LSB of wLength | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.33 WLENGTHH

Address offset: 0x49C

SETUP data, byte 7, MSB of wLength

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | WLENGTHH | | | | | | | | | | SETUP data, byte 7, MSB of wLength | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.34 SIZE.EPOUT[0]

Address offset: 0x4A0

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | Amount of bytes received last in the data stage of this OUT endpoint | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.35 SIZE.EPOUT[1]

Address offset: 0x4A4

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | Amount of bytes received last in the data stage of this OUT endpoint | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.36 SIZE.EPOUT[2]

Address offset: 0x4A8

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | **Description** | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SIZE | | | | | | | | | | Amount of bytes received last in the data stage of this OUT endpoint | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.37 SIZE.EPOUT[3]

Address offset: 0x4AC

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Amount of bytes received last in the data stage of this OUT endpoint |

## 51.13.38 SIZE.EPOUT[4]

Address offset: 0x4B0

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Amount of bytes received last in the data stage of this OUT endpoint |

## 51.13.39 SIZE.EPOUT[5]

Address offset: 0x4B4

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Amount of bytes received last in the data stage of this OUT endpoint |

## 51.13.40 SIZE.EPOUT[6]

Address offset: 0x4B8

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Amount of bytes received last in the data stage of this OUT endpoint |

## 51.13.41 SIZE.EPOUT[7]

Address offset: 0x4BC

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | SIZE | | | Amount of bytes received last in the data stage of this OUT endpoint |

## 51.13.42 SIZE.ISOOUT

Address offset: 0x4C0

Amount of bytes received last on this iso OUT data endpoint

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | B | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00010000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | SIZE | | | Amount of bytes received last on this iso OUT data endpoint |
| B | R | ZERO | | | Zero-length data packet received |
| | | | Normal | 0 | No zero-length data received, use value in SIZE |
| | | | ZeroData | 1 | Zero-length data received, ignore value in SIZE |

## 51.13.43 ENABLE

Address offset: 0x500

Enable USB

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ENABLE | | | Enable USB |
| | | | Disabled | 0 | USB peripheral is disabled |
| | | | Enabled | 1 | USB peripheral is enabled |

## 51.13.44 USBPULLUP

Address offset: 0x504

Control of the USB pull-up

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | CONNECT | | | Control of the USB pull-up on the D+ line |
| | | | Disabled | 0 | Pull-up is disconnected |
| | | | Enabled | 1 | Pull-up is connected to D+ |

## 51.13.45 DPDMVALUE

Address offset: 0x508

State at which the DPDMDRIVE task will force D+ and D-. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing).

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A |
| **Reset 0x00000000** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STATE | | | State at which the DPDMDRIVE task will force D+ and D- | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Resume | 1 | D+ forced low, D- forced high (K state) for a timing pre-set in hardware (50 us or 5 ms, depending on bus state) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | J | 2 | D+ forced high, D- forced low (J state) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | K | 4 | D+ forced low, D- forced high (K state) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.46 DTOGGLE

Address offset: 0x50C

Data toggle control and status.

Write this register first with VALUE=Nop to select the endpoint; then read it to get the status from VALUE, or write it again with VALUE=Data0 or Data1.

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | C | C | B | | | | | A | A | A |
| **Reset 0x00000100** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | EP | | | Select bulk endpoint number | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | IO | | | Selects IN or OUT endpoint | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Out | 0 | Selects OUT endpoint | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | In | 1 | Selects IN endpoint | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | VALUE | | | Data toggle value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Nop | 0 | No action on data toggle when writing the register with this value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Data0 | 1 | Data toggle is DATA0 on endpoint set by EP and IO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Data1 | 2 | Data toggle is DATA1 on endpoint set by EP and IO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.47 EPINEN

Address offset: 0x510

Endpoint IN enable

| Bit number | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | **Description** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | IN0 | | | Enable IN endpoint 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 0 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | Enable endpoint IN 0 (response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | IN1 | | | Enable IN endpoint 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 1 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | Enable endpoint IN 1 (response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | IN2 | | | Enable IN endpoint 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 2 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | Enable endpoint IN 2 (response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | IN3 | | | Enable IN endpoint 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 3 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | Enable endpoint IN 3 (response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | IN4 | | | Enable IN endpoint 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 4 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | Enable endpoint IN 4 (response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | IN5 | | | Enable IN endpoint 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | Disable endpoint IN 5 (no response to IN tokens) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | IN6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | IN7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | ISOIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.48 EPOUTEN

Address offset: 0x514

Endpoint OUT enable

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OUT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | OUT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | OUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | OUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | OUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | OUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | OUT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | OUT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I | RW | ISOOUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.49 EPSTALL

Address offset: 0x518

STALL endpoints

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | C | B | | | | | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | EP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | W | IO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Out | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | In | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | W | STALL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | UnStall | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Stall | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.50 ISOSPLIT

Address offset: 0x51C

Controls the split of ISO buffers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SPLIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | OneDir | 0x0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | HalfIN | 0x0080 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.51 FRAMECNTR

Address offset: 0x520

Returns the current value of the start of frame counter

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | R | FRAMECNTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.52 LOWPOWER

Address offset: 0x52C

Controls USBD peripheral low-power mode during USB suspend

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LOWPOWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | ForceNormal | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | LowPower | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 51.13.53 ISOINCONFIG

Address offset: 0x530

Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | RESPONSE | | | | | | | | | | | | | | | | | | | | | | | | | | | Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent | | | | | | |
| | | | NoResp | 0 | | | | | | | | | | | | | | | | | | | | | | | | | Endpoint does not respond in that case | | | | | | |
| | | | ZeroData | 1 | | | | | | | | | | | | | | | | | | | | | | | | | Endpoint responds with a zero-length data packet in that case | | | | | | |

## 51.13.54 EPIN[0].PTR

Address offset: 0x600

Data pointer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | Data pointer. Accepts any address in Data RAM. | | | | | | |

## 51.13.55 EPIN[0].MAXCNT

Address offset: 0x604

Maximum number of bytes to transfer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | MAXCNT | | [64..0] | | | | | | | | | | | | | | | | | | | | | | | | | Maximum number of bytes to transfer | | | | | | |

## 51.13.56 EPIN[0].AMOUNT

Address offset: 0x608

Number of bytes transferred in the last transaction

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | R | AMOUNT | | | | | | | | | | | | | | | | | | | | | | | | | | | Number of bytes transferred in the last transaction | | | | | | |

## 51.13.57 EPIN[1].PTR

Address offset: 0x614

Data pointer

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | Data pointer. Accepts any address in Data RAM. | | | | | | |

## 51.13.58 EPIN[1].MAXCNT

Address offset: 0x618

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.59 EPIN[1].AMOUNT

Address offset: 0x61C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.60 EPIN[2].PTR

Address offset: 0x628

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.61 EPIN[2].MAXCNT

Address offset: 0x62C

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.62 EPIN[2].AMOUNT

Address offset: 0x630

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.63 EPIN[3].PTR

Address offset: 0x63C

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.64 EPIN[3].MAXCNT

Address offset: 0x640

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.65 EPIN[3].AMOUNT

Address offset: 0x644

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.66 EPIN[4].PTR

Address offset: 0x650

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.67 EPIN[4].MAXCNT

Address offset: 0x654

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.68 EPIN[4].AMOUNT

Address offset: 0x658

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.69 EPIN[5].PTR

Address offset: 0x664

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.70 EPIN[5].MAXCNT

Address offset: 0x668

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.71 EPIN[5].AMOUNT

Address offset: 0x66C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.72 EPIN[6].PTR

Address offset: 0x678

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.73 EPIN[6].MAXCNT

Address offset: 0x67C

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.74 EPIN[6].AMOUNT

Address offset: 0x680

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.75 EPIN[7].PTR

Address offset: 0x68C

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.76 EPIN[7].MAXCNT

Address offset: 0x690

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.77 EPIN[7].AMOUNT

Address offset: 0x694

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.78 ISOIN.PTR

Address offset: 0x6A0

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.79 ISOIN.MAXCNT

Address offset: 0x6A4

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [1023..1] | Maximum number of bytes to transfer |

## 51.13.80 ISOIN.AMOUNT

Address offset: 0x6A8

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.81 EPOUT[0].PTR

Address offset: 0x700

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.82 EPOUT[0].MAXCNT

Address offset: 0x704

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.83 EPOUT[0].AMOUNT

Address offset: 0x708

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.84 EPOUT[1].PTR

Address offset: 0x714

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.85 EPOUT[1].MAXCNT

Address offset: 0x718

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.86 EPOUT[1].AMOUNT

Address offset: 0x71C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.87 EPOUT[2].PTR

Address offset: 0x728

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.88 EPOUT[2].MAXCNT

Address offset: 0x72C

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.89 EPOUT[2].AMOUNT

Address offset: 0x730

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.90 EPOUT[3].PTR

Address offset: 0x73C

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.91 EPOUT[3].MAXCNT

Address offset: 0x740

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.92 EPOUT[3].AMOUNT

Address offset: 0x744

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.93 EPOUT[4].PTR

Address offset: 0x750

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.94 EPOUT[4].MAXCNT

Address offset: 0x754

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.95 EPOUT[4].AMOUNT

Address offset: 0x758

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.96 EPOUT[5].PTR

Address offset: 0x764

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.97 EPOUT[5].MAXCNT

Address offset: 0x768

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.98 EPOUT[5].AMOUNT

Address offset: 0x76C

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.99 EPOUT[6].PTR

Address offset: 0x778

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.100 EPOUT[6].MAXCNT

Address offset: 0x77C

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.101 EPOUT[6].AMOUNT

Address offset: 0x780

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.102 EPOUT[7].PTR

Address offset: 0x78C

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.103 EPOUT[7].MAXCNT

Address offset: 0x790

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | [64..0] | Maximum number of bytes to transfer |

## 51.13.104 EPOUT[7].AMOUNT

Address offset: 0x794

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

## 51.13.105 ISOOUT.PTR

Address offset: 0x7A0

Data pointer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | PTR | | | Data pointer. Accepts any address in Data RAM. |

## 51.13.106 ISOOUT.MAXCNT

Address offset: 0x7A4

Maximum number of bytes to transfer

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | MAXCNT | | | Maximum number of bytes to transfer |

## 51.13.107 ISOOUT.AMOUNT

Address offset: 0x7A8

Number of bytes transferred in the last transaction

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | R | AMOUNT | | | Number of bytes transferred in the last transaction |

# 51.14 Electrical specification

## 51.14.1 USB Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{USB,ACTIVE,VBUS}$ | Current from $V_{BUS}$ supply, USB active, excluding current through pull-up and $I_{USB,QUIES}$ | | | | mA |
| $I_{USB,SUSPEND,VBUS}$ | Current from $V_{BUS}$ supply, USB suspended, excluding current through pull-up | | | | µA |
| $I_{USB,DISABLED,VBUS}$ | Current from $V_{BUS}$ supply, USB disabled | | | | µA |
| $I_{USB,ACTIVE,VDD}$ | Current from $V_{DD}$ supply, USB active, including 48 MHz clock, excluding DMA accesses | | | | mA |
| $I_{USB,SUSPEND,VDD}$ | Current from $V_{DD}$ supply, USB suspended | | | | µA |
| $I_{USB,DISABLED,VDD}$ | Current from $V_{DD}$ supply, USB disabled, $V_{BUS}$ supply connected | | | | µA |
| $R_{USB,PU,ACTIVE}$ | Value of pull-up on D+, bus active (upstream device transmitting) | 1425 | 2300 | 3090 | Ω |
| $R_{USB,PU,IDLE}$ | Value of pull-up on D+, bus idle | 900 | 1200 | 1575 | Ω |
| $t_{USB,DETRST}$ | Minimum duration of an SE0 state to be detected as a USB reset condition | | | | µs |
| $f_{USB,CLK}$ | Frequency of local clock, USB active | | 48 | | MHz |
| $f_{USB,TOL}$ | Accuracy of local clock, USB active[40] | | | ±1000 | ppm |
| $T_{USB,JITTER}$ | Jitter on USB local clock, USB active | | | ±1 | ns |
| $t_{USB,RSMREC}$ | Hardware Resume Recovery Time (includes local clock startup time)[41] | | | | ms |
| $t_{USB,SUSPEND}$ | Time of bus inactivity detected as USB suspend | | | | ms |
| $t_{USB,RSTREC}$ | Hardware Reset Recovery Time (includes local clock startup time)[42] | | | | ms |
| $t_{USB,DRIVEK}$ | Duration of driving resume upstream (using the automated Resume function in the DPDMVALUE register) | | | | ms |
| $t_{USB,FDRATE}$ | Full-speed data rate | | | | Mb/s |
| $t_{SOF,EVENT}$ | Time from USB start of frame to EVENTS_SOF sent | | | | µs |
| $t_{EN2RDY}$ | Time from ENABLE=Enabled to READY event sent | | | | µs |

[40] The local clock can be stopped during USB suspend

[41] This is a contributor to the $T_{RSMRCY}$ time as defined in USB specification chapter 7

[42] This is a contributor to the $T_{RSTRCY}$ time as defined in USB specification chapter 7

# 52 QSPI — Quad serial peripheral interface

The QSPI peripheral provides support for communicating with an external flash memory device using SPI.

Listed here are the main features for the QSPI peripheral:

- Single/dual/quad SPI input/output
- 2–32 MHz configurable clock frequency
- Single-word read/write access from/to external flash
- EasyDMA for block read and write transfers
- Execute in place (XIP) for executing program directly from external flash
- XIP execution speed: Up to 8 million instruction fetches per second for 16 bit instructions, up to 4 million instruction fetches per second for 32 bit instructions.

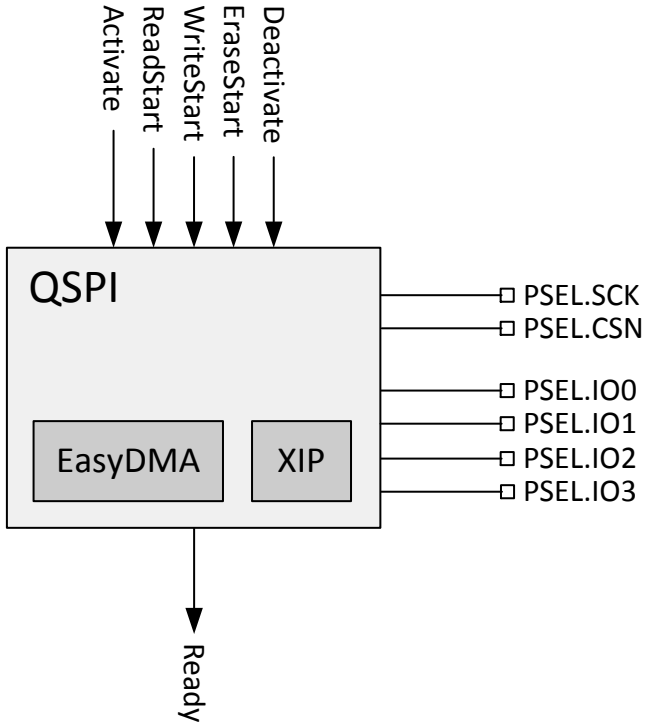



**Figure 187: Block diagram**

## 52.1 Configuring peripheral

Before any data can be transferred to or from the external flash memory, the peripheral needs to be configured.

1. Select input/output pins in *PSEL.SCK* on page 674, *PSEL.CSN* on page 675, *PSEL.IO0* on page 675, *PSEL.IO1* on page 675, *PSEL.IO2* on page 675, and *PSEL.IO3* on page 676. See *Reference circuitry* on page 688 for the recommended pins.
2. To ensure stable operation, set the GPIO drive strength to “high drive”. See the *GPIO — General purpose input/output* on page 154 chapter for details on how to configure GPIO drive strength.
3. Configure the interface towards the external flash memory using *IFCONFIG0* on page 676, *IFCONFIG1* on page 677, and *ADDRCONF* on page 678.
4. Enable the QSPI peripheral and acquire I/O pins using *ENABLE* on page 673.
5. Activate the external flash memory interface using the ACTIVATE task. The READY event will be generated when the interface has been activated and the external flash memory is ready for access.

**Important:** If the *IFCONFIG0* on page 676 register is configured to use the quad mode, the external flash device also needs to be set in the quad mode before any data transfers can take place.

This can be done by sending custom instructions to the external flash device, as described in *Sending custom instructions* on page 665.

## 52.2 Write operation

A write operation to the external flash is configured using the *WRITE.DST* on page 673, *WRITE.SRC* on page 674, and *WRITE.CNT* on page 674 registers and started using the WRITESTART task.

The READY event is generated when the transfer is complete.

The QSPI peripheral automatically takes care of splitting DMA transfers into page writes.

## 52.3 Read operation

A read operation from the external flash is configured using the *READ.SRC* on page 673, *READ.DST* on page 673, and *READ.CNT* on page 673registers and started using the READSTART task.

The READY event is generated when the transfer is complete.

## 52.4 Erase operation

Erase of pages/blocks of the external flash is configured using the *ERASE.PTR* on page 674and *ERASE.LEN* on page 674registers and started using the ERASESTART task.

The READY event is generated when the erase operation has been started.

Note that in this case the READY event will not indicate that the erase operation of the flash has been completed, but it only signals that the erase operation has been started. The actual status of the erase operation can normally be read from the external flash using a custom instruction, see *Sending custom instructions* on page 665.

## 52.5 Execute in place

Execute in place (XIP) allows the CPU to execute program code directly from the external flash.

After the external flash has been configured, the CPU can execute code from the external flash by accessing the XIP memory region. See the figure below and *Memory map* on page 21 for details.

When accessing the XIP memory region, the start address of this XIP memory region will map to the address *XIPOFFSET* on page 676 of the external flash.

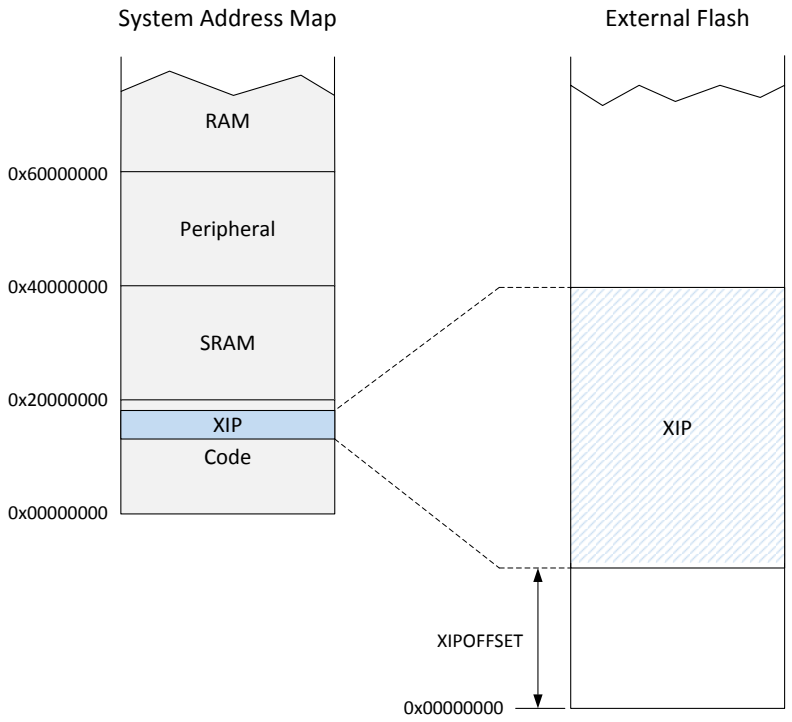



**Figure 188: XIP memory map**

## 52.6 Sending custom instructions

Custom instructions can be sent to the external flash using the *CINSTRCONF* on page 678, *CINSTRDAT0* on page 679, and *CINSTRDAT1* on page 679 registers. It is possible to send an instruction consisting of a one-byte opcode and up to 8 bytes of additional data and to read its response.

A custom instruction is prepared by first writing the data to be sent to *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 before writing the opcode and other configurations to the *CINSTRCONF* on page 678 register.

The custom instruction is sent when the *CINSTRCONF* on page 678 register is written and it is always sent on a single data line SPI interface.

The READY event will be generated when the custom instruction has been sent.

After a custom instruction has been sent, the *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 will contain the response bytes from the custom instruction.

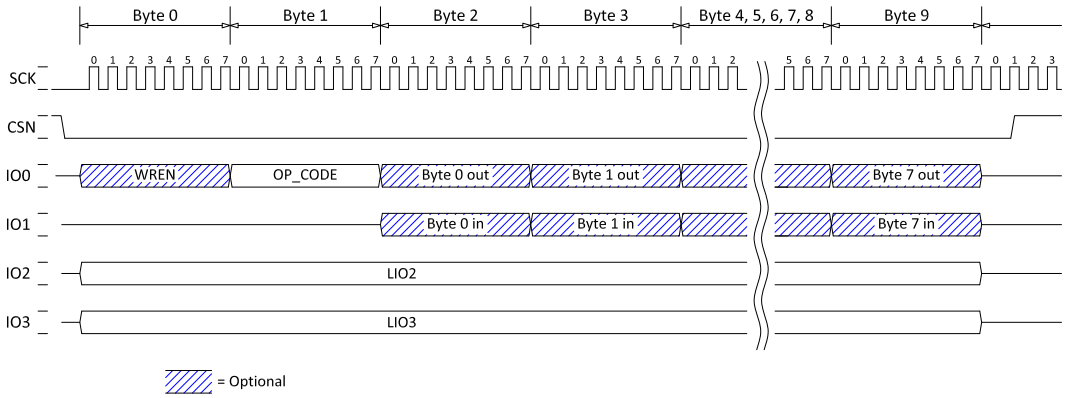



**Figure 189: Sending custom instruction**

### 52.6.1 Long frame mode

The LFEN and LFSTOP fields in the *CINSTRCONF* on page 678 control the operation of the custom instruction long frame mode. The long frame mode is a mechanism that permits arbitrary byte length custom instructions. While in long frame mode a long custom instruction sequence is split in multiple writes to the *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 registers.

To enable the long frame mode every write to the *CINSTRCONF* on page 678 register must have the LFEN field set to 1. The contents of the OPCODE field will be transmitted after the first write to *CINSTRCONF* on page 678 and will be omitted in every subsequent write to this register. For subsequent writes the number of data bytes as specified in the LENGTH field are transferred (that is the value of LENGTH - 1 data bytes). The values of the LIO2 and LIO3 fields are set in the first write to *CINSTRCONF* on page 678 and will apply for the entire custom instruction transmission until the long frame is finalized.

To finalize a long frame transmission, the LFSTOP field in *CINSTRCONF* on page 678 must be set to 1 in the last write to this register.

## 52.7 Deep power-down mode

The external flash memory can be put in deep power-down mode (DPM) to minimize its current consumption when there is no need to access the memory.

DPM is enabled in the *IFCONFIG0* on page 676 register and configured in the *DPMDUR* on page 678 register. The DPM status of the external memory can be read in the *STATUS* on page 677 register. The DPMDUR register has to be configured according to the external flash specification to get the information in the STATUS register and the timing of the READY event correct.

Entering/exiting DPM is controlled using the *IFCONFIG1* on page 677 register.

## 52.8 Instruction set

The table below shows the instruction set being used by the QSPI peripheral when communicating with an external flash device.

**Table 129: Instruction set**

| Instruction | Opcode | Description |
|---|---|---|
| WREN | 0x06 | Write enable |
| RDSR | 0x05 | Read status register |
| WRSR | 0x01 | Write status register |
| FASTREAD | 0x0B | Read bytes at higher speed |
| READ2O | 0x3B | Dual-read output |
| READ2IO | 0xBB | Dual-read input/output |
| READ4O | 0x6B | Quad-read output |
| READ4IO | 0xEB | Quad-read input/output |
| PP | 0x02 | Page program |
| PP2O | 0xA2 | Dual-page program output |
| PP4O | 0x32 | Quad-page program output |
| PP4IO | 0x38 | Quad-page program input/output |
| SE | 0x20 | Sector erase |
| BE | 0xD8 | Block erase |
| CE | 0xC7 | Chip erase |
| DP | 0xB9 | Enter deep power-down mode |
| DPE | 0xAB | Exit deep power-down mode |
| EN4B | Specified in the *ADDRCONF* on page 678 register | Enable 32 bit address mode |

## 52.9 Interface description

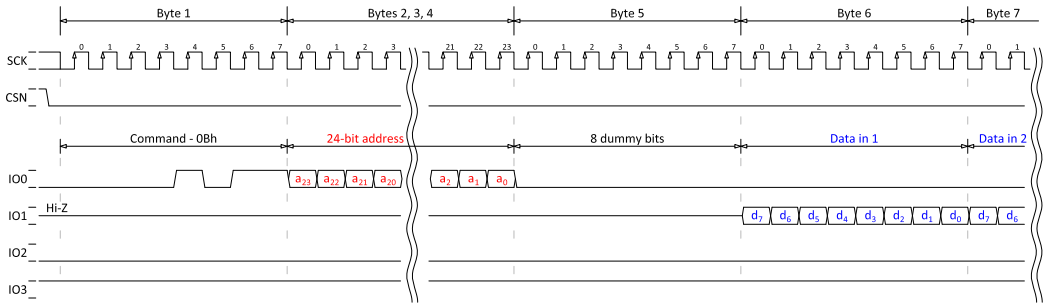



**Figure 190: 24-bit FASTREAD, SPIMODE = MODE0**

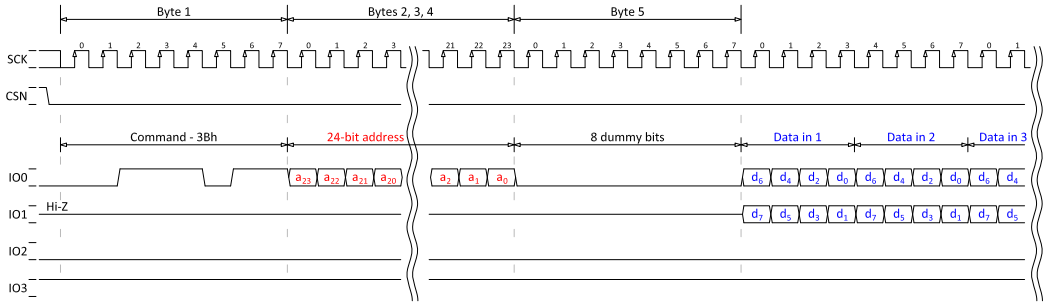



**Figure 191: 24-bit READ2O (dual-read output), SPIMODE = MODE0**

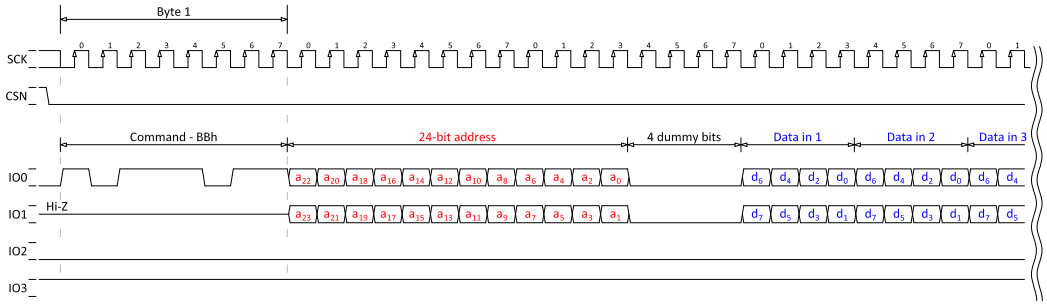



**Figure 192: 24-bit READ2IO (dual read input/output), SPIMODE = MODE0**

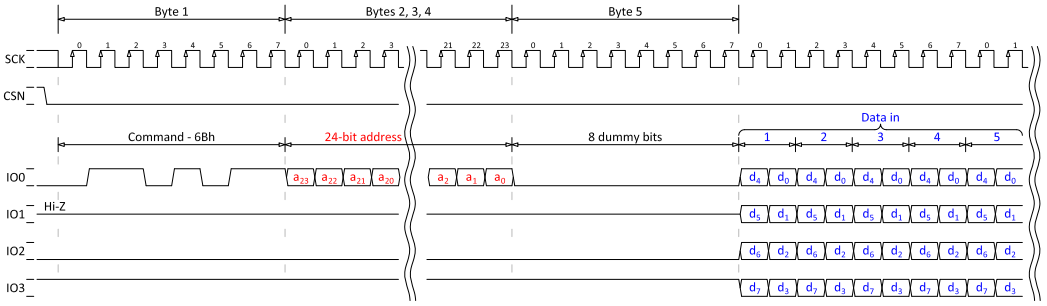



**Figure 193: 24-bit READ4O (quad-read output), SPIMODE = MODE0**

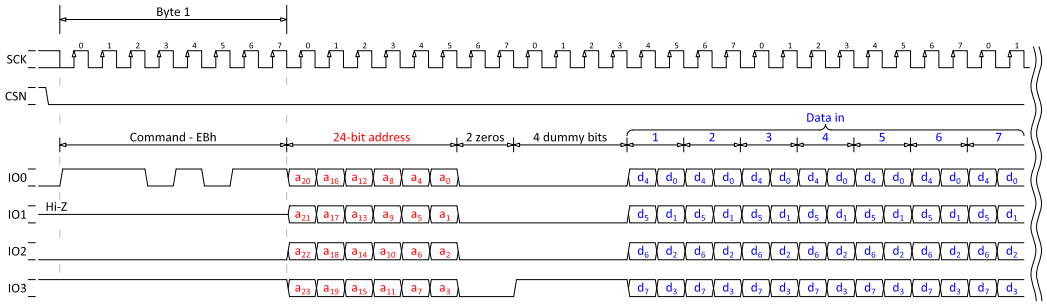



**Figure 194: 24-bit READ4IO (quad-read input/output), SPIMODE = MODE0**

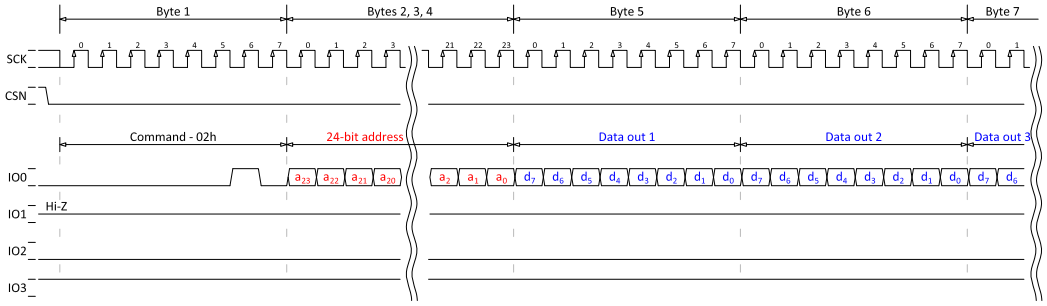



**Figure 195: 24-bit PP (page program), SPIMODE = MODE0**

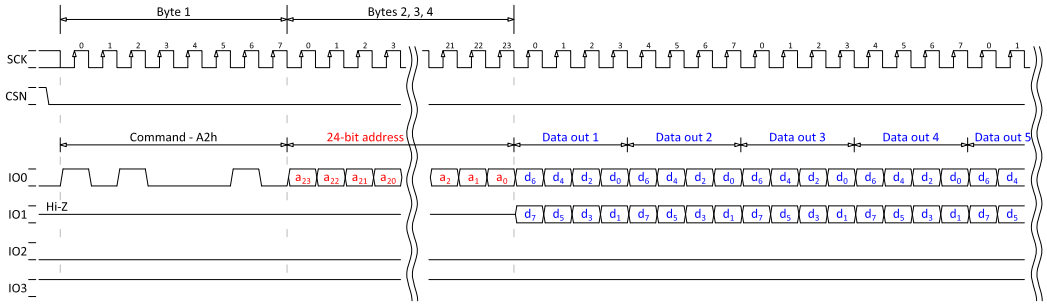



**Figure 196: 24-bit PP2O (dual-page program output), SPIMODE = MODE0**

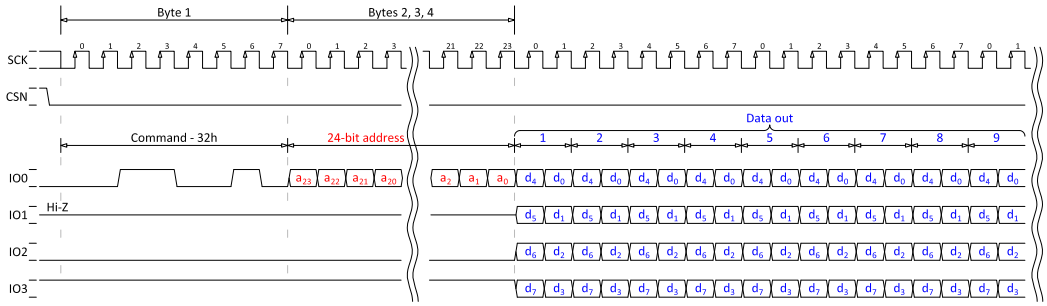



**Figure 197: 24-bit PP4O (quad page program output), SPIMODE = MODE0**

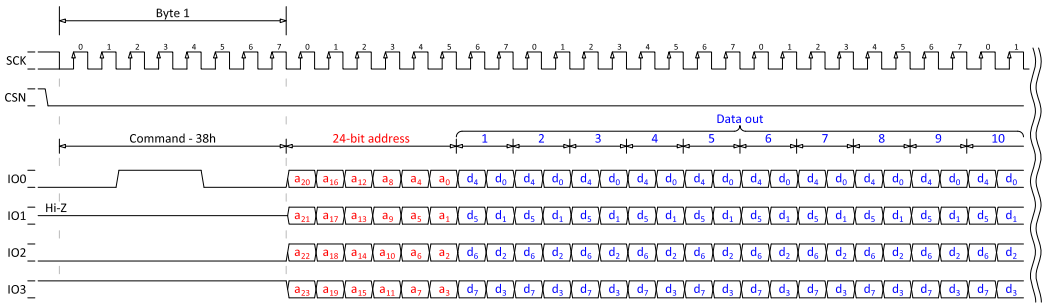



**Figure 198: 24-bit PP4IO (quad page program input/output), SPIMODE = MODE0**

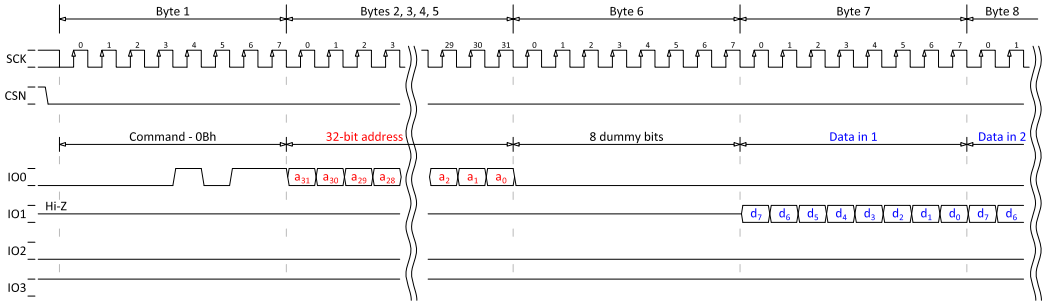



**Figure 199: 32-bit FASTREAD, SPIMODE = MODE0**

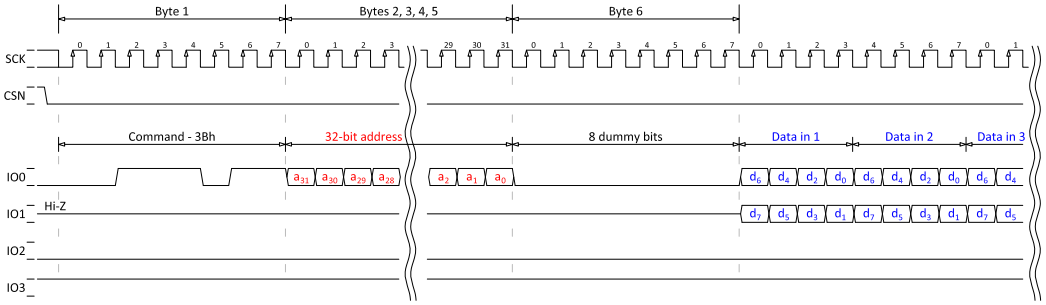



**Figure 200: 32-bit READ2O (dual-read output), SPIMODE = MODE0**

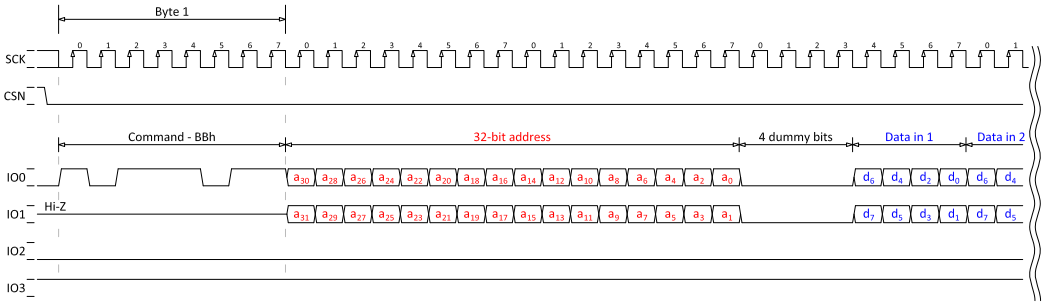



**Figure 201: 32-bit READ2IO (dual read input/output), SPIMODE = MODE0**

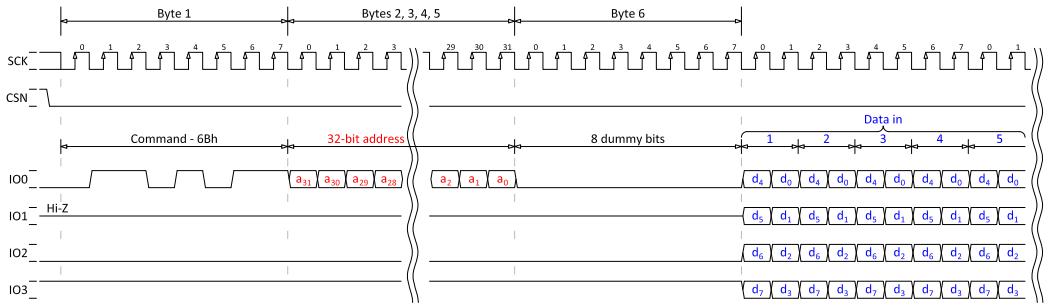



**Figure 202: 32-bit READ4O (quad-read output), SPIMODE = MODE0**

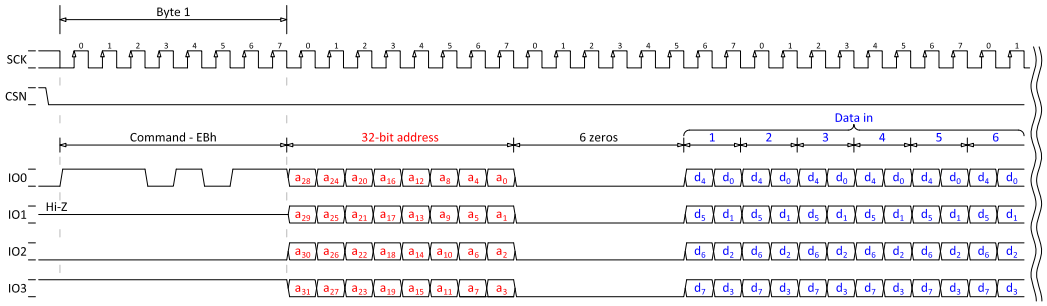



**Figure 203: 32-bit READ4IO (quad-read input/output), SPIMODE = MODE0**

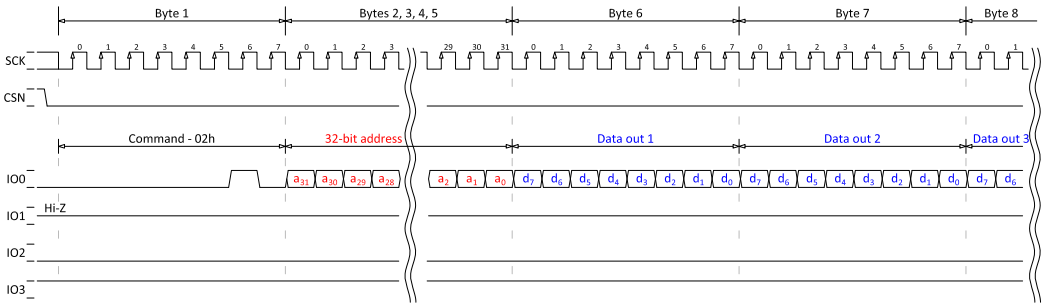



**Figure 204: 32-bit PP (page program), SPIMODE = MODE0**

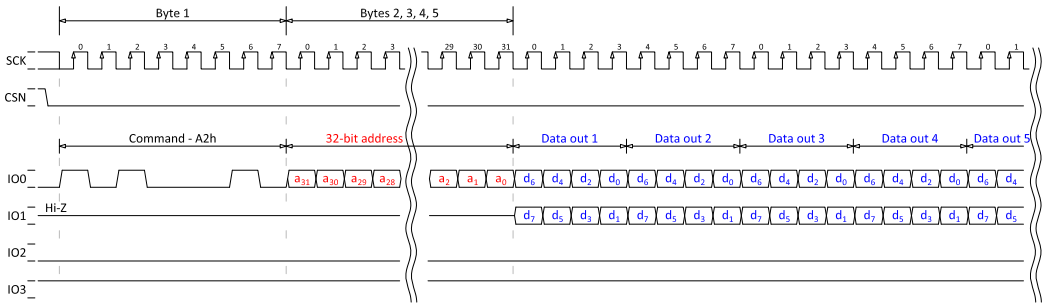



**Figure 205: 32-bit PP2O (dual-page program output), SPIMODE = MODE0**

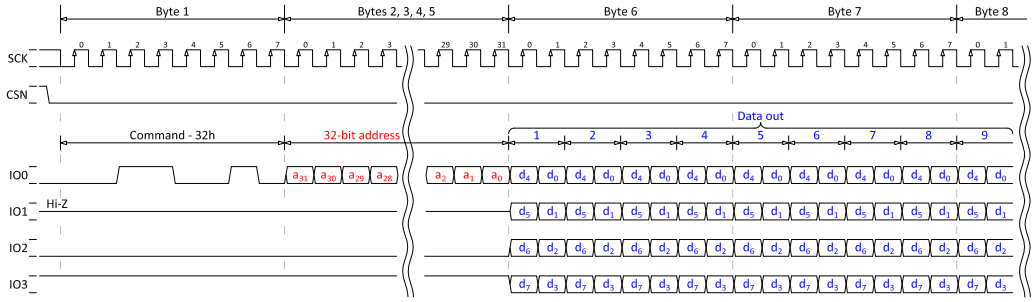



**Figure 206: 32-bit PP4O (quad-page program output), SPIMODE = MODE0**

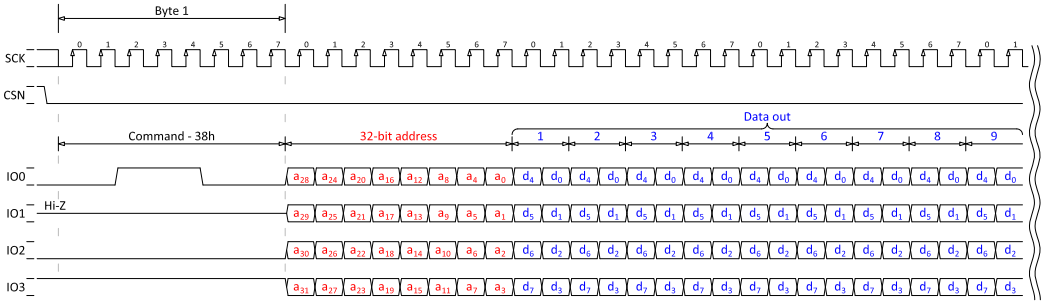



**Figure 207: 32-bit PP4IO (quad page program input/output), SPIMODE = MODE0**

# 52.10 Registers

### Table 130: Instances

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x40029000 | QSPI | QSPI | External memory interface | |

### Table 131: Register Overview

| Register | Offset | Description |
|---|---|---|
| TASKS_ACTIVATE | 0x000 | Activate QSPI interface |
| TASKS_READSTART | 0x004 | Start transfer from external flash memory to internal RAM |
| TASKS_WRITESTART | 0x008 | Start transfer from internal RAM to external flash memory |
| TASKS_ERASESTART | 0x00C | Start external flash memory erase operation |
| TASKS_DEACTIVATE | 0x010 | Deactivate QSPI interface |
| EVENTS_READY | 0x100 | QSPI peripheral is ready. This event will be generated as a response to any QSPI task. |
| *INTEN* | 0x300 | Enable or disable interrupt |
| *INTENSET* | 0x304 | Enable interrupt |
| *INTENCLR* | 0x308 | Disable interrupt |
| *ENABLE* | 0x500 | Enable QSPI peripheral and acquire the pins selected in PSELn registers |
| *READ.SRC* | 0x504 | Flash memory source address |
| *READ.DST* | 0x508 | RAM destination address |
| *READ.CNT* | 0x50C | Read transfer length |
| *WRITE.DST* | 0x510 | Flash destination address |
| *WRITE.SRC* | 0x514 | RAM source address |
| *WRITE.CNT* | 0x518 | Write transfer length |
| *ERASE.PTR* | 0x51C | Start address of flash block to be erased |
| *ERASE.LEN* | 0x520 | Size of block to be erased. |
| *PSEL.SCK* | 0x524 | Pin select for serial clock SCK |
| *PSEL.CSN* | 0x528 | Pin select for chip select signal CSN. |
| *PSEL.IO0* | 0x530 | Pin select for serial data MOSI/IO0. |
| *PSEL.IO1* | 0x534 | Pin select for serial data MISO/IO1. |

| Register | Offset | Description |
|---|---|---|
| *PSEL.IO2* | 0x538 | Pin select for serial data IO2. |
| *PSEL.IO3* | 0x53C | Pin select for serial data IO3. |
| *XIPOFFSET* | 0x540 | Address offset into the external memory for Execute in Place operation. |
| *IFCONFIG0* | 0x544 | Interface configuration. |
| *IFCONFIG1* | 0x600 | Interface configuration. |
| *STATUS* | 0x604 | Status register. |
| *DPMDUR* | 0x614 | Set the duration required to enter/exit deep power-down mode (DPM). |
| *ADDRCONF* | 0x624 | Extended address configuration. |
| *CINSTRCONF* | 0x634 | Custom instruction configuration register. |
| *CINSTRDAT0* | 0x638 | Custom instruction data register 0. |
| *CINSTRDAT1* | 0x63C | Custom instruction data register 1. |
| *IFTIMING* | 0x640 | SPI interface timing. |

## 52.10.1 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | READY | | | Enable or disable interrupt for READY event |
| | | | | | See *EVENTS_READY* |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 52.10.2 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | READY | | | Write '1' to Enable interrupt for READY event |
| | | | | | See *EVENTS_READY* |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 52.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | READY | | | Write '1' to Disable interrupt for READY event |
| | | | | | See *EVENTS_READY* |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 52.10.4 ENABLE

Address offset: 0x500

Enable QSPI peripheral and acquire the pins selected in PSELn registers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | ENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable or disable QSPI |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Disable QSPI |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Enable QSPI |

## 52.10.5 READ.SRC

Address offset: 0x504

Flash memory source address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Word-aligned flash memory source address. |

## 52.10.6 READ.DST

Address offset: 0x508

RAM destination address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Word-aligned RAM destination address. |

## 52.10.7 READ.CNT

Address offset: 0x50C

Read transfer length

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | CNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Read transfer length in number of bytes. The length must be a multiple of 4 bytes. |

## 52.10.8 WRITE.DST

Address offset: 0x510

Flash destination address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | **Description** |
| A | RW | DST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Word-aligned flash destination address. |

## 52.10.9 WRITE.SRC

Address offset: 0x514

RAM source address

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SRC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Word-aligned RAM source address.

## 52.10.10 WRITE.CNT

Address offset: 0x518

Write transfer length

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | CNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Write transfer length in number of bytes. The length must be a multiple of 4 bytes.

## 52.10.11 ERASE.PTR

Address offset: 0x51C

Start address of flash block to be erased

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PTR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Word-aligned start address of block to be erased.

## 52.10.12 ERASE.LEN

Address offset: 0x520

Size of block to be erased.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | LEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4KB | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 64KB | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | All | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEN

Erase 4 kB block (flash command 0x20)

Erase 64 kB block (flash command 0xD8)

Erase all (flash command 0xC7)

## 52.10.13 PSEL.SCK

Address offset: 0x524

Pin select for serial clock SCK

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pin number

Port number

Connection

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.14 PSEL.CSN

Address offset: 0x528

Pin select for chip select signal CSN.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.15 PSEL.IO0

Address offset: 0x530

Pin select for serial data MOSI/IO0.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.16 PSEL.IO1

Address offset: 0x534

Pin select for serial data MISO/IO1.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.17 PSEL.IO2

Address offset: 0x538

Pin select for serial data IO2.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.18 PSEL.IO3

Address offset: 0x53C

Pin select for serial data IO3.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | B | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | PIN | | [0..31] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | PORT | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | CONNECT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disconnected | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Connected | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.19 XIPOFFSET

Address offset: 0x540

Address offset into the external memory for Execute in Place operation.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | XIPOFFSET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Address offset into the external memory for Execute in Place operation. Value must be a multiple of 4.

## 52.10.20 IFCONFIG0

Address offset: 0x544

Interface configuration.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | G | | | | D | C | B | B | B | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | READOC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | FASTREAD | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | READ2O | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | READ2IO | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | READ4O | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | READ4IO | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | WRITEOC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | PP | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | PP2O | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | PP4O | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | PP4IO | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | ADDRMODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Addressing mode.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | G | | | | | D | C | B | B | B | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| | | | 24BIT | 0 | | | | | | | | | | | | | | | | | | | | | | | | 24-bit addressing. | | | | | | | |
| | | | 32BIT | 1 | | | | | | | | | | | | | | | | | | | | | | | | 32-bit addressing. | | | | | | | |
| D | RW | DPMENABLE | | | | | | | | | | | | | | | | | | | | | | | | | | Enable deep power-down mode (DPM) feature. | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | Disable DPM feature. | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enable DPM feature. | | | | | | | |
| G | RW | PPSIZE | | | | | | | | | | | | | | | | | | | | | | | | | | Page size for commands PP, PP2O, PP4O and PP4IO. | | | | | | | |
| | | | 256Bytes | 0 | | | | | | | | | | | | | | | | | | | | | | | | 256 bytes. | | | | | | | |
| | | | 512Bytes | 1 | | | | | | | | | | | | | | | | | | | | | | | | 512 bytes. | | | | | | | |

## 52.10.21 IFCONFIG1

Address offset: 0x600

Interface configuration.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | G | G | G | G | | | E | D | | | | | | | | | | | | | | | | | A | A | A | A | A | A | A | A |
| **Reset 0x00040480** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| A | RW | SCKDELAY | | [0..255] | | | | | | | | | | | | | | | | | | | | | | | | Minimum amount of time that the CSN pin must stay high before it can go low again. Value is specified in number of 16 MHz periods (62.5 ns). | | | | | | | |
| D | RW | DPMEN | | | | | | | | | | | | | | | | | | | | | | | | | | Enter/exit deep power-down mode (DPM) for external flash memory. | | | | | | | |
| | | | Exit | 0 | | | | | | | | | | | | | | | | | | | | | | | | Exit DPM. | | | | | | | |
| | | | Enter | 1 | | | | | | | | | | | | | | | | | | | | | | | | Enter DPM. | | | | | | | |
| E | RW | SPIMODE | | | | | | | | | | | | | | | | | | | | | | | | | | Select SPI mode. | | | | | | | |
| | | | MODE0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | Mode 0: Data are captured on the clock rising edge and data is output on a falling edge. Base level of clock is 0 (CPOL=0, CPHA=0). | | | | | | | |
| | | | MODE3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | Mode 3: Data are captured on the clock falling edge and data is output on a rising edge. Base level of clock is 1 (CPOL=1, CPHA=1). | | | | | | | |
| G | RW | SCKFREQ | | [0..15] | | | | | | | | | | | | | | | | | | | | | | | | SCK frequency is given as 32 MHz / (SCKFREQ + 1). | | | | | | | |

## 52.10.22 STATUS

Address offset: 0x604

Status register.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | F | F | F | F | F | F | F | F | | | | | | | | | | | | | | | | | | | | | D | C | | |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | **Description** | | | | | | | |
| C | R | DPM | | | | | | | | | | | | | | | | | | | | | | | | | | Deep power-down mode (DPM) status of external flash. | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | External flash is not in DPM. | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | External flash is in DPM. | | | | | | | |
| D | R | READY | | | | | | | | | | | | | | | | | | | | | | | | | | Ready status. | | | | | | | |
| | | | READY | 1 | | | | | | | | | | | | | | | | | | | | | | | | QSPI peripheral is ready. It is allowed to trigger new tasks, writing custom instructions or enter/exit DPM. | | | | | | | |
| | | | BUSY | 0 | | | | | | | | | | | | | | | | | | | | | | | | QSPI peripheral is busy. It is not allowed to trigger any new tasks, writing custom instructions or enter/exit DPM. | | | | | | | |
| F | R | SREG | | | | | | | | | | | | | | | | | | | | | | | | | | Value of external flash device Status Register. When the external flash has two bytes status register this field includes the value of the low byte. | | | | | | | |

## 52.10.23 DPMDUR

Address offset: 0x614

Set the duration required to enter/exit deep power-down mode (DPM).

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0xFFFFFFFF** | | | | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | ENTER | | [0..0xFFFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | given as ENTER * 256 * 62.5 ns. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | EXIT | | [0..0xFFFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | as EXIT * 256 * 62.5 ns. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.24 ADDRCONF

Address offset: 0x624

Extended address configuration.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | F | E | D | D | C | C | C | C | C | C | C | B | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x000000B7** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **1** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OPCODE | | [0xFF..0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Opcode that enters the 32-bit addressing mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | BYTE0 | | [0xFF..0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Byte 0 following opcode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | BYTE1 | | [0xFF..0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Byte 1 following byte 0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Extended addressing mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | NoInstr | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Do not send any instruction. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Opcode | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | OpByte0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, byte0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | All | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, byte0, byte1. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | WIPWAIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Wait for write complete before sending command. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | No wait. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Wait. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | WREN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send WREN (write enable opcode 0x06) before instruction. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Do not send WREN. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send WREN. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.25 CINSTRCONF

Address offset: 0x634

Custom instruction configuration register.

A new custom instruction is sent every time this register is written. The READY event will be generated when the custom instruction has been sent.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00002000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | OPCODE | | [0..255] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Opcode of Custom instruction. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | LENGTH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Length of custom instruction in number of bytes. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1B | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode only. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2B | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, CINSTRDAT0.BYTE0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3B | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE1. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4B | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE2. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5B | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE3. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 6B | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT1.BYTE4. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | B | B | A | A | A | A | A | A | A | A |
| **Reset 0x00002000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 7B | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 8B | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 9B | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | LIO2 | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | LIO3 | | [0..1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | WIPWAIT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RW | WREN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | RW | LFEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RW | LFSTOP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Stop | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.26 CINSTRDAT0

Address offset: 0x638

Custom instruction data register 0.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BYTE0 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | BYTE1 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | BYTE2 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | BYTE3 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.27 CINSTRDAT1

Address offset: 0x63C

Custom instruction data register 1.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | D | D | D | D | D | D | D | D | C | C | C | C | C | C | C | C | B | B | B | B | B | B | B | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **Id** | **RW** | **Field** | **Value Id** | **Value** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | BYTE4 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | BYTE5 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | BYTE6 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | BYTE7 | | [0..0xFF] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 52.10.28 IFTIMING

Address offset: 0x640

SPI interface timing.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | C | C | C | | | | | | | | |
| **Reset 0x00000200** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| C | RW | RXDELAY | | [7..0] | Timing related to sampling of the input serial data. The value of RXDELAY specifies the number of 64 MHz cycles (15.625 ns) delay from the the rising edge of the SPI Clock (SCK) until the input serial data is sampled. As en example, if set to 0 the input serial data is sampled on the rising edge of SCK. |

# 52.11 Electrical specification

## 52.11.1 Current consumption

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{QSPI,IDLE}$ | Idle current (enabled, but not activated). | | | | µA |
| $I_{QSPI,ACTIVE}$ | Idle current (activated, but not transferring data). | | | | µA |
| $I_{QSPI,DATA}$ | Run current (activated and transferring data to/from external Flash at 32 MHz clock frequency). | | | | µA |

## 52.11.2 Timing specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $F_{QSPI,CLK}$ | SCK frequency | | | 32 | MHz |
| $DC_{QSPI,CLK}$ | SCK duty cycle | | | | % |
| $F_{QSPI,XIP,16}$ | XIP fetch frequency for 16 bit instructions. | | | 8 | MHz |
| $F_{QSPI,XIP,32}$ | XIP fetch frequency for 32 bit instructions. | | | 4 | MHz |
| $t_{IO,OUT,VALID}$ | Time from SCK falling until new data valid. | | | | ns |
| $t_{IO,OUT,INVALID}$ | Time from SCK falling until previous data invalid. | | | | ns |

# 53 CRYPTOCELL — ARM TrustZone CryptoCell 310

ARM® TrustZone® CryptoCell 310 (CRYPTOCELL) is a security subsystem which provides root of trust (RoT) and cryptographic services for a device. CRYPTOCELL services are available to the application through a software library API.

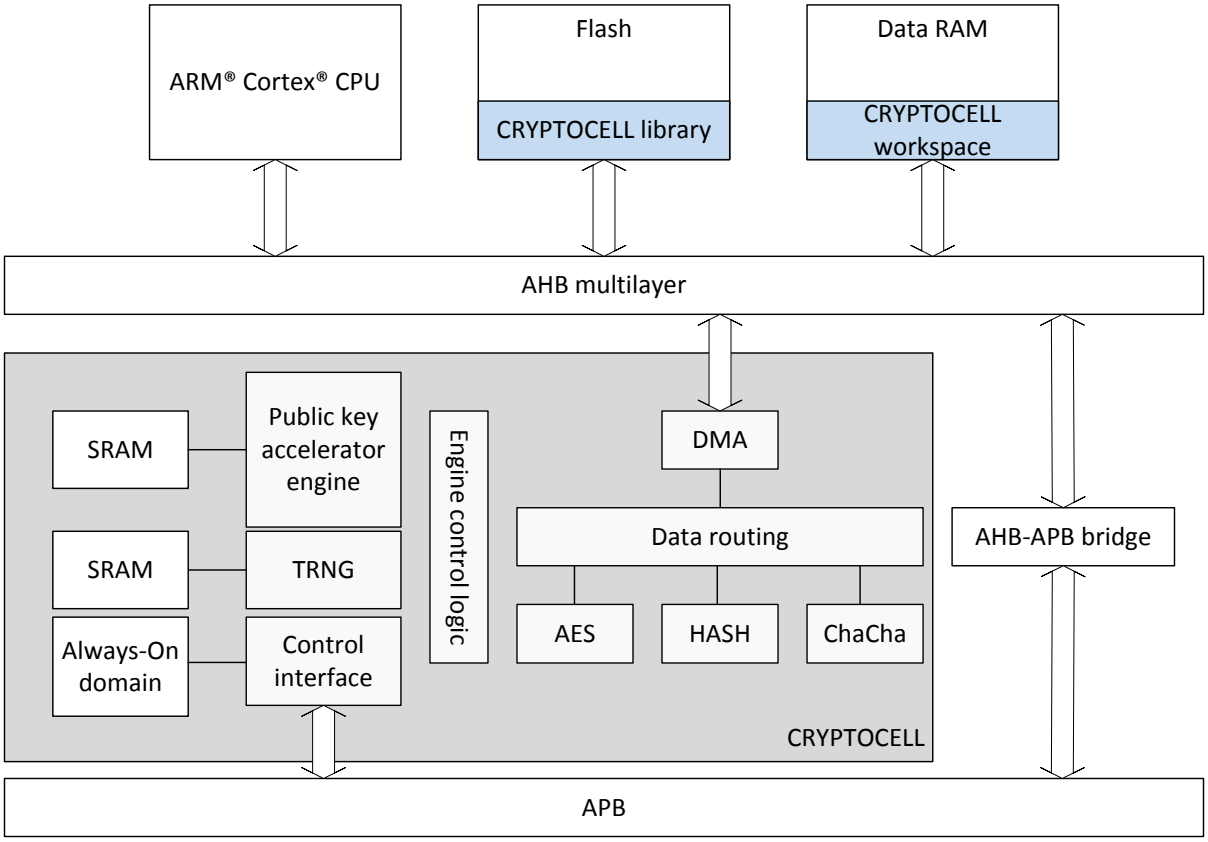



**Figure 208: Block diagram for CRYPTOCELL**

The following cryptographic features are provided:

- FIPS-140-2 certified true random number generator (TRNG)
- RSA asymmetric encryption
  - Up to 2048 bit key size
  - PKCS#1 v2.1/v1.5
  - Optional CRT support
- Elliptic curve cryptography (ECC)
  - NIST FIPS 186-4 recommended curves using pseudo-random parameters, up to 521 bits:
    - Prime field: P-192, P-224, P-256, P-384, P-521
  - SEC 2 recommended curves using pseudo-random parameters, up to 521 bits:
    - Prime field: P-160, P-192, P-224, P-256, P-384, P-521
  - Koblitz curves using fixed parameters, up to 256 bits:
    - Prime field: P-160, P-192, P-224, P-256
  - Edwards/Montgomery curves:
    - Ed25519, Curve25519
  - ECDH/ECDSA support
- Secure remote password protocol (SRP)

  - Up to 3072 bit operations
- Hashing functions
  - SHA-1, SHA-2 up to 256 bit size
  - Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
  - General purpose AES engine (encrypt/decrypt, sign/verify)
  - 128 bit key size
  - Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*
- ChaCha20/Poly1305 symmetric encryption
  - Supported key size: 128 and 256 bits
  - Authenticated encryption with associated data (AEAD) mode

## 53.1 Standards

ARM® TrustZone® CryptoCell 310 (CRYPTOCELL) supports a number of cryptography standards.

**Table 132: CRYPTOCELL cryptography standards**

| Algorithm family | Identification code | Document name |
|---|---|---|
| TRNG | NIST 800-90B[43] | Recommendation for the entropy sources used for random bit generation |
| | AIS-31 | Functionality classes and evaluation methodology for physical random number generators |
| PRNG | NIST 800-90A | Recommendation for random number generation using deterministic random bit generators |
| Stream cipher | Chacha | "ChaCha, a variant of Salsa20", Daniel J. Bernstein, January 28th 2008 |
| MAC | Poly1305 | "The Poly1305-AES message-authentication code", Daniel J. Bernstein<br><br>"Cryptography in NaCl", Daniel J. Bernstein |
| Key agreement | SRP | "The Secure Remote Password Protocol", Thomas Wu |
| AES | FIPS-197 | Advanced Encryption Standard |
| | NIST SP 800-38A | Recommendation for block cipher modes of operation - methods and techniques |
| | NIST SP 800-38B | Recommendation for block cipher modes of operation: The CMAC mode for authentication |
| | NIST SP 800-38C | Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality |
| | ISO/IEC 9797-1 | AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 |
| | IEEE 802.15.4-2011 | Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation |
| Hash | FIPS 180-3 | Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) |
| | RFC2104 | HMAC: Keyed-hashing for message authentication |
| RSA | PKCS#1 | RSA cryptography standard v1.5/v2.1 |
| Diffie-Hellman | ANS X9.42 | Agreement of symmetric keys using discrete logarithm cryptography |
| | PKCS#3 | Diffie-Hellman key agreement standard |
| ECC | ANS X9.63 | Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography |
| | IEEE 1363 | Standard specifications for public key cryptography |
| | ANS X9.62 | Public key cryptography for the financial services industry, the Elliptic Curve Digital Signature Algorithm (ECDSA) |
| | Ed25519 | Edwards-curve, "High-speed high-security signatures", Daniel J. Bernstein, Niels Duif, Tanja Lange, Peter Schwabe, and Bo-Yin Yang |
| | Curve25519 | Montgomery curve, "Curve25519: new Diffie-Hellman speed records", Daniel J. Bernstein |
| | FIPS 186-4 | Digital Signature Standard (DSS) |
| | NIST SP 800-56A rev. 2 | Recommendation for Pair-Wise Key Establishment Schemes Using Discrete Logarithm Cryptography |
| General | FIPS 140-2 | Security requirements for cryptographic modules |

## 53.2 Control interface

To reduce power consumption, the CRYPTOCELL subsystem is disabled by default, and must be enabled prior to use. Device specific secrets are retained even when CRYPTOCELL is disabled.

### 53.2.1 Registers

**Table 133: Instances**

| Base address | Peripheral | Instance | Description | Configuration |
|---|---|---|---|---|
| 0x5002A000 | CRYPTOCELL | CRYPTOCELL | CryptoCell subsystem control interface | |

[43] This standard is still marked as draft.

### Table 134: Register Overview

| Register | Offset | Description |
|---|---|---|
| *ENABLE* | 0x500 | Control power and clock for CRYPTOCELL subsystem |

#### ENABLE

Address offset: 0x500

Control power and clock for CRYPTOCELL subsystem

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Id | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| Id | RW | Field | Value Id | Value | Description |
|---|---|---|---|---|---|
| A | RW | ENABLE | | | Enable or disable the CRYPTOCELL subsystem |
| | | | Disabled | 0 | CRYPTOCELL subsystem disabled |
| | | | Enabled | 1 | CRYPTOCELL subsystem enabled |
| | | | | | When enabled the CRYPTOCELL subsystem can be initialized and controlled through the CryptoCell firmware API |

## 53.2.2 Electrical specification

### ARM TrustZone CryptoCell 310 Electrical Specification

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $I_{CC310,DISABLED}$ | CRYPTOCELL subsystem disabled. Regulator = DC/DC, VDD = 3 V. | | 1.5 | | µA |
| $I_{CC310,IDLE}$ | CRYPTOCELL subsystem enabled. Regulator = DC/DC, VDD = 3 V. | | 0.8 | | mA |

# 54 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

## 54.1 AQFN73 7 x 7 mm package

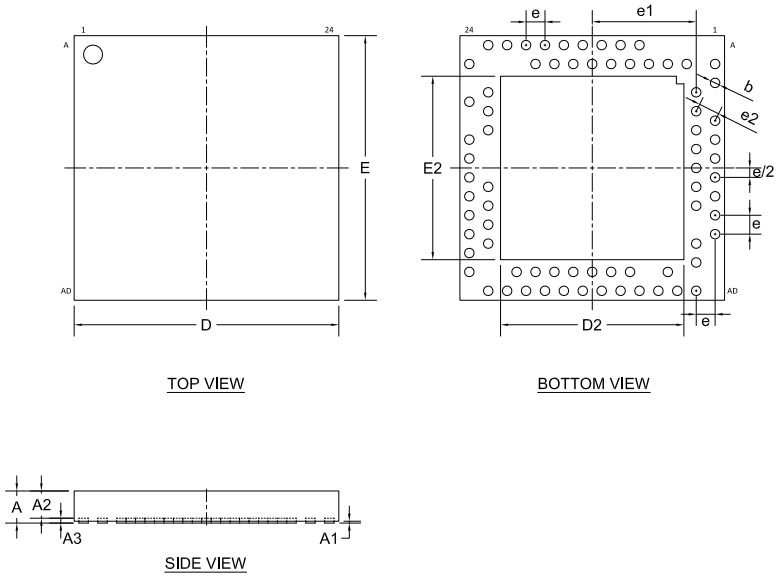



**Figure 209: AQFN73 7 x 7 mm package**

**Table 135: AQFN73 dimensions in millimeters**

| Package | A | A1 | A2 | A3 | b | D, E | D2, E2 | e | e1 | e2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.02 | | | 0.20 | | 4.75 | | | | **Min.** |
| AQFN73 (7x7) | | 0.05 | 0.675 | 0.13 | 0.25 | 7.00 | 4.85 | 0.5 | 2.75 | 0.559 | **Nom.** |
| | 0.85 | 0.08 | | | 0.30 | | 4.95 | | | | **Max.** |

# 55 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

## 55.1 Package marking

The nRF52840 SoC package is marked as shown in the figure below.

| | | | | | |
|---|---|---|---|---|---|
| N | 5 | 2 | 8 | 4 | 0 |
| <P | P> | <V | V> | <H> | <P> |
| <Y | Y> | <W | W> | <L | L> |

**Figure 210: Package marking**

## 55.2 Box labels

Here are the box labels used for the nRF52840.

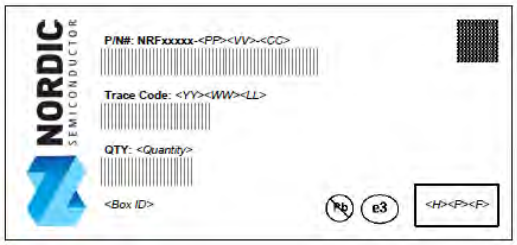



**Figure 211: Inner box label**

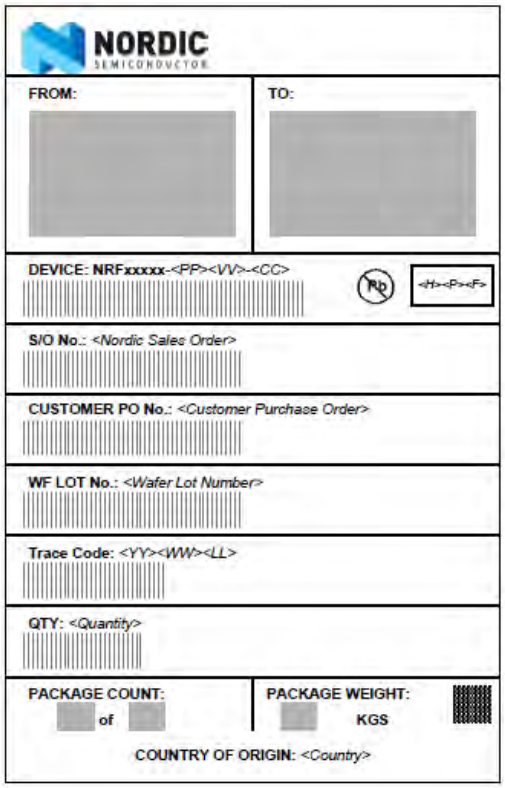



**Figure 212: Outer box label**

## 55.3 Order code

Here are the nRF52840 order codes and definitions.

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| n | R | F | 5 | 2 | 8 | 4 | 0 | - | <P | P> | <V | V> | - | <C | C> |

**Figure 213: Order code**

**Table 136: Abbreviations**

| Abbrevitation | Definition and implemented codes |
|---|---|
| N52/nRF52 | nRF52 series product |
| 840 | Part code |
| <PP> | Package variant code |
| <VV> | Function variant code |
| <H><P><F> | Build code |
| | H - Hardware version code |
| | P - Production configuration code (production site, etc.) |
| | F - Firmware version code (only visible on shipping container label) |
| <YY><WW><LL> | Tracking code |
| | YY - Year code |
| | WW - Assembly week number |
| | LL - Wafer lot code |
| <CC> | Container code |

## 55.4 Code ranges and values

Defined here are the nRF52840 code ranges and values.

**Table 137: Package variant codes**

| <PP> | Package | Size (mm) | Pin/Ball count | Pitch (mm) |
|---|---|---|---|---|
| QI | AQFN | 7 x 7 | 73 | 0.5 |

### Table 138: Function variant codes

| <VV> | Flash (kB) | RAM (kB) |
|---|---|---|
| AA | 1024 | 256 |

### Table 139: Hardware version codes

| <H> | Description |
|---|---|
| [A . . Z] | Hardware version/revision identifier (incremental) |

### Table 140: Production configuration codes

| <P> | Description |
|---|---|
| [0 . . 9] | Production device identifier (incremental) |
| [A . . Z] | Engineering device identifier (incremental) |

### Table 141: Production version codes

| <F> | Description |
|---|---|
| [A . . N, P . . Z] | Version of preprogrammed firmware |
| [0] | Delivered without preprogrammed firmware |

### Table 142: Year codes

| <YY> | Description |
|---|---|
| [16 . . 99] | Production year: 2016 to 2099 |

### Table 143: Week codes

| <WW> | Description |
|---|---|
| [1 . . 52] | Week of production |

### Table 144: Lot codes

| <LL> | Description |
|---|---|
| [AA . . ZZ] | Wafer production lot identifier |

### Table 145: Container codes

| <CC> | Description |
|---|---|
| R7 | 7" Reel |
| R | 13" Reel |
| T | Tray |

## 55.5 Product options

Defined here are the nRF52840 product options.

### Table 146: nRF52840 order codes

| Order code | MOQ[44] | Comment |
|---|---|---|
| nRF52840-QIAA-R7 | 800 | Availability to be announced. |
| nRF52840-QIAA-R | 3000 | |
| nRF52840-QIAA-T | 260 | |

### Table 147: Development tools order code

| Order code | Description |
|---|---|
| nRF52840-PREVIEW-DK | nRF52840 Preview Development Kit |

# 56 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from *www.nordicsemi.com*.

In this section there are 6 reference circuits to show the components and component values to support on-chip features in a design.

> **Important:** This is not a complete list of configurations, but all required circuitry is shown for further configurations.

Some general guidance is summarized here:

- External supply from VDD is only available when power is supplied to VDDH. External supply is annotated with the VEXT net name.
- When supplying power from a USB source only, VBUS must be connected to VDDH if USB is to be used.
- Components required for DC/DC function are only needed if DC/DC mode is enabled for that regulator.
- NFC can be used in any configuration.
- USB can be used in any configuration as long as VBUS is supplied by the USB host.

**Table 148: Circuit configurations**

| Config no. | Supply configuration | | Features that can be enabled for each configuration example | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| *Config. 1* | USB (VDDH = VBUS) | N/A | Yes | No | No | Yes | No |
| *Config. 2* | Battery/Ext. regulator | N/A | Yes | No | No | Yes | No |
| *Config. 3* | N/A | Battery/Ext. regulator | No | No | No | Yes | No |
| *Config. 4* | Battery/Ext. regulator | N/A | Yes | Yes | Yes | Yes | No |
| *Config. 5* | N/A | Battery/Ext. regulator | No | No | Yes | Yes | Yes |
| *Config. 6* | N/A | Battery/Ext. regulator | No | No | No | No | No |

## 56.1 Circuit configuration no. 1

**Table 149: Configuration summary for circuit configuration no. 1**

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 1 | USB (VDDH = VBUS) | N/A | Yes | No | No | Yes | No |

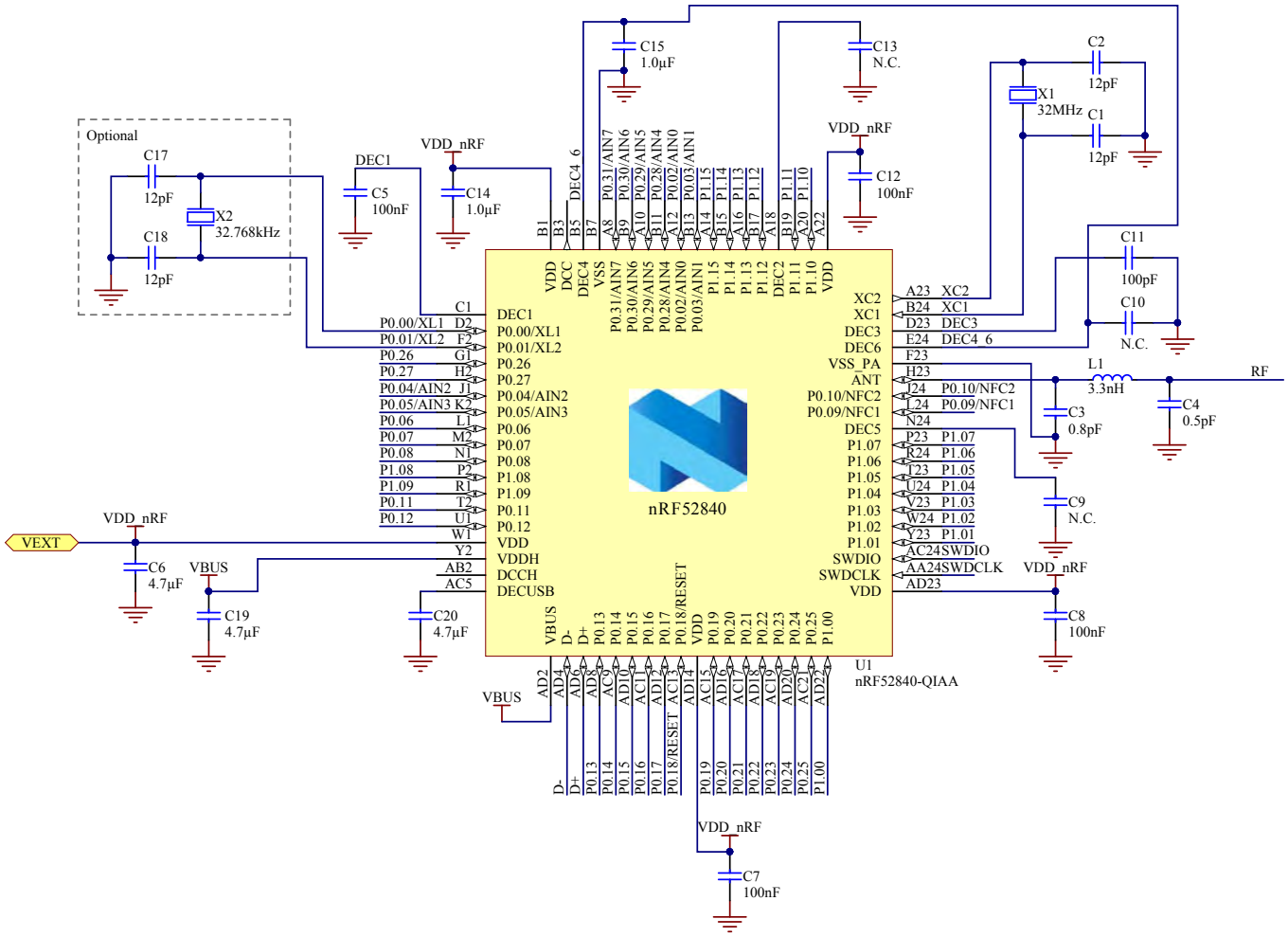



**Figure 214: Circuit configuration no. 1 schematic**

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

**Table 150: Bill of material for circuit configuration no. 1**

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C6, C20 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| C19 | 4.7 µF | Capacitor, X7S, ±10% | 0603 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.2 Circuit configuration no. 2

**Table 151: Configuration summary for circuit configuration no. 2**

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 2 | Battery/Ext. regulator | N/A | Yes | No | No | Yes | No |

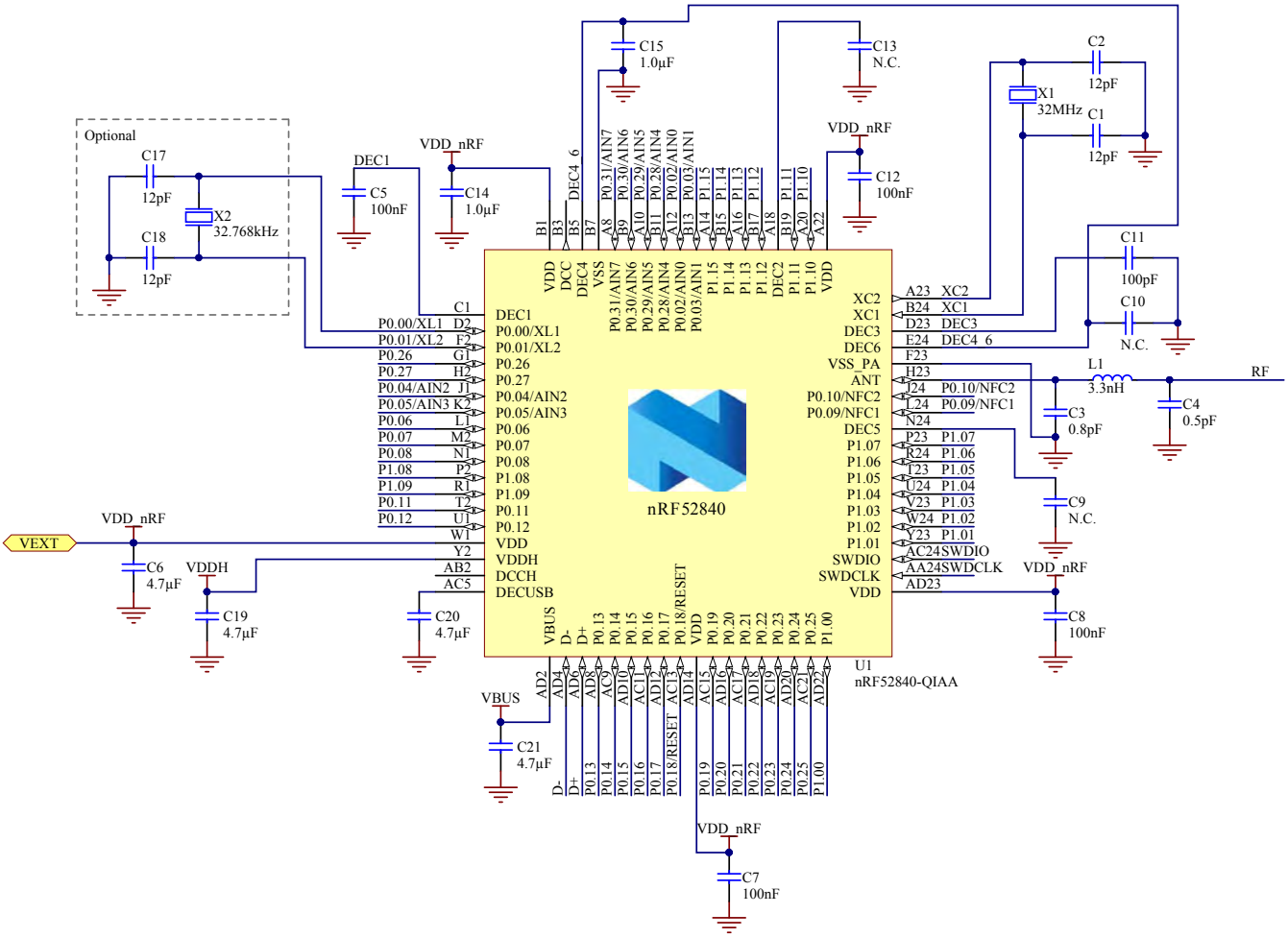



**Figure 215: Circuit configuration no. 2 schematic**

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

**Table 152: Bill of material for circuit configuration no. 2**

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C6, C20 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| C19, C21 | 4.7 µF | Capacitor, X7S, ±10% | 0603 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.3 Circuit configuration no. 3

**Table 153: Configuration summary for circuit configuration no. 3**

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 3 | N/A | Battery/Ext. regulator | No | No | No | Yes | No |

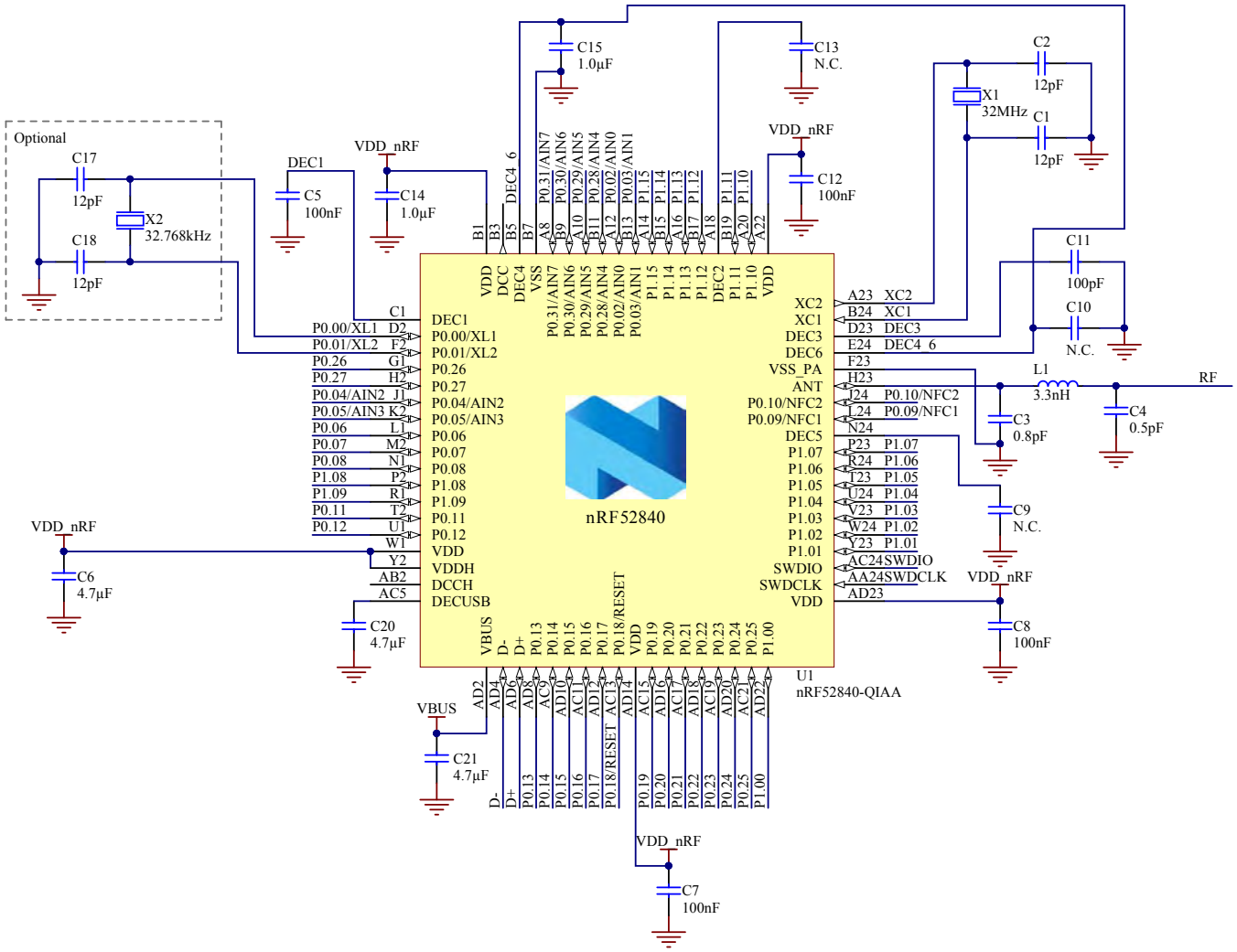



**Figure 216: Circuit configuration no. 3 schematic**

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

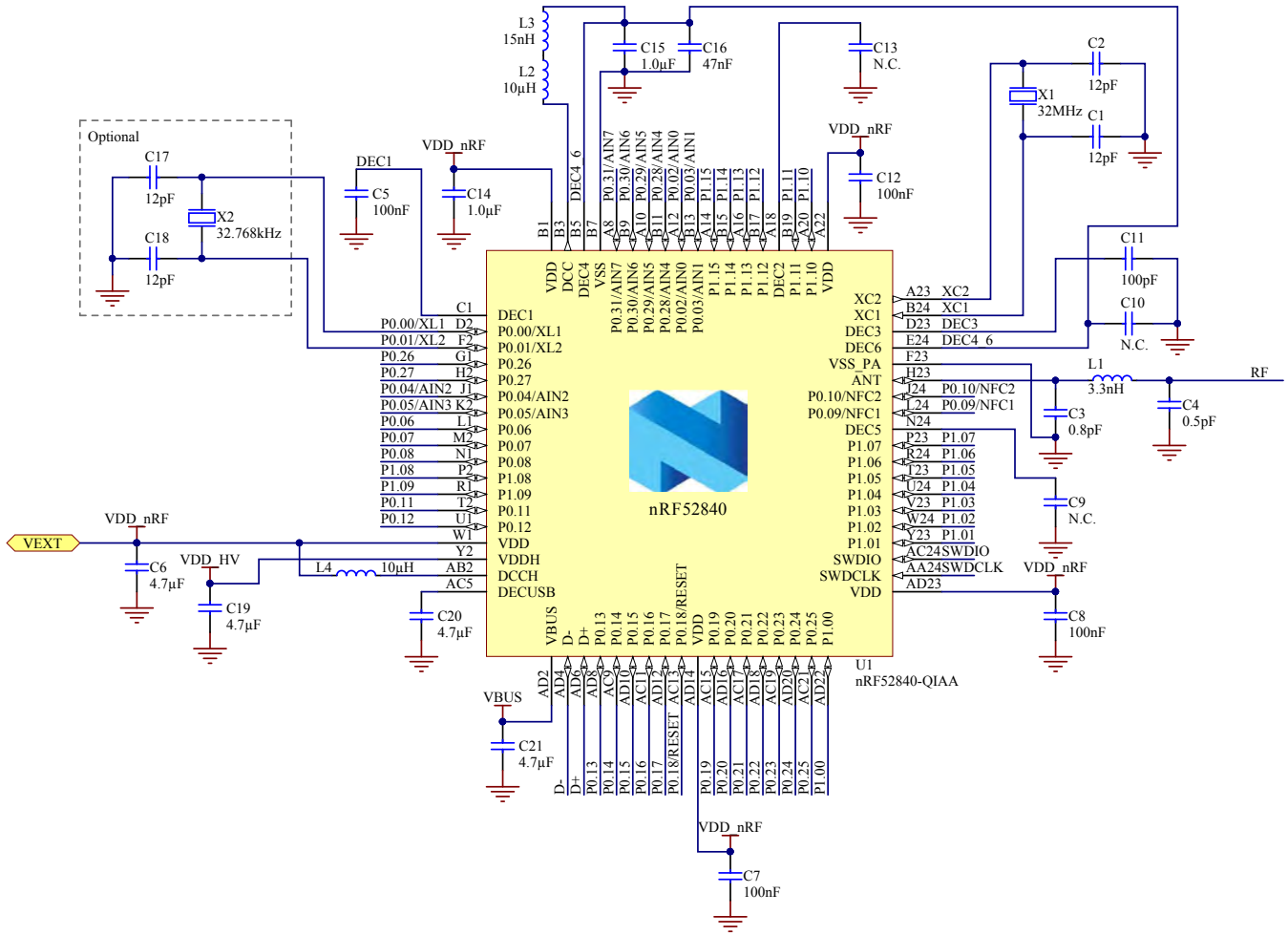
**Table 154: Bill of material for circuit configuration no. 3**

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C6, C20 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| C21 | 4.7 µF | Capacitor, X7S, ±10% | 0603 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.4 Circuit configuration no. 4

### Table 155: Configuration summary for circuit configuration no. 4

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 4 | Battery/Ext. regulator | N/A | Yes | Yes | Yes | Yes | No |




### Figure 217: Circuit configuration no. 4 schematic

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

### Table 156: Bill of material for circuit configuration no. 4

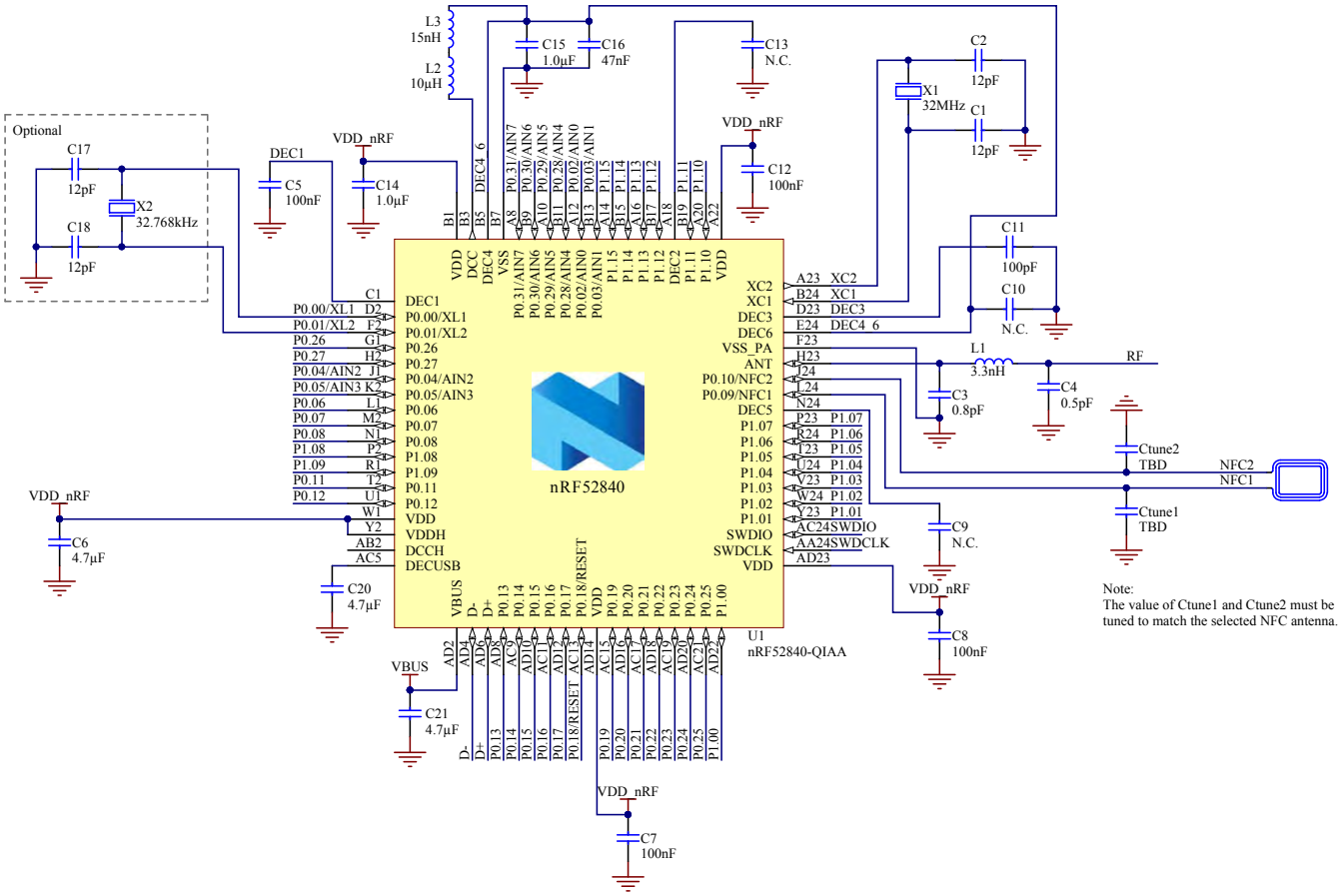
| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C6, C20 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| C16 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C19, C21 | 4.7 µF | Capacitor, X7S, ±10% | 0603 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 µH | Chip inductor, IDC min = 50 mA, ±20% | 0603 |
| L3 | 15 nH | High frequency chip inductor ±10% | 0402 |
| L4 | 10 µH | Chip inductor, IDC min = 80 mA, ±10% | 0603 |

| Designator | Value | Description | Footprint |
|---|---|---|---|
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.5 Circuit configuration no. 5

### Table 157: Configuration summary for circuit configuration no. 5

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 5 | N/A | Battery/Ext. regulator | No | No | Yes | Yes | Yes |




### Figure 218: Circuit configuration no. 5 schematic

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

### Table 158: Bill of material for circuit configuration no. 5

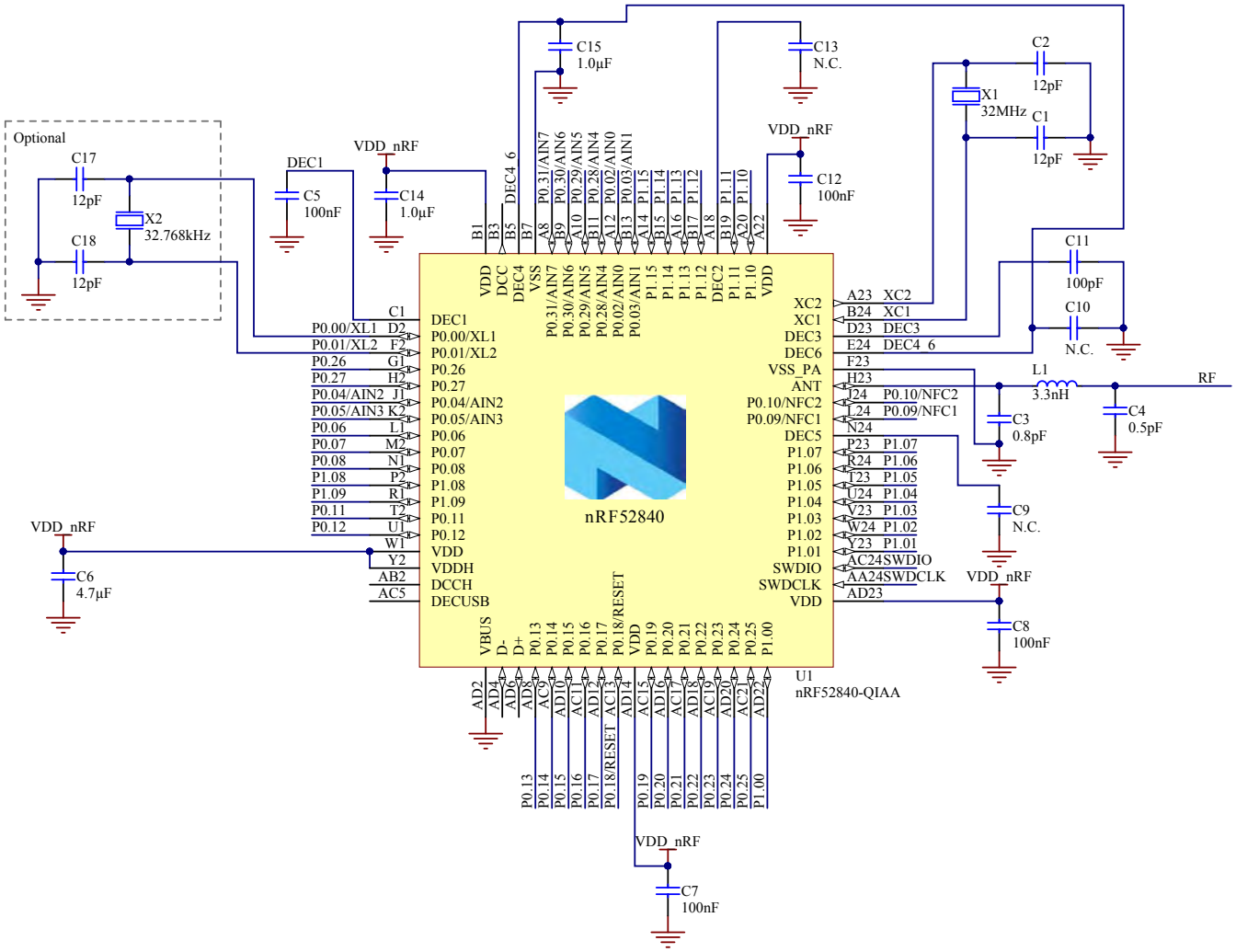
| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C6, C20 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| C16 | 47 nF | Capacitor, X7S, ±10% | 0402 |
| C21 | 4.7 µF | Capacitor, X7S, ±10% | 0603 |
| $C_{tune1}$, $C_{tune2}$ | TBD | Capacitor, NP0, ±5% | 0402 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |

| Designator | Value | Description | Footprint |
|---|---|---|---|
| L2 | 10 µH | Chip inductor, IDC min = 50 mA, ±20% | 0603 |
| L3 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.6 Circuit configuration no. 6

### Table 159: Configuration summary for circuit configuration no. 6

| Config no. | Supply configuration | | Enabled features | | | | |
|---|---|---|---|---|---|---|---|
| | VDDH | VDD | EXTSUPPLY | DCDCEN0 | DCDCEN1 | USB | NFC |
| Config. 6 | N/A | Battery/Ext. regulator | No | No | No | No | No |




### Figure 219: Circuit configuration no. 6 schematic

**Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

### Table 160: Bill of material for circuit configuration no. 6

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C17, C18 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 0.8 pF | Capacitor, NP0, ±5% | 0402 |
| C4 | 0.5 pF | Capacitor, NP0, ±10% | 0402 |
| C5, C7, C8, C12 | 100 nF | Capacitor, X7R, ±10% | 0402 |

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C6 | 4.7 µF | Capacitor, X7R, ±10% | 0603 |
| C9, C10, C13 | N.C. | Not mounted | 0402 |
| C11 | 100 pF | Capacitor, NP0, ±5% | 0402 |
| C14, C15 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L1 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF52840-QIAA | Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip | AQFN-73 |
| X1 | 32 MHz | Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm | XTAL_2016 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm | XTAL_3215 |

## 56.7 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *www.nordicsemi.com*.

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single-ended antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal RF performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended AQFN73 package reference circuitry from *Circuit configuration no. 1* on page 688.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

## 56.8 PCB layout example

The PCB layout shown below is a reference layout for the AQFN package with internal LDO setup and VBUS supply.

> **Important:** Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS_PA pin F23. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the Reference Layout section on the Downloads tab for nRF52840 on *www.nordicsemi.com*.

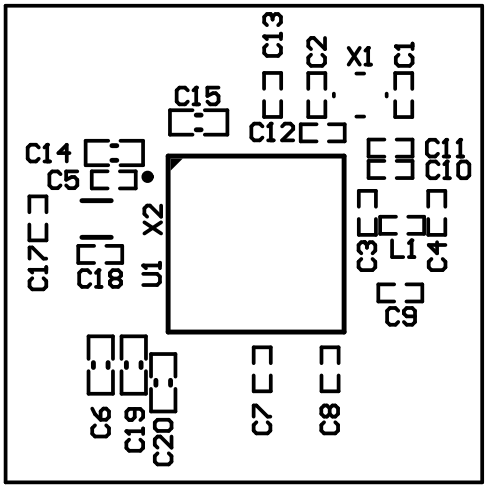



**Figure 220: Top silk layer**

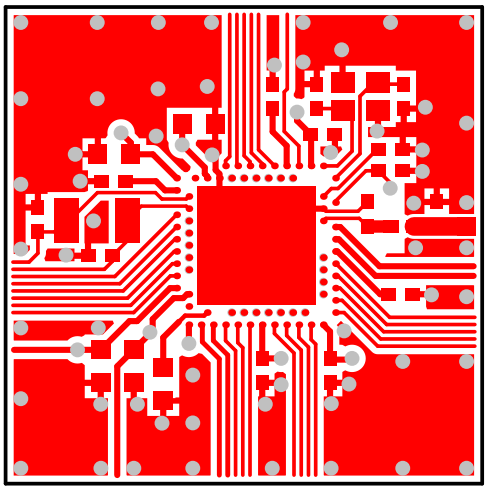


**Figure 221: Top layer**

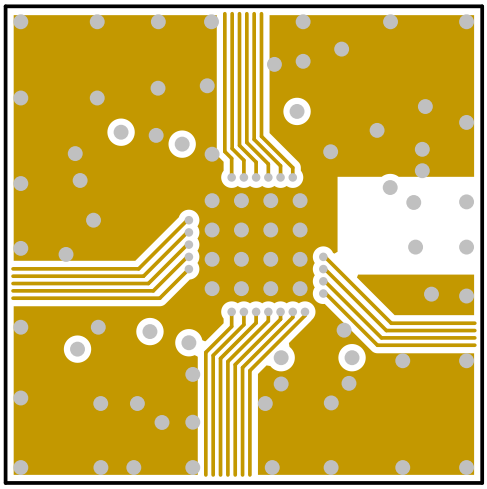


**Figure 222: Mid layer 1**

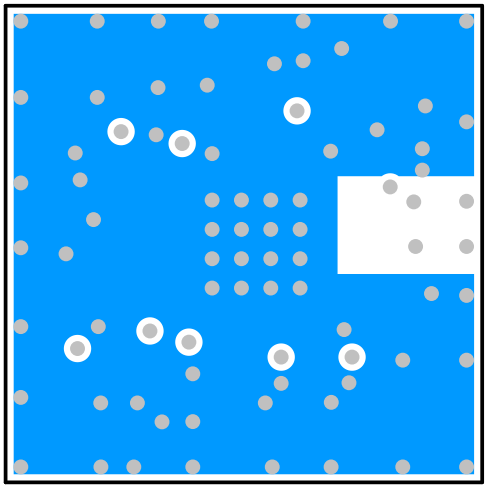


**Figure 223: Mid layer 2**

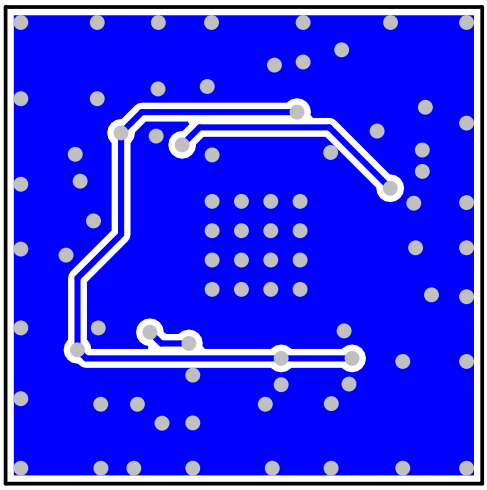


**Figure 224: Bottom layer**

**Important:** No components in bottom layer.

# 57 Liability disclaimer

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein.

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Nordic Semiconductor products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS) and the requirements of the REACH regulation (EC 1907/2006) on Registration, Evaluation, Authorization and Restriction of Chemicals.

The SVHC (Substances of Very High Concern) candidate list is continually being updated. Complete hazardous substance reports, material composition reports and latest version of Nordic's REACH statement can be found on our website .

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