

# WXQ65NFC Hardware Design Guide

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Application note  
COMPANY PUBLIC

## Document information

Info	Content
<b>Keywords</b>	WXQ65NFC, Hardware Design, Power modes, Chip interfaces
<b>Abstract</b>	<p>This document is intended to provide an overview on how to integrate the NFC Controller WXQ65NFC from hardware perspective.</p> <p>It presents the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation.</p> <p>In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption.</p>



## Revision history

Rev	Date	Description
1.3	20200710	Tuning impedance recommendation aligned to AN11755
1.2	20180115	Adding information related to WLCSP42 package Editorial changes
1.1	20160523	Security status changed into "COMPANY PUBLIC"
1.0	20151204	First official version of the document

## Contact information

For additional information, please visit: <http://www.nxp.com>

## 1. Introduction

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The WXQ65NFC is a full feature NFC Controller designed for integration in devices compliant with NFC Forum standards.

It is designed based on learning from previous NXP NFC device generation to ease the integration of the NFC technology in electronic devices by providing:

- A low PCB footprint and a reduced external Bill of Material by enabling as unique feature the capability to achieve RF standards with small form factor antenna
- An optimized architecture for low power consumption in different modes (standby, low power polling loop)
- An highly efficient integrated power management unit allowing direct supply from a battery while a constant output power (operating distance in Poll mode) for extended battery supply range (2.75 to 5.5V) can be achieved.

It embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, MIFARE and FeliCa specifications. This new contactless front-end design brings a major performance step-up with a higher sensitivity.

Detailed chip features set can be found in the [WXQ65NFC Product Datasheet \[1\]](#).

This application note is intended to give an overview of the way the WXQ65NFC must be integrated into a hardware platform. It presents in particular the different hardware design options offered by the WXQ65NFC and it provides guidelines on how to select the most appropriate ones for a given implementation.

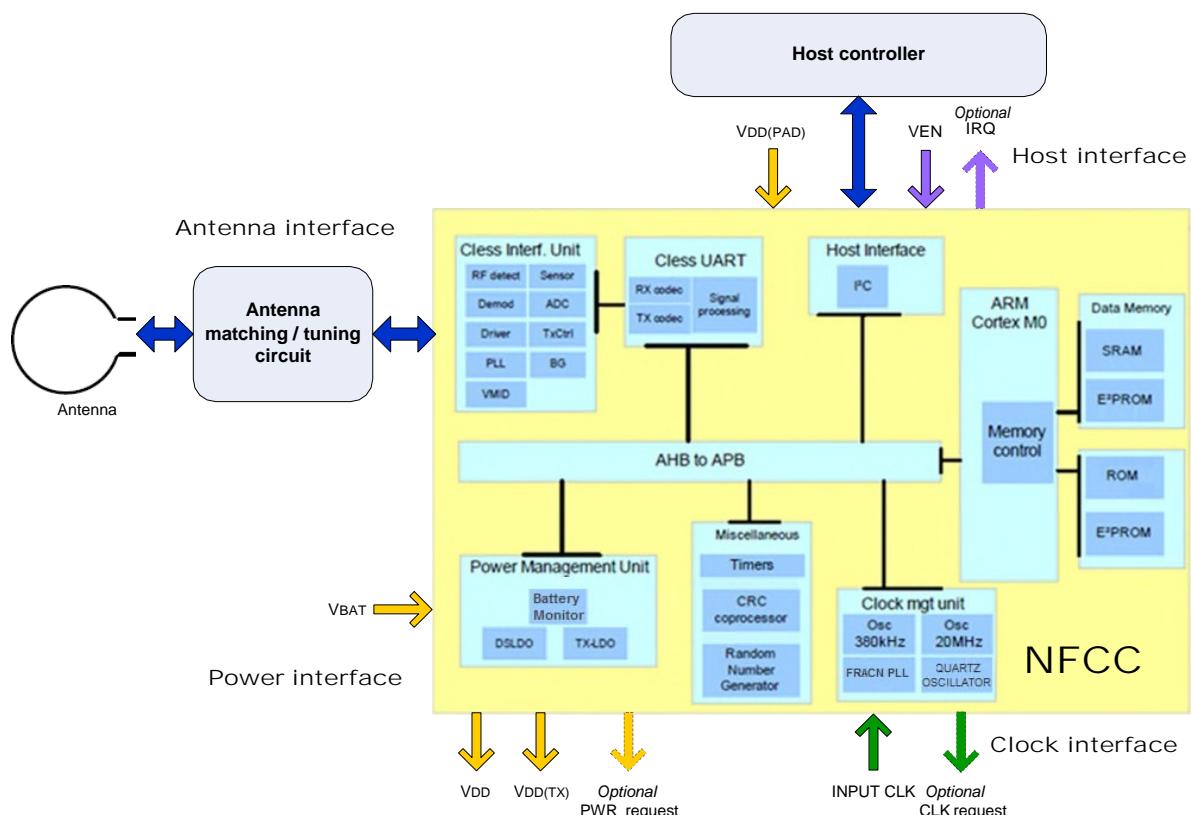
An overview of the different chip interfaces is first shown. Then detailed information related to each interface is depicted and the related configurations are presented.

## 2. Interfaces

The purpose of this chapter is to give an overview of the WXQ65NFC interfaces and to show how the chip is interconnected to the external world.

WXQ65NFC external connections are shown in *Fig 1*.

Then, WXQ65NFC interfaces are listed in *Table 1* and the different configuration options are mentioned.



**Fig 1. Interfaces summary**

The WXQ65NFC provides the following interfaces:

- Host interface
- Clock interface
- Power interface
- Antenna interface

**Table 1. Interface summary**

Interface	Short description	Options
Host interface	Link with host controller	<ul style="list-style-type: none"><li>• I<sup>2</sup>C address configuration</li><li>• IRQ or polling</li><li>• Reset control</li></ul>
Clock interface	Input clock required when generating RF field	<ul style="list-style-type: none"><li>• Input clock characteristics</li><li>• CLK request mechanism</li></ul>
Power interface	Interface to power management unit (direct battery supply supported)	<ul style="list-style-type: none"><li>• Power management concept</li><li>• Decoupling capacitors</li></ul>
Antenna interface	Link to an NFC antenna in order to enable communication with a remote contactless device	<ul style="list-style-type: none"><li>• Antenna selection</li><li>• Antenna matching</li></ul>

### 3. Typical application schematics

The purpose of this chapter is to propose an application schematic for WXQ65NFC.

The below depicted configuration is based on the following implementation choices:

- The use of a crystal as input clock source (see 5.1)
- The use of a standard antenna (see 7.1)
- The use of VBAT to generate TVDD (see 6.4.1)

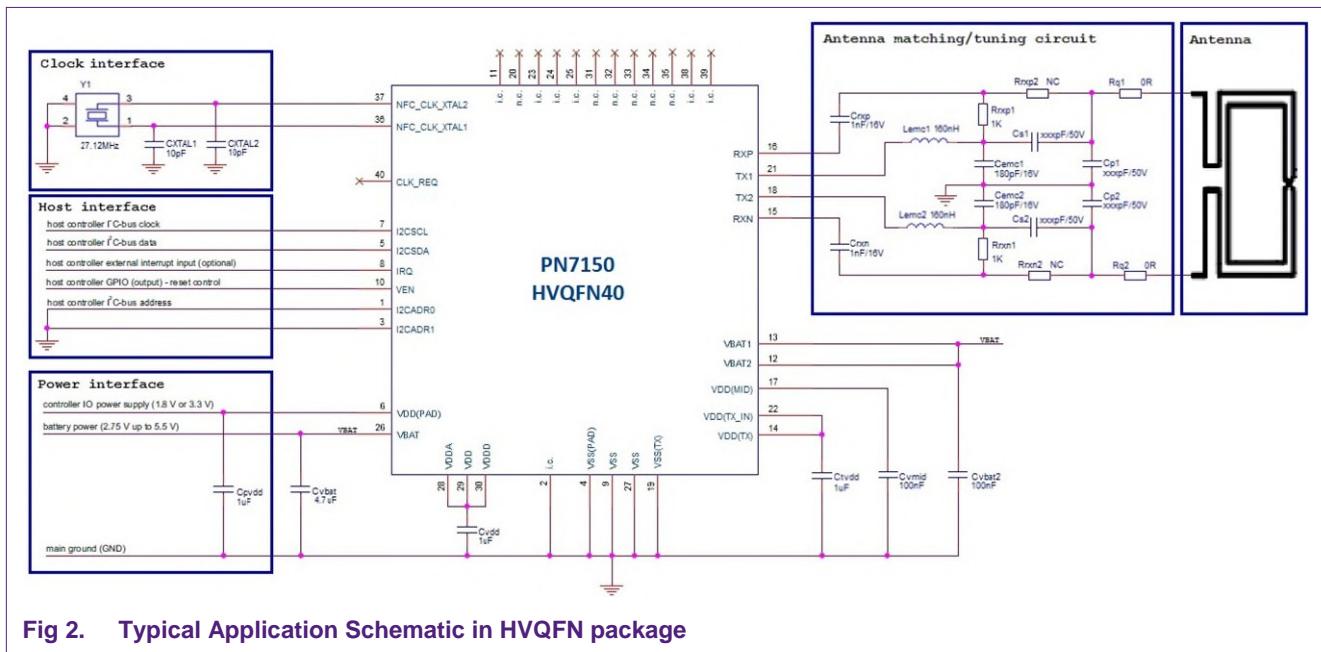


Fig 2. Typical Application Schematic in HVQFN package

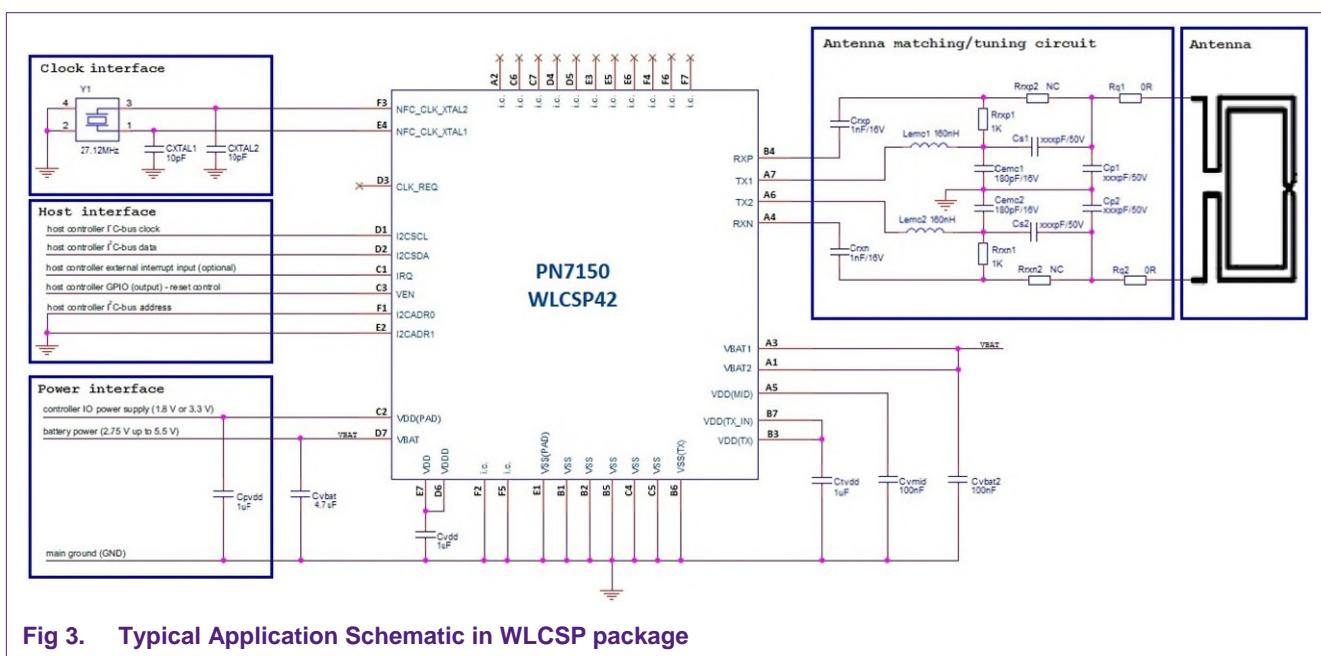


Fig 3. Typical Application Schematic in WLCSP package

## 4. Host interface

### 4.1 Host interface pinning

Table 2. Host interface pinning

HVQFN pin	WLCSP pin	Symbol	Description
#1	F1	I2CADR0	I2C-bus ADDRess bit 0 input
#3	E2	I2CADR1	I2C-bus ADDRess bit 1 input
#5	D2	I2CSDA	I2C-bus Serial DAta
#7	D1	I2CSCL	I2C-bus Serial Clock Line
#8	C1	IRQ	Interrupt ReQuest output
#10	C3	VEN	V ENable input. Set the device in Hard Power Down

### 4.2 Host interface pin characteristics

Detailed characteristics of the host interface pins can be found in the [WXQ65NFC Product datasheet \[1\]](#).

### 4.3 Digital interface levels

The host controller interface power supply must be connected to the WXQ65NFC on the VDD(PAD) pin. Both 1.8V and 3V supply levels are supported.

Thus, multiple digital levels between the host controller and the WXQ65NFC can be supported without the need for level shifters.

For details on the VDD(PAD) range, please refer to the [WXQ65NFC Product Datasheet \[1\]](#).

### 4.4 I<sup>2</sup>C bus specificities

#### Slave address:

In the case where I<sup>2</sup>C is the selected host interface, the chip will answer to a given I<sup>2</sup>C slave address.

This is determined by the combination of a base address and the logical state of I2CADR0 and I2CADR1 pins: b' 0 1 0 1 0 I2CADR1 I2CADR0' where I2CADR0 and I2CADR1 are the least significant bits. For instance, if both I2CADR0 and I2CADR1 are tied to ground, the 7-bits slave address of the WXQ65NFC is "0x28" (gives 0x50 as 8-bits write address).

Table 3. I<sup>2</sup>C slave 8-bits address

I2CADR0 Level	I2CADR1 Level	I <sup>2</sup> C write address (R/W bit = 0)	I <sup>2</sup> C read address (R/W bit = 1)
0 (GND)	0 (GND)	0x50	0x51
1 (VDD(PAD))	0 (GND)	0x52	0x53
0 (GND)	1 (VDD(PAD))	0x54	0x55
1 (VDD(PAD))	1 (VDD(PAD))	0x56	0x57

### Pull-up selection:

Pull-up resistors to VDD(PAD) are required on the I<sup>2</sup>C lines SDA and SCL. The resistors value must be selected to meet the I<sup>2</sup>C timing requirements based on the line capacitance, the VDD(PAD) level and the targeted maximum I<sup>2</sup>C clock speed. More details can be found in the [I<sup>2</sup>C bus specification \[3\]](#) document.

## 4.5 Frames reading synchronization

WXQ65NFC answers / notifications toward the host controller are asynchronous and they can be triggered by an external event (e.g. detection of a card in the RF field).

Therefore, a mechanism must be put in place so that asynchronous frames from the WXQ65NFC are well captured by the host controller. For this, 3 implementations can be foreseen on the host controller side:

- 1- IRQ pin external interrupt
- 2- IRQ pin polling
- 3- Read polling

For 1-, connect pin IRQ of the WXQ65NFC to an external interrupt line on the host controller side. In this case, when the WXQ65NFC has some data available, the IRQ line will be asserted and if configured accordingly, a software interrupt is generated on the host controller side. An I<sup>2</sup>C read is then managed by the corresponding interrupt handler.

For 2-, the principle is to regularly poll the status of the IRQ pin and when it toggles, to perform a read on the I<sup>2</sup>C interface.

For 3-, the principle is to regularly perform some read on the I<sup>2</sup>C interface and to discard frames starting with the default value as in this case it would mean that no data is available from the WXQ65NFC. The I<sup>2</sup>C address will not be acknowledged in case the WXQ65NFC doesn't have any meaningful data to send to the host.

Implementation -1 is recommended.

### IRQ Signal Specification:

- The signal can be configured active high or active low via the NCI Configuration API. This configuration is stored in non-volatile memory. Details can be found in the [WXQ65NFC User Manual \[2\]](#).
- The signal will be active any time data is available in the WXQ65NFC send buffer
- The pad state is maintained during the standby mode
- The pad is configured in pull down in hard power down mode

## 4.6 Reset control (VEN)

The WXQ65NFC HW is activated using the input pin VEN.

When VEN is greater than 1.1V the WXQ65NFC core is supplied from VBAT.

For VEN lower than 0.4V the WXQ65NFC is in hard power down state and the chip's internal core is no more supplied.

The chip is reset when VEN is switched back to a voltage level higher than 1.1V.

It is strongly recommended to foresee a control of VEN pin from the host controller side so that it can reset WXQ65NFC whenever needed.

The VEN pad state is considered as valid information only when the VDD(PAD) pad is supplied.

Indeed, VEN signal is supposed to be driven by the host controller with which VDD(PAD) supply is shared. When the supply is not there, this means that the host controller is not able to drive a meaningful state on the WXQ65NFC VEN pin.

An internal pull-down resistor can be programmed on the WXQ65NFC internal VEN signal in order to define a clear pin state when it is not externally driven by the host (details can be found in [WXQ65NFC User Manual \[2\]](#)). It means that when the device is powered-up with VBAT and VDD(PAD) supplied to the WXQ65NFC, the NFC chip will stand in hard power down until the host controller explicitly drives the VEN pin to the digital high state (during its boot sequence).

The full WXQ65NFC power states, considering VBAT, VDD(PAD) and VEN pin level, is given in [WXQ65NFC Product datasheet \[1\]](#).

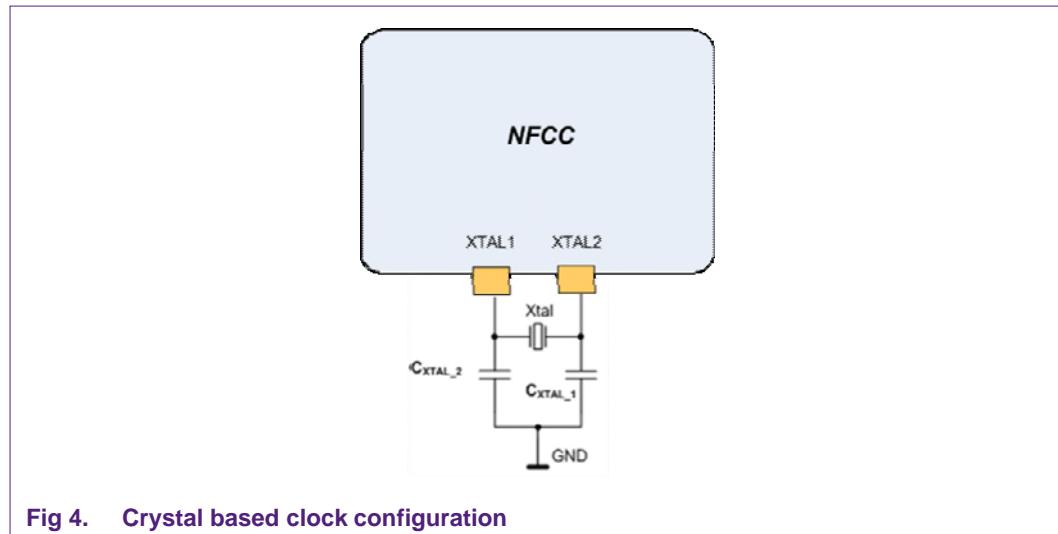
## 5. Clock interface

The core microcontroller of the WXQ65NFC chip can run without any external clock (based on an internal oscillator). However, the 13.56MHz RF field carrier accuracy requirements are not compatible with the use of an internal oscillator. As a consequence, the WXQ65NFC needs either to have an external clock supplied to its XTAL1 pin or to be connected to a crystal oscillator before starting to emit an RF field.

The WXQ65NFC clock interface must be configured properly to reflect whether it is connected to a crystal oscillator or to an external clock (in this case, the frequency must also be configured). This is done through the NCI host interface. Details can be found in [WXQ65NFC User Manual \[2\]](#).

### 5.1 Use of crystal oscillator

A 27.12MHz crystal can be used as input clock for WXQ65NFC. For instance, when there is no clock on the system complying with the WXQ65NFC input clock specification. When using a crystal, frequency accuracy and drive level must be carefully selected according to the specification provided in the [WXQ65NFC Product Datasheet \[1\]](#).



Crystal interface has been verified with several references as given below. Other crystal units might be suitable for the specified usage, but only the ones below have been properly checked by NXP.

- NDK:
  - o NX2016AA 27.12MHz EXS00A-03778 (discontinued)
  - o NX2016SA 27.12MHz EXS00A-CS06346
  - o NX2016HA 27.12MHz EXS00A-CH00075
- MURATA:
  - o XRCGB27M120F3M10R0

## 5.2 Use of system clock

### 5.2.1 Input clock characteristics

When an external system clock is used, the input clock frequency must be one of the following values: 13MHz, 19.2MHz, 24MHz, 26MHz, 38.4MHz or 52MHz

Please note that the voltage level of the system clock signal provided to WXQ65NFC must be 1.8V.

The system clock used with the WXQ65NFC chip must fulfill the phase noise requirement described in the datasheet.

The WXQ65NFC input impedance on the XTAL1 pin depends on the input clock frequency:

At 13MHz, it is between 25Kohms and 86Kohms in active mode and between 49Kohms and 53Kohms in standby or Hard Power Down mode.

At 52MHz, it is between 5Kohms and 7.5Kohms in active mode and between 12Kohms and 14Kohms in standby or Hard Power Down mode.

Based on this input clock signal, the WXQ65NFC internal PLL generates the required 27.12MHz internal clock for field generation.

Detailed system clock characteristics can be found in the [WXQ65NFC Product Datasheet \[1\]](#).

### 5.2.2 Clock request mechanism

In order to optimize the device power consumption, the input clock could be provided by the system only when it is actually needed by the chip (i.e. when the NFCC needs to generate an RF field). For this, a clock request mechanism has been put in place.

When the WXQ65NFC needs an input clock, it toggles the CLK\_REQ pin to the digital high level and keeps it high as long as the input clock is required. It requires a specific connection of the CLK\_REQ pin which would switch-on the system clock signal whenever the pin is at the digital high level and switch it off when the pin is set back to the digital low level.

This feature is enabled according to WXQ65NFC EEPROM configuration (see details in the [WXQ65NFC User Manual \[2\]](#)).

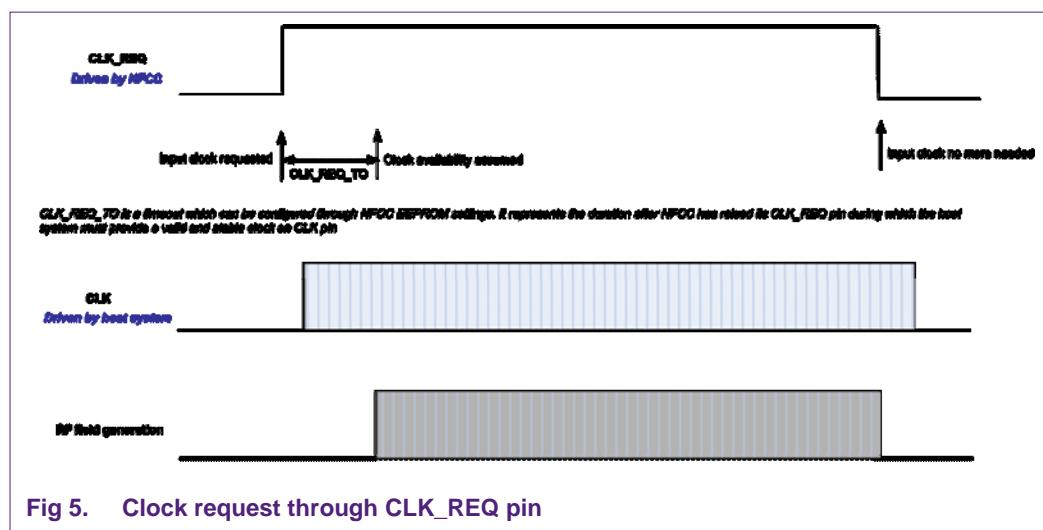
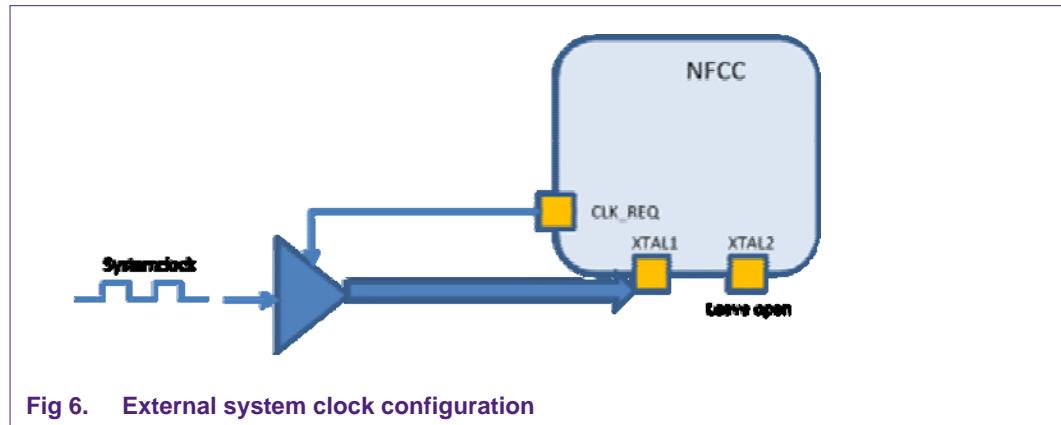


Fig 5. Clock request through CLK\_REQ pin

**Warning:** XTAL1 pin is referenced to VDD(PAD) supply. Therefore VDD(PAD) must always be supplied to the WXQ65NFC when a valid input clock signal is required (i.e. to generate an RF field)

The dedicated clock request pin (CLK\_REQ) can be optionally connected to a clock buffer. CLK\_REQ pin is driven high when the NFCC needs an input clock. Otherwise it is driven low.



## 6. Power interface

### 6.1 Power Management Unit

The WXQ65NFC supports to be directly connected to a battery power supply. It can operate with a wide voltage input range from 5.5V down to 2.75V.

Detailed current consumption versus the different power mode and min/typical/max voltage information can be found in the [WXQ65NFC Product Datasheet \[1\]](#).

### 6.2 External capacitors requirement

The recommended external capacitors (value and voltage it must at least withstand) are listed below:

Table 4. Decoupling capacitors need

	Values	Comments
$C_{VDD}$	1 $\mu$ F/2V	
$C_{VDD(PAD)}$	1 $\mu$ F/2V or 3.3V	Depending on host power supply decoupling needs
$C_{TVDD}$	1 $\mu$ F/3.6V	
$C_{VBAT}$	4.7 $\mu$ F/5.5V	
$C_{VBAT2}$	100nF/5V	
$C_{VMID}$	100nF/1.8V	

A tolerance of 10% or better is recommended for those capacitors. Component de-rating over voltage and temperature must be carefully considered during the decoupling capacitors selection process.

### 6.3 Power application schematic

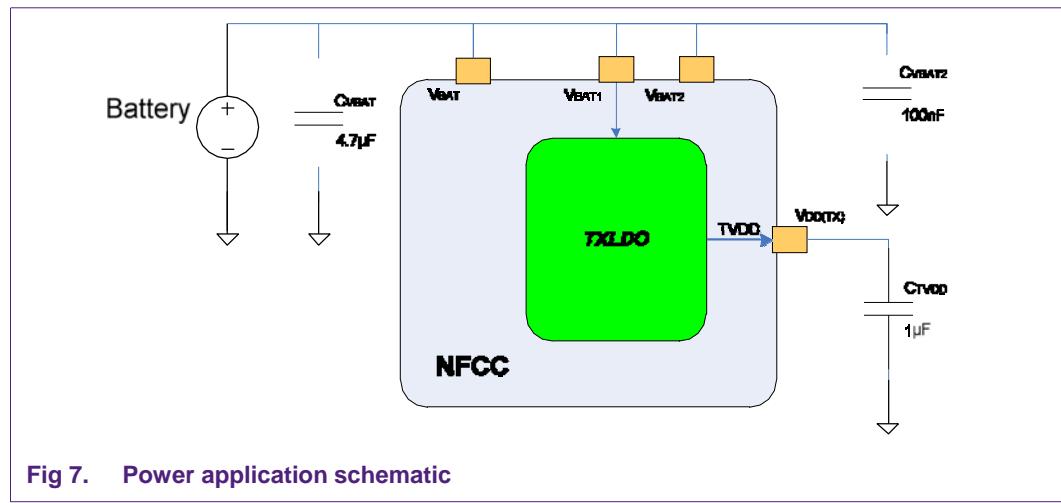


Fig 7. Power application schematic

## 6.4 TVDD supply options

The strength of the field emitted by the WXQ65NFC is linked to several parameters such as the antenna geometrical characteristics, the antenna matching circuit and the voltage level on TX output buffer.

The voltage level on TX output buffer is coming from TVDD. Typical TVDD influence on RF reading distance is depicted on the below picture:

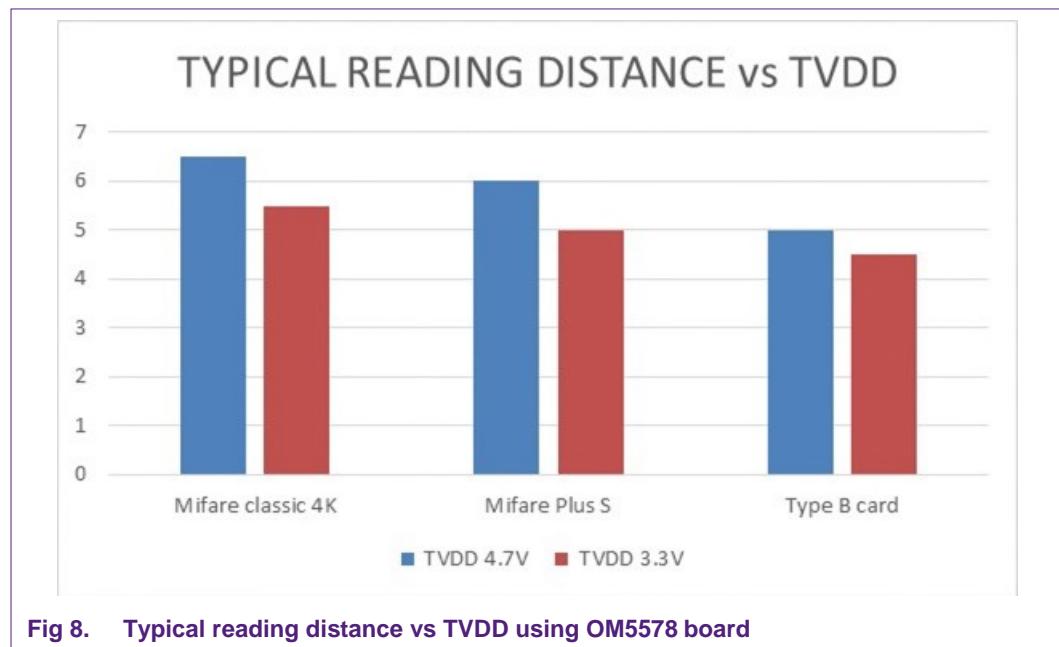


Fig 8. Typical reading distance vs TVDD using OM5578 board

TVDD can be regulated by the TXLDO which will be powered internally by the WXQ65NFC. The voltages choice will depend on the configuration used.

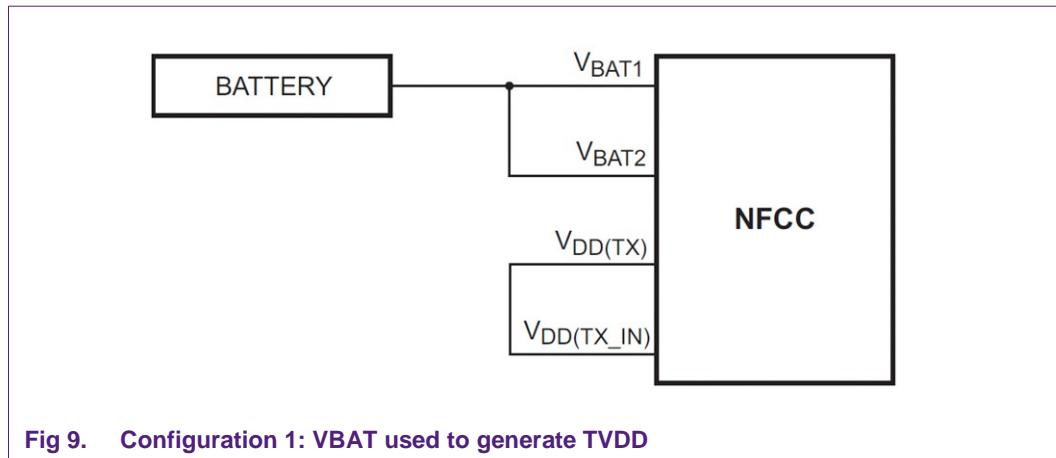
**Please note that if the product has already been certified, changing one RF parameter like TVDD setting must lead to a full re-certification.**

The programming of the TVDD configuration is described in [WXQ65NFC User Manual \[2\]](#).

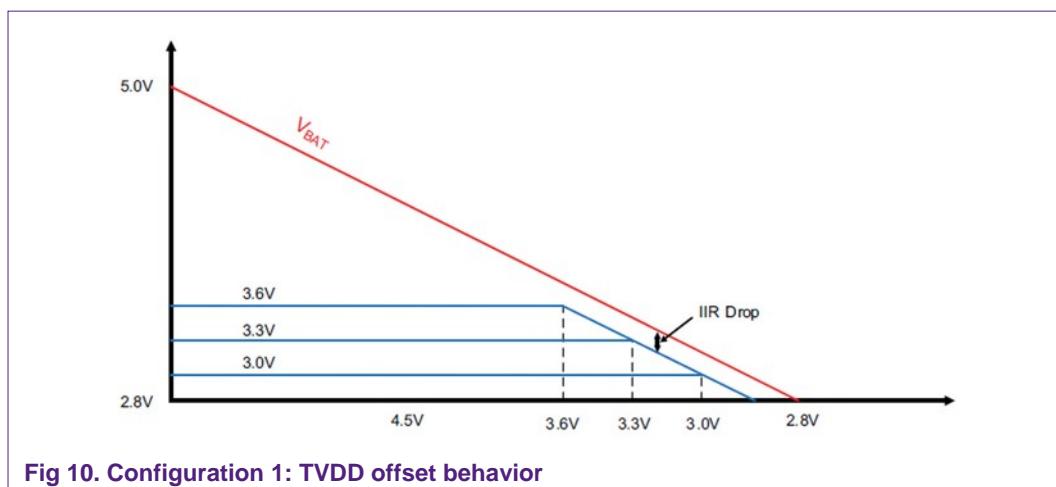
### 6.4.1 Config 1: VBAT used to generate TVDD

The Low drop Out Regulator has been designed to generate a 3.0 V, 3.3 V or 3.6 V supply voltage to a transmitter with a current load up to 180 mA.

The input supply voltage of this regulator is a battery voltage connected to VBAT1 pin.



TVDD value shall be chosen according the minimum targeted VBAT value for which reader mode shall work.



For example, if chosen TVDD is 3.6V and current to be delivered by the TxLDO is  $Itx$ , it means:

$$\begin{aligned} &\text{if } VBAT \geq (3.6V + 1\Omega * Itx) \text{ then } TVDD = 3.6V \\ &\text{if } 2.3V \leq VBAT \leq 3.6V \text{ then } TVDD = VBAT - 1\Omega * Itx \end{aligned}$$

As the maximum current allowed is 180mA, a margin of 180mV between the VBAT and the chosen TVDD value is needed to work on the regulated area of the LDO.

**In Standby state, whenever TVDD is configured for 3V, 3.3V or 3.6V, TVDD is regulated @2.5V**

**Table 5. Configuration 1 summary**

	Reader mode	Card mode	Standby mode
TVDD available voltage	3/3.3/3.6	3/3.3/3.6	2.5

#### 6.4.2 Config 2: external 5V used to generate TVDD

In this case the TXLDO can provide a TVDD of 3V/3.3V/3.6V/4.5V or 4.75V.

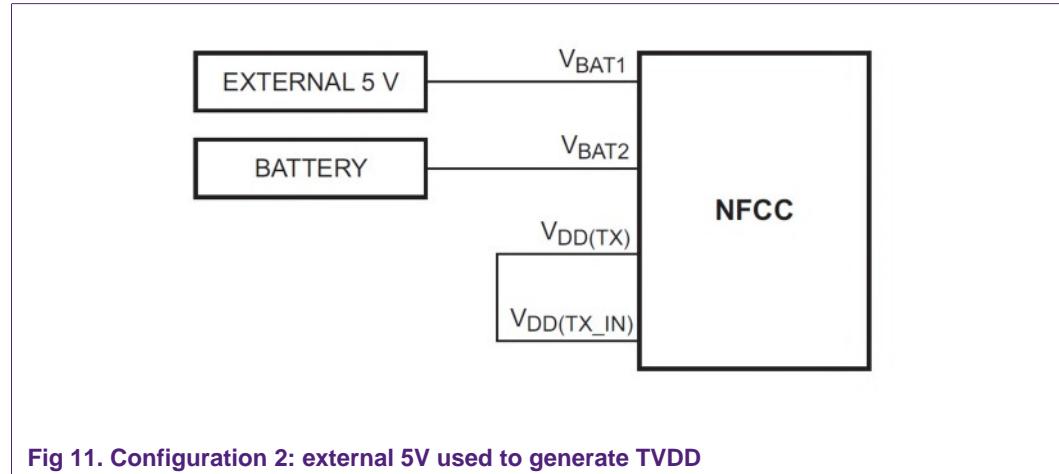


Fig 11. Configuration 2: external 5V used to generate TVDD

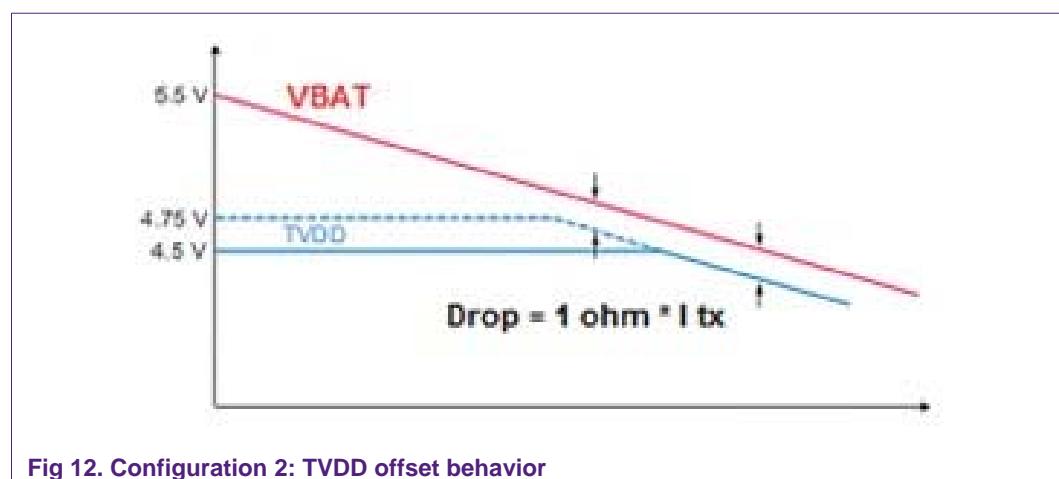


Fig 12. Configuration 2: TVDD offset behavior

Depending on the wanted behaviour of the external 5V in card mode, 2 different programming are available.

Table 6. Configuration 2 summary

	Reader mode	Card mode	Standby mode
TVDD available voltage	3/3.3/3.6/4.5/4.75	3/3.3/3.6/4.5/4.75	2.5

#### 6.4.3 TVDD configuration summary

Table 7. Available TVDD value for each configuration

	Reader mode	Card mode	Standby mode
Config 1	3/3.3/3.6/4.5/4.75	3/3.3/3.6	2.5
Config 2	3/3.3/3.6/4.5/4.75	3/3.3/3.6/4.5/4.75	2.5

Table 8. Pros and cons for each TVDD configuration

	Pros	Cons
<b>Configuration 1</b>	- No external 5V supply	- No performances improvement thanks to higher VDD(TX) voltage
<b>Configuration 2</b>	- Maximize the performances in reader mode and card mode - Use the internal TXLDO to filter the 5V power supply	- Higher power consumption compare to configuration 1

WXQ65NFC can operate at fixed RF field strength in Poll mode with a continuous battery voltage down to:

- 3.1V when TVDD is set to 2.7V
- 3.5V when TVDD is set to 3.1V

The figure below shows 2 typical battery discharge cycles.

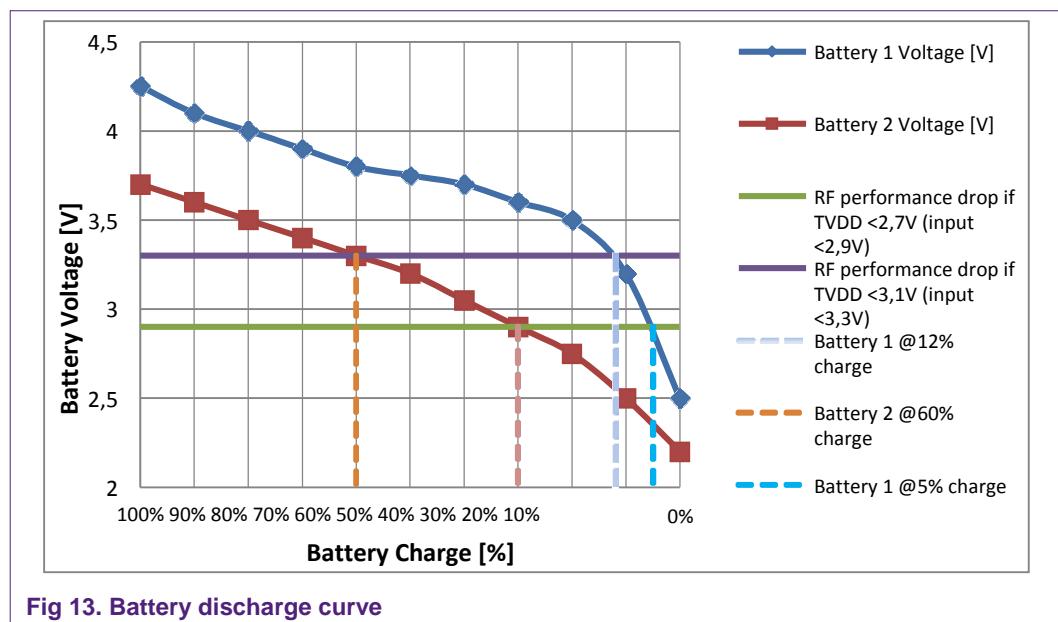


Fig 13. Battery discharge curve

## 7. Antenna interface

### 7.1 Typical matching circuit

The WXQ65NFC is intended to be connected to an antenna through a matching circuit. The typical topology for this circuit is depicted below:

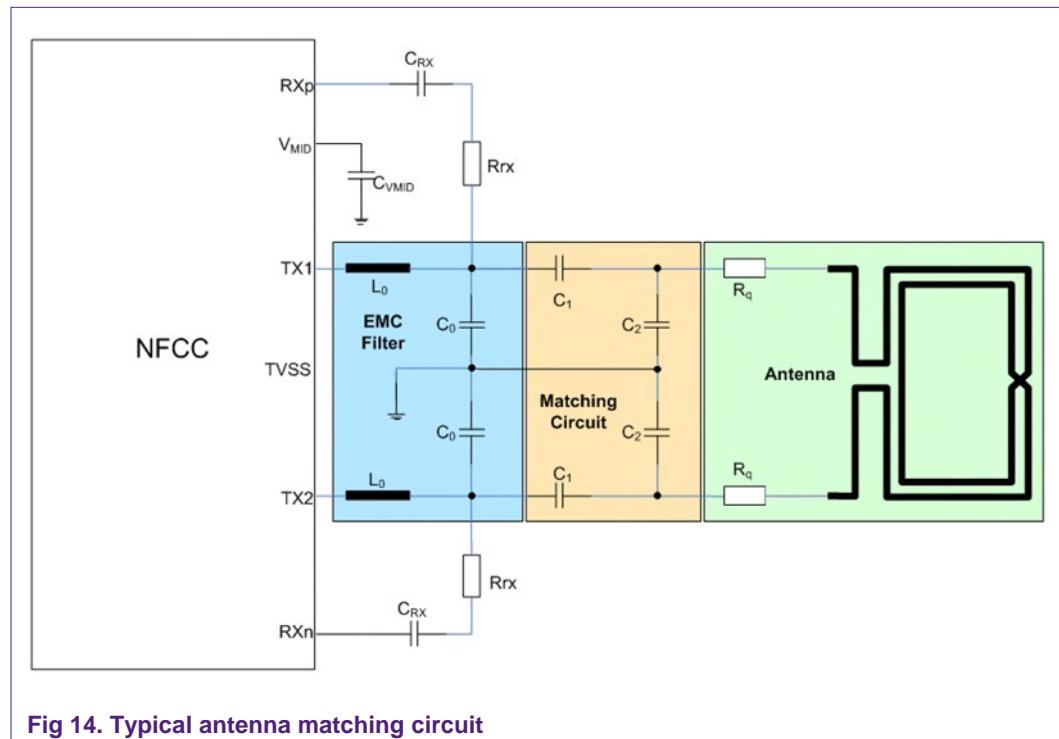


Fig 14. Typical antenna matching circuit

The components values are antenna dependent.

$L_0 / C_0$  are a 2<sup>nd</sup> order low pass filter used to reduce the spectrum power amplitude in the high frequency range but without altering the meaningful communication signal.

$C_1 / C_2$  are used to tune the Poll mode and Listen mode frequency at 13.56MHz and to adapt the equivalent impedance presented on TX1/TX2 at this frequency (30 ohms recommended).

$R_q$  is optionally used to reduce the qualify factor of the antenna when it is above 35 (if it is already below, which is rather common in embedded equipment environment with ferrite shielding,  $R_q$  must not be placed)

How to select or design a proper antenna for the WXQ65NFC and how to calculate the value of the matching components is explained in a dedicated application note. Please refer to the [WXQ65NFC Antenna Design and Matching Guide \[4\]](#).

### 7.2 Matching circuit BoM optimization

Based on careful technical consideration, the number of matching circuit components presented on the above schematics can be lowered.

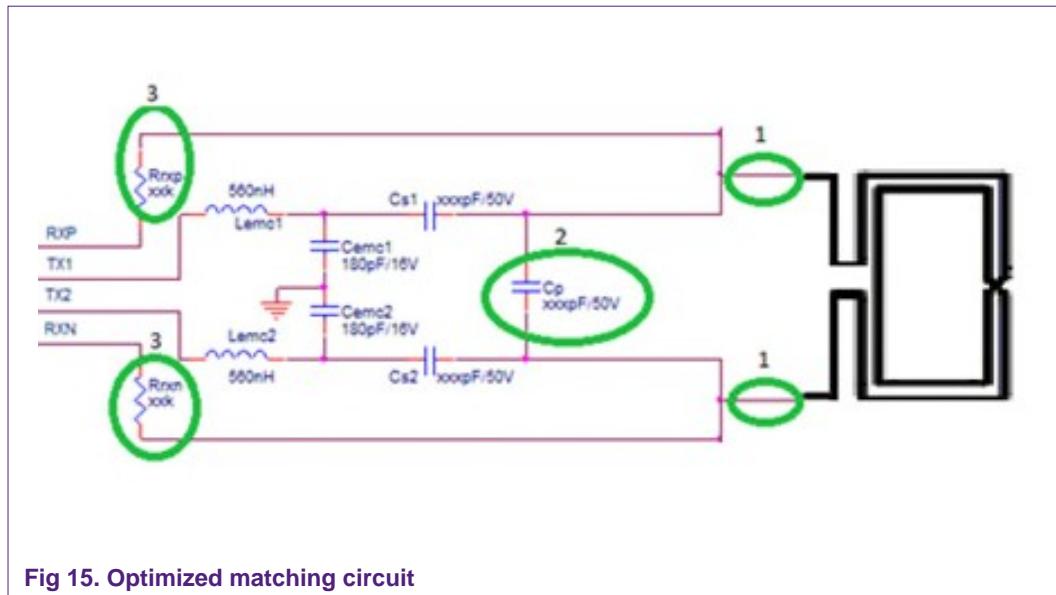


Fig 15. Optimized matching circuit

### 7.2.1 Damping resistors

$R_q$  damping resistors are used to lower the antenna quality factor when it is above 35. Indeed, a too high quality factor will negatively impact the generated signal shaping.

However, in an embedded environment, the presence of metal (battery, PCB tracks, electronic components...) tends to significantly reduce the antenna quality factor.

Therefore, although they can be needed on an open-air board environment, it is very unlikely that these 2 resistors are required for embedded equipment integration.

**Proof point:**

Once the customer has measured its NFC antenna within its final environment he should calculate the resulting quality factor as explained in the [WXQ65NFC Antenna Design Guide \[4\]](#). If the quality factor is below or equal to 35,  $R_q$  resistors can be safely removed.

See circles 1 in above Fig 15.

### 7.2.2 $C_2$ parallel capacitor

Two serial capacitors are used in parallel with the antenna to tune it to 13.56MHz.

The reason to have 2 capacitors in parallel is that the peak to peak voltage at antenna ends can reach more than 50V depending on the antenna geometrical characteristics (size, number of turns...)

However, if for a given antenna, the maximum peak to peak voltage measured at antenna ends is lower, then a single parallel capacitor on  $C_p$  can eventually be used.

Its value needs then to be divided by 2 compared to the ones used in case of 2 serial capacitors solution.

**Proof point:**

As the voltage generated at antenna ends for a given external field power will be strongly linked to the antenna environment, this measurement must be performed within the final product.

It must be placed on an ISO/IEC10373-6 PCD assembly test bench and the maximum external field strength that an ISO/IEC14443 compliant device must withstand (12A/m) must be generated.

Then, the peak to peak voltage at antenna end must be measured with an oscilloscope using a low parasitic capacitor probe (2pF max).

Depending on the value measured, the customer can decide whether a single 50V parallel capacitor is suitable

See circle 2 in above Fig 15.

### 7.2.3 Rx path

In case a small antenna is connected to the WXQ65NFC, the peak to peak voltage generated at antenna ends will be limited.

Then this offers the possibility to simplify the RF path circuitry by removing the decoupling  $C_{rx}$  caps and connecting directly the  $R_{rx}$  to the antenna ends (see drawing below)

#### Proof point:

The measurements needed to decide whether or not, the  $C_{rx}$  capacitors can be safely removed for a given configuration are still under definition.

See circles 3 in above Fig 15.

## 8. Power modes

- Hard Power Down (HPD)
- Full Power
- Standby

A simplified figure is depicted below to provide an overview of the different WXQ65NFC power modes, with VEN and VBAT as input parameters. The complete diagram including VDD(PAD) is given in [WXQ65NFC Product Datasheet \[1\]](#).

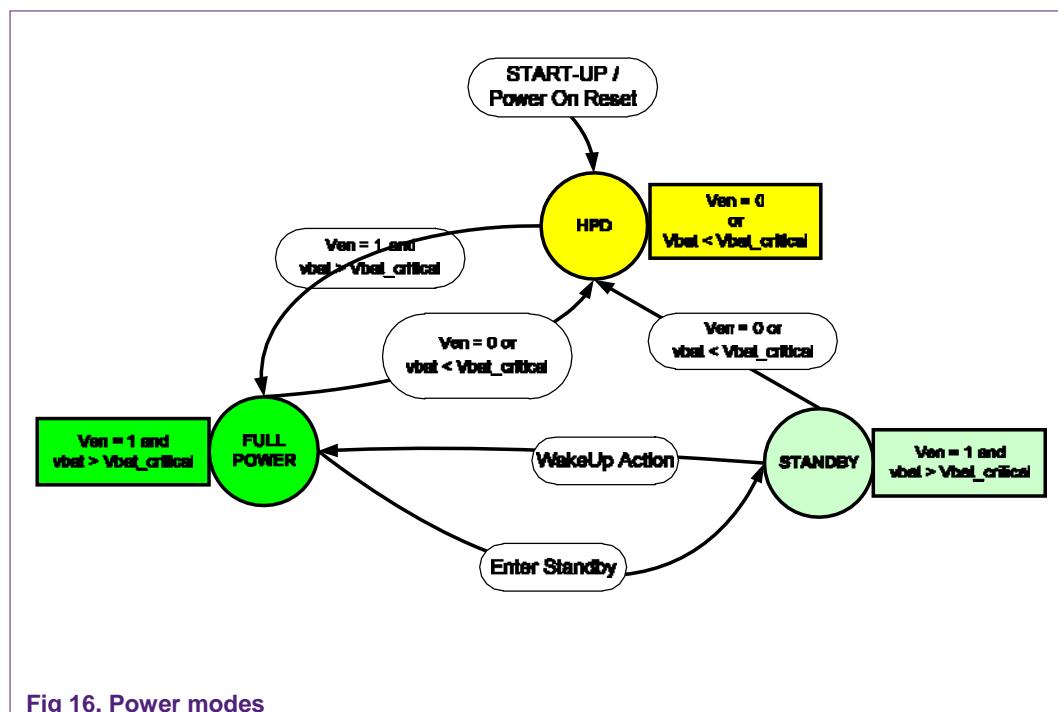


Fig 16. Power modes

When VEN is low or when the battery voltage is below its critical level the IC goes in Hard Power-Down mode.

When VEN is high and sufficient battery power is available, the chip is in full power mode. It can then switch to Stand-by mode if this mode has been enabled (Software configuration) and no activity has occurred on the host interface during a configurable duration.

The WXQ65NFC resumes from stand-by to full power mode when an external or internal event occur (e.g. host interface communication, external field entry, internal discovery loop...)

## 9. Layout guidelines

### 9.1 Antenna EMC inductors

The selection of the EMC inductors is key for best performance. There are several parameters to consider when selecting a reference, as described below:

- High-Q factor ( $> 20$  @ 13.56MHz) is preferred. Its dependencies are:
  - o Size (e.g. 603)
  - o Inductance value (e.g. 160nH)
- AC Current Characteristics (depending on  $\mu$  saturation vs. H value)
  - o The flat test inductance variation vs. AC current increase ( $I_{p-p}$ ) is preferred.
  - o Still, the inductance might be rather flat until a certain amount of  $I_{p-p}$  current (e.g. 100mA), which can be good enough for an application
- Coupling effect
  - o The lowest coupling factor vs. distance between coils is preferred

Suppliers generally provide two types of technology, Wire-wound and Multi-layer inductors. The following table summarizes the benefits of each technology. One shall select the best compromise vs. all parameters.

Table 9. Inductance characteristics

	Q-Factor	AC current $\mu$ saturation	Coupling
<b>Wire-wound</b>			
<b>Multi-layer</b>			

To minimize the coupling effect, there can be several inductance placements as depicted in the below *Fig 19*:

- Parallel
  - o When the field lines are parallel, they can couple each other and the system gets potentially de-tuned
- 90° or T-mount
- Symmetrical or series mounted

Please take care of the rules provided by your supplier for the optimal placement. During the matching process this might not be directly seen as an impedance analyzer typically delivers some few mW of power. During operation, the WXQ65NFC can introduce far more

than few mW which causes a very much different field distribution compared to the one captured with the impedance analyzer.

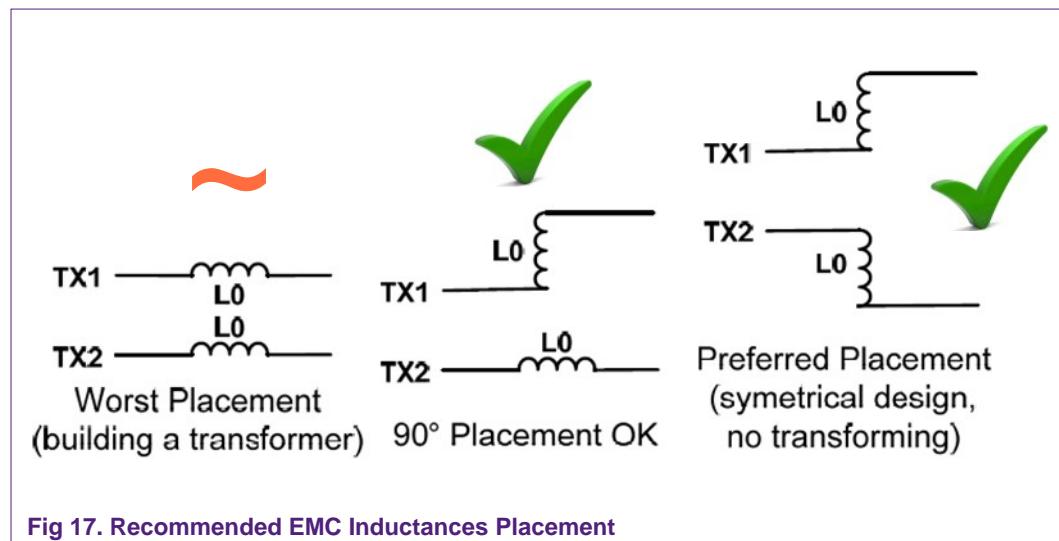


Fig 17. Recommended EMC Inductances Placement

WXQ65NFC EMC inductors have been verified with several references as given below. Other references might be suitable, but only the ones below have been properly checked by NXP.

- TDK
  - o MLF series: e.g. MLF1608
- MURATA
  - o Multi-layer parts: LQB18 series
  - o Wire-wound parts: LQW18 series

## 9.2 RF paths

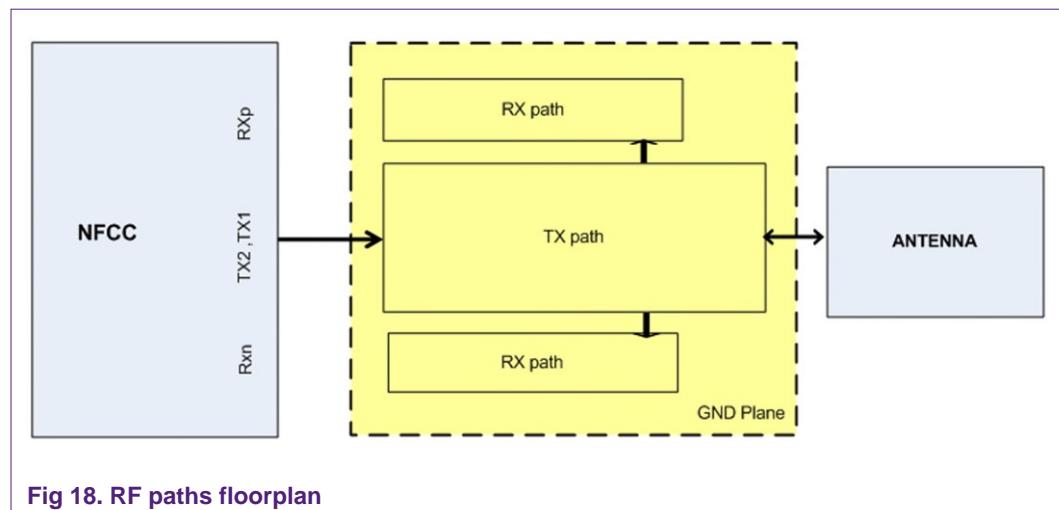
All the signals are quite sensitive to noise hence some ground plane shall be applied all around these paths to minimize radiation from the circuit towards other system components and vice versa.

RF paths must be kept away from clock lines.

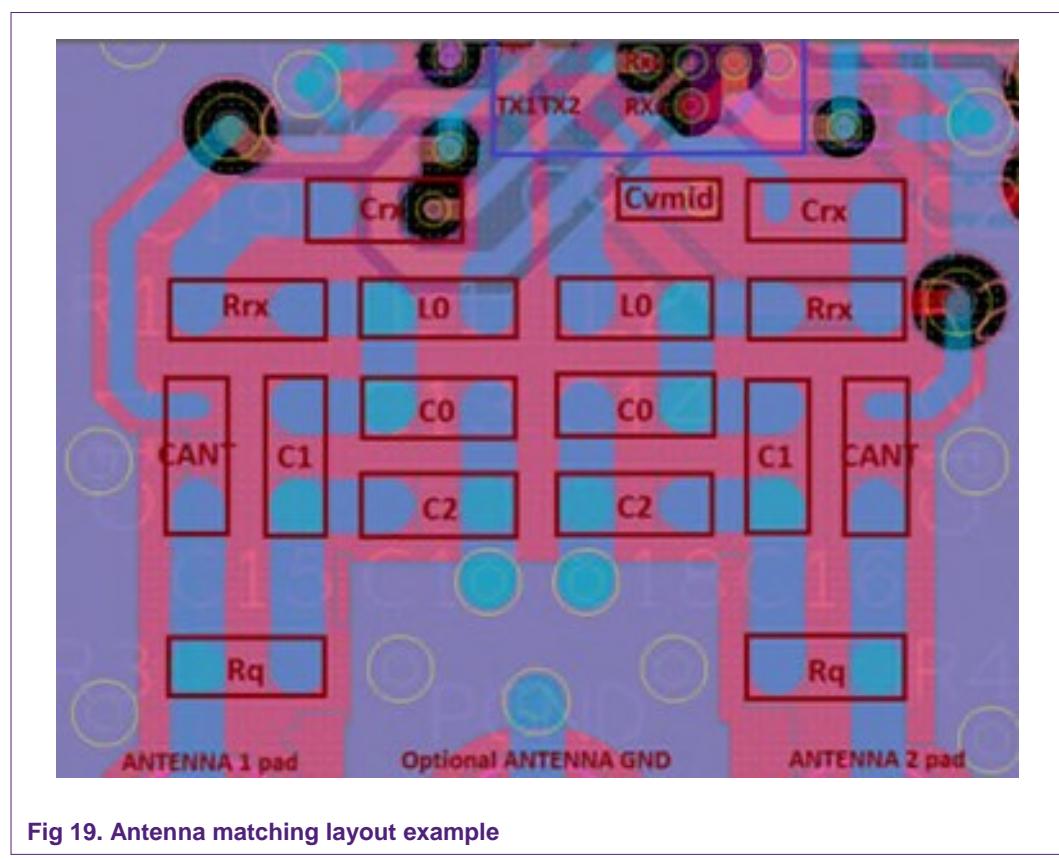
Track length must be minimized and a symmetrical routing must be used wherever possible.

Line crossing must be avoided as it would imply some voltage/current induction between the different paths.

A possible top-level implementation of the Antenna matching circuit is shown below:



The WXQ65NFC reference design layout depicted below can be used as an example of proper antenna components routing.



Please note that you shall take care of having multiple vias to connect different ground layers to avoid too resistive bottleneck, especially on the TX path grounding.

### 9.3 XTAL layout recommendations

The XTAL must be connected as close as possible to the CLK1 and CLK2 pins from the WXQ65NFC to achieve the best performances as possible.

Please follow these guidelines for the layout of the XTAL connections:

- As the XTAL is very sensitive to parasitic capacitance and noise, we advise to:
  - o put the XTAL far from other signals (especially other CLK lines or signals with frequent switching)
  - o limit the crosstalk between CLK lines and other signals
- Load capacitor connections:
  - o Choose capacitor with a good temperature stability like COG
  - o Place the capacitors closed to each other and close to the XTAL
  - o Avoid to connect them to a dirty ground (perturbed by return current from others functionalities on the board like USB, PWM or power supply lines)

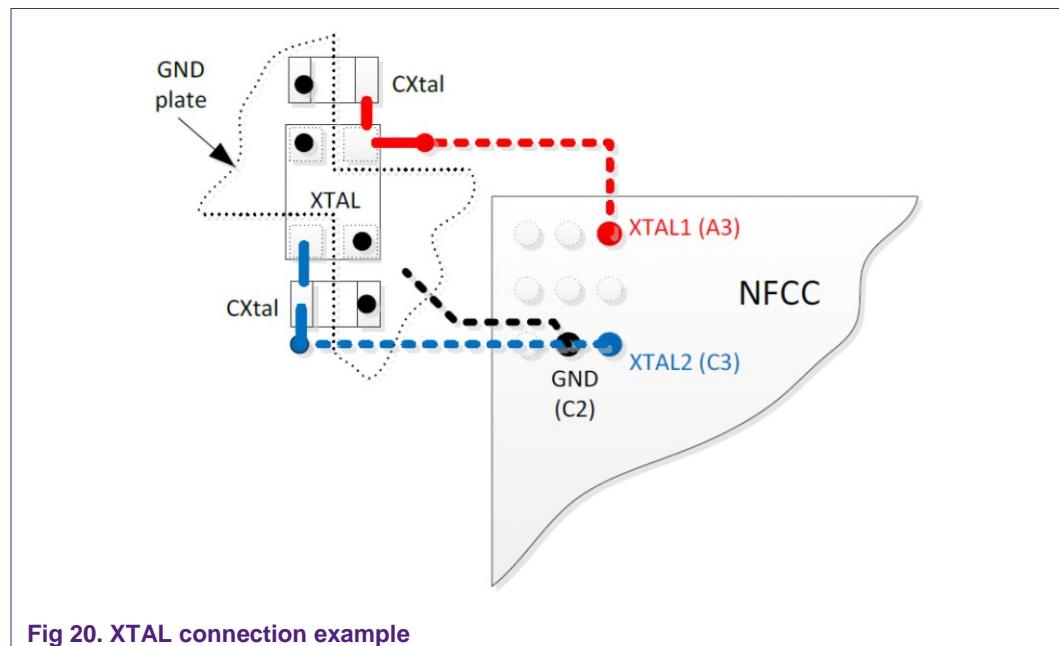


Fig 20. XTAL connection example

### 9.4 Input clock

Clock signal must be:

- Shielded from the rest of the board
- Kept as short as possible

### 9.5 De-Coupling (blocking) capacitors

Standard layout rules consisting in decoupling capacitors being placed as close as possible to the chip apply.

## 10. Q&A

---

- **How to optimize the NFC controller power consumption when the host controller is shutdown or enters stand-by mode?**

The WXQ65NFC can be configured to enter standby mode when there is no activity from the host controller side after a programmable timeout (see configuration details in the [\*WXQ65NFC User Manual \[2\]\*](#)).

Standby mode can be activated by setting the proper EEPROM configuration and it is retained (so only need to be activated once if not disabled afterwards).

- **When using the WXQ65NFC, is it mandatory to connect VBAT2 to VBAT?**

Yes, it is mandatory.

## 11. References

---

- [1] WXQ65NFC Product Datasheet
- [2] UM10936 – WXQ65NFC User Manual
- [3] I<sup>2</sup>C Bus Specification
- [4] AN11755 – WXQ65NFC Antenna Design and Matching Guide

## 12. Abbreviations

Abbr.	Meaning
AN	Application Note
BoM	Bill of material
CLK	Clock
EEPROM	Electrically Erasable Programmable Read Only Memory
GND	Ground
GPIO	General Purpose Input Output
HW	Hardware
I <sup>2</sup> C	Inter-Integrated Circuit (serial data bus)
IC	Integrated Circuit
IO	Input / Output
IRQ	Interrupt Request
ISO/IEC	International Standard Organization / International Electrotechnical Community
mA	milli Ampere
MHz	Mega Hertz
mW	milli Watt
NFC	Near Field Communication
NFCC	NFC Controller (i.e. WXQ65NFC)
OS	Operating System
PCD	Proximity Coupling Device (Contactless reader)
PICC	Proximity Integrated Circuit Card (Contactless card)
PMU	Power Management unit
RF	Radiofrequency
RST	Reset
VEN	V ENable pin (Hard reset control)

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**NOTICE:**

- ♦please keep this product and accessories attached to the places which children can't touch;
- ♦do not splash water or other liquid onto this product, otherwise it may cause damage;
- ♦do not put this product near the heat source or direct sunlight, otherwise it may cause deformation or malfunction;
- ♦please keep this product away from flammable or naked flame;
- ♦please do not repair this product by yourself. Only qualified personnel can be repaired.

**FCC Statement**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains FCC ID:2A639-WXQ65NFC" any similar wording that expresses the same meaning may be used.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

The module is limited to OEM installation ONLY.

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.

The module is limited to installation in mobile application.

A separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and difference antenna configurations.

There is requirement that the grantee provide guidance to the host manufacturer for compliance with Part 15B requirements.

The module complies with FCC Part 15.225 and apply for Single module approval.

Trace antenna designs: Not applicable.

---

## Antennas:NFC

The antenna is permanently attached, can't be replaced.

Antenna manufacturer: Heyuan City Lianteng Industrial Co. LTD

Model: WXQ-NFC-ANT-V1.1

## Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

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- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

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"Contains IC: 29997-WXQ65NFC"

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---

**Radiation Exposure Statement**

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