IEEE 802.11 1X1 a/b/g/n/ac Wireless LAN Bluetooth 5.2 Combo Stamp Module

Datasheet

Version 1.1

LS005ONWCS Datasheet

Date	Revision Content	Revised By	Version
2022/01/25	Initial Release	EE	V1.0
2022/02/24	Modify BT Specification	RF	V1.1

LS005ONWCS Datasheet

Contents

1. Introduction

Product Overview and Functional Description

The LS005ONWCS is a highly integrated Wi-Fi5 (2.4/5 GHz) and Bluetooth single-chip solution, specifically designed to support the speed, reliability, and quality requirements of next generation Very High Throughput (VHT) products.

The module provides both simultaneous and independent operation of the following:

- IEEE 802.11ac (Wave 2), 1x1 with data rates up to MCS9 (433 Mbit/s)
- Bluetooth 5.2 (includes Bluetooth Low Energy (LE))

For security, the device supports high performance 802.11i security standards through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBCMAC Protocol (CCMP), AES/Galois/Counter Mode Protocol (GCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), AES/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported . The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

The module supports multiple interfaces:

WLAN: SDIO3.0; Bluetooth: SDIO3.0, UART.

Audio interface: PCM for Bluetooth.

2. Features

2.1 Wi-Fi Features

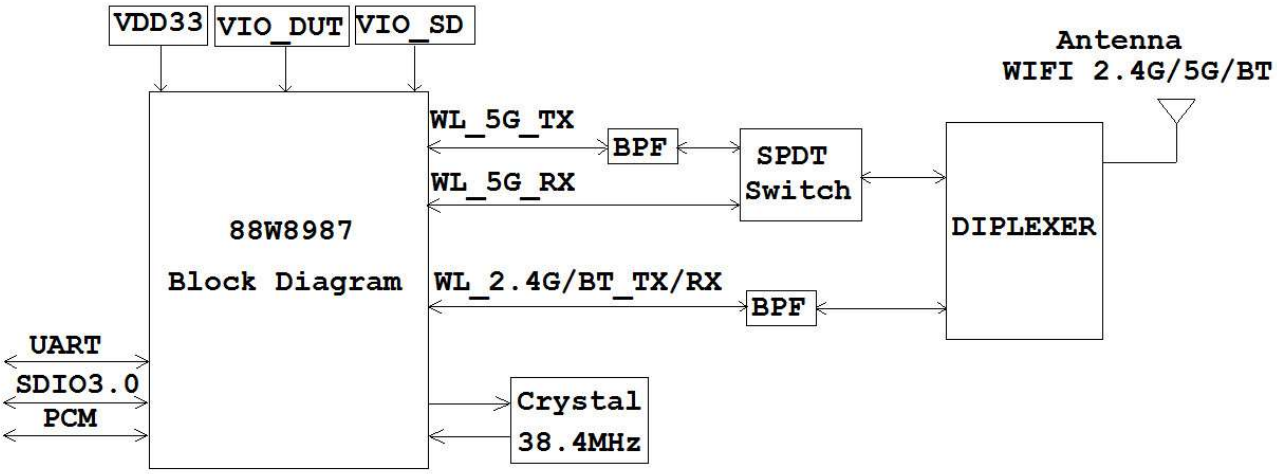
- Support 802.11 a/b/g/n/ac
- Dual band: 2.4 GHz and 5 GHz
- PHY data rates up to 433 Mbit/s
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- 80 MHz bandwidth/channel, 4 positions of 20 MHz packets in 80 MHz channel, upper/lower 40 MHz packets in 80 MHz channel, 20 MHz quadruplicate legacy packets in 80 MHz channel mode operation
- Modulation and Coding Scheme(MCS)
- -802.11ac—MCS 0~9 Nsts = 1
- -802.11n—MCS 0~7 and MCS 32 (duplicate 6 Mbit/s)
- Support 802.11mc for indoor location
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- On-chip Tx and Rx FIFO for maximum throughput
- Security: TKIP, WEP, AES, CCMP, CMAC, GCMP, WAPI

2.2 Bluetooth Features

- Full Bluetooth 5.2 features
- Bluetooth Class 2
- Bluetooth Class 1
- Baseband and radio BDR and EDR packet types—1 Mbit/s(GFSK), 2 Mbit/s(П/4-DQPSK), and 3 Mbit/s(8DPSK)
- 1 Mbit/s and 2 Mbit/s Bluetooth LE
- Audio interface: PCM
- Security: AES

3. Block Diagram

A simplified block diagram of the LS005ONWCS is depicted in the figure below.



4. Specifications Table

4.1 General Specification

Model Name	LS005ONWCS
Product Description	Support Wi-Fi 5/BT 5.2 Functionalities
Dimension	L x W x H(MAX)： 15*15*2.55(Max)mm
Main Chip	88W8987(NXP)
Standard	802.11a/b/g/n/ac
Wi-Fi Encryption	Temporal Key Integrity Protocol (TKIP) /Wired Equivalent Privacy (WEP) Advanced Encryption Standard (AES) / Counter-Mode/CBC-MAC Protocol (CCMP) Advanced Encryption Standard (AES) /Cipher-Based Message Authentication Code (CMAC) Advanced Encryption Standard (AES) / Galois/Counter Mode Protocol(GCMP) WLAN Authentication and Privacy Infrastructure (WAPI)
BT Encryption	AES
Wi-Fi Interface	SDIO3.0
BT Interface	SDIO3.0/UART
Package	Stamp
Audio interface	PCM

4.2 WLAN&BT Specification

4.2.1 2.4G WLAN Specification

Features	Description
Operating Frequency	2.412GHz~2.472 GHz
Standards	IEEE 802.11b/g/n, Wi-Fi compliant
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM
Data Rates	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: Maximum data rates up to 150Mbps (40MHz channel)
Output Power	802.11b@11Mbps : 16dBm +/-2dBm @ EVM≦35%
	802.11g@54Mbps : 14dBm +/-2dBm @ EVM≦-27dB
	802.11n@HT20 MCS 7 : 13dBm +/-2dBm @ EVM≦-28dB
	802.11n@HT40 MCS 7 : 12dBm +/-2dBm @ EVM≦-28dB
Receiver Sensitivity	802.11b@11Mbps : -84dBm
	802.11g@54Mbps : -70dBm
	802.11n@HT20 MCS 7 : -66dBm
	802.11n@HT40 MCS 7 : -64dBm
Number of Channel	USA, North America, Canada and Taiwan: (Ch. 1-11) China, Australia, Most European Countries, Japan: (Ch. 1-13)

4.2.2 5G WLAN Specification

Features	Description
Operating Frequency	5.15GHz~5.825 GHz
Standards	IEEE 802.11a/n/ac, Wi-Fi compliant
Modulation	802.11a/n/ac : OFDM
Data Rates	802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n/802.11ac: Maximum data rates up to 86.7 Mbit/s (20MHz channel), 200 Mbit/s (40MHz channel), 433Mbit/s(80 MHZ channel)
Output Power	802.11a@54Mbps : 13dBm +/-2dBm @ EVM≦-27dB
	802.11n@HT20 MCS 7 : 10dBm +/-2dBm @ EVM≦-28dB
	802.11n@HT40 MCS 7 : 10dBm +/-2dBm @ EVM≦-28dB
	802.11ac@VHT20 MCS 8 : 10dBm +/-2dBm @ EVM≦-30dB
	802.11ac@VHT40 MCS 9 : 9dBm +/-2dBm @ EVM≦-32dB
	802.11ac@VHT80 MCS 9 : 8dBm +/-2dBm @ EVM≦-32dB
Receiver Sensitivity	802.11a@54Mbps : -68dBm
	802.11n@HT20 MCS 7 : -64dBm
	802.11n@HT40 MCS 7 : -60dBm
	802.11ac@VHT20 MCS 8 : -64dBm
	802.11ac@VHT40 MCS 9 : -56dBm
	802.11ac@VHT80 MCS 9 : -52dBm
Number of Channel	USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165 Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140 China - 36,40,44,48,52,56,60,64, 149,153,157,161,165

4.2.3 BT Specification

Standard	Bluetooth 5.2
Modulation	GFSK, π/4-DQPSK, 8DPSK
Frequency Band	2402MHz~2480MHz
Output Power	BDR: typ:2dBm EDR: typ:-1dBm LE: typ:2dBm
Sensitivity	BDR(DH1): -86dBm @ BER<0.1% EDR(2DH5): -86dBm @ BER<0.01% LE : -90dBm @ BER<30.8%
Number of Channel	79 Channels

4.3 Operating Conditions

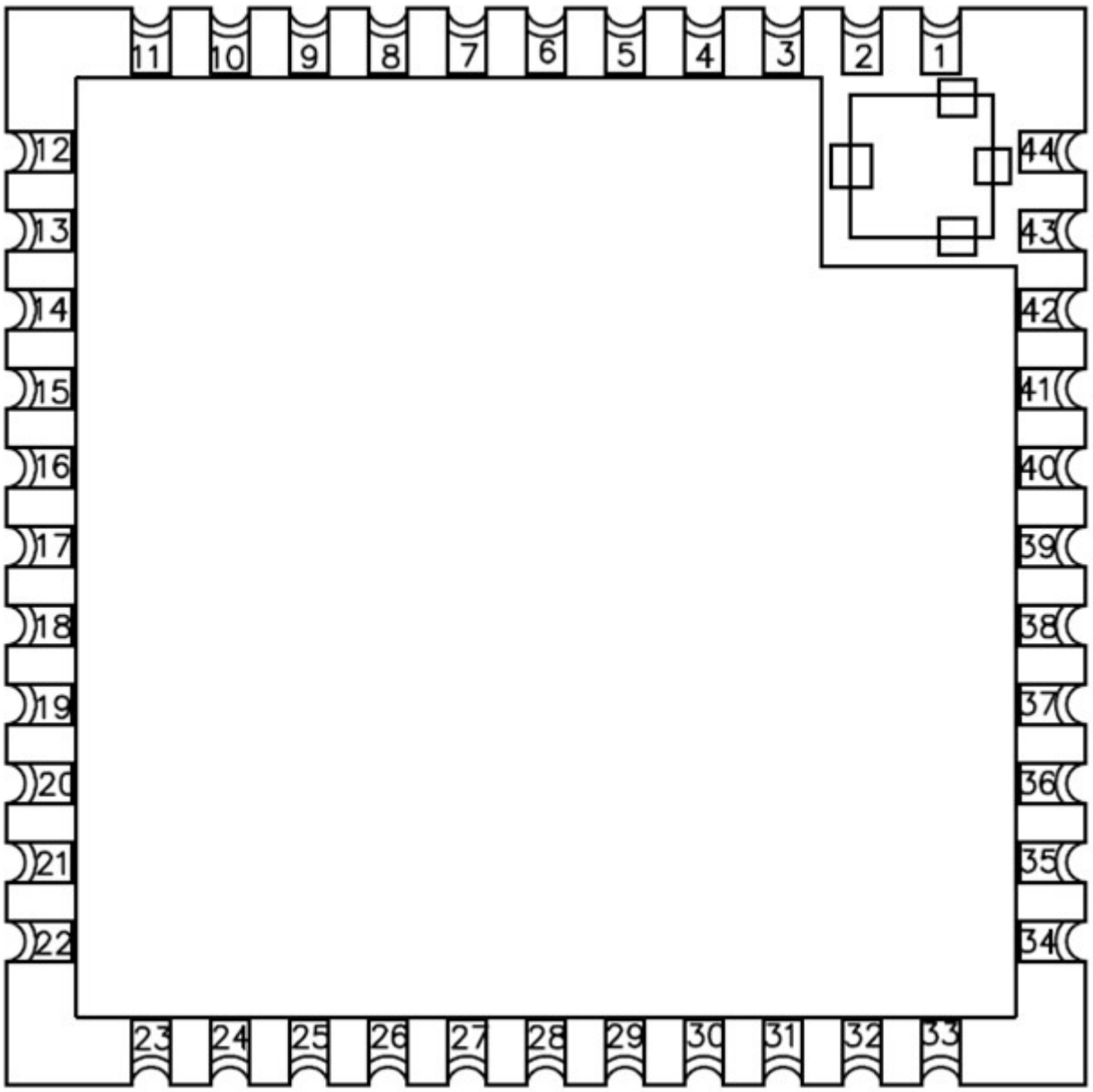
Operation Conditions	
Voltage	VDD33: 3.3V VIO: 3.3V/1.8V VIO_SD: 1.8V
Operating Temperature	-30℃ to 85℃
Storage Temperature	-40℃ to 105℃
Humidity	Less than 95% (Non-Condensing)
ESD Protection	
Human Body Model	+-2KV
Changed Device Model	+-500V

5. Pin Assignments

5.1 Pin Map

LS005ONWCS Top View Pin Map

Unit: mm



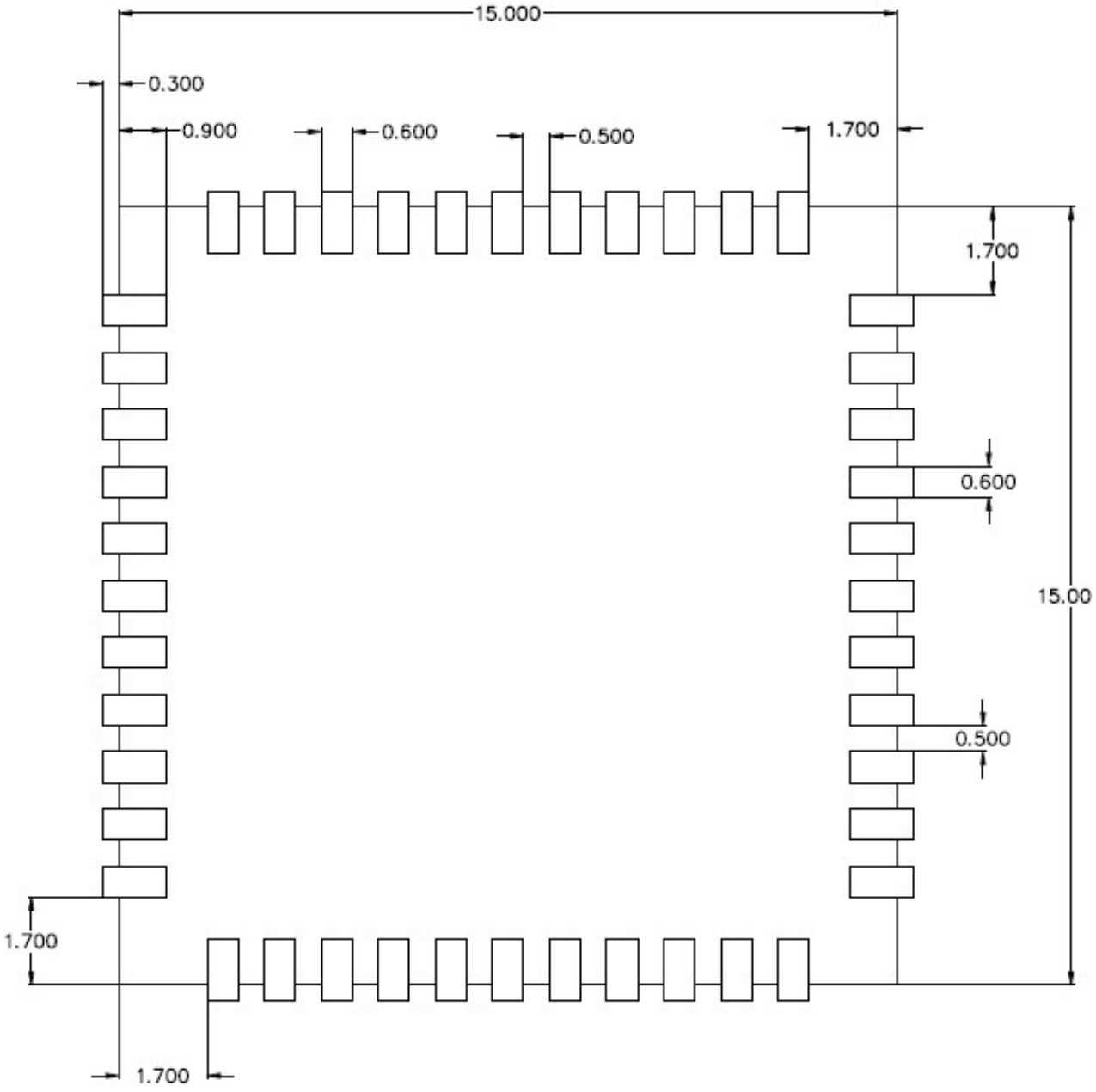
5.2 Pin Definition

Pin No	Definition	Description	Voltage	Type
1	GND	Ground connections	---	---
2	GND	Ground connections	---	---
3	NC	No connect to anything	---	Floating
4	CON[0]	10 - SDIO[WLAN] + UART[BT] 11 - SDIO[WLAN] + SDIO[BT] To set a configuration bit to 0, attach a 51k resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1	1.8V	I
5	CON[1]		1.8V	I
6	NC	No connect to anything	---	Floating
7	NC	No connect to anything	---	Floating
8	GND	Ground connections	---	---
9	GND	Ground connections	---	---
10	GND	Ground connections	---	---
11	GND	Ground connections	---	---
12	GND	Ground connections	---	---
13	GND	Ground connections	---	---
14	VDD33	3.3V power supply	3.3V	P
15	VDD33	3.3V power supply	3.3V	P
16	SLP_CLK	External Low Power Clock input(32.768KHz)	VIO	I
17	BT_RESET	BT Reset Pin	VIO	I
18	WL_RESET	WL Reset Pin	VIO	I
19	GPIO5_PCM_DOUT	GPIO Mode: GPIO[5] PCM Mode: PCM_DOUT	VIO	I/O O
20	GPIO7_PCM_SYNC	GPIO Mode: GPIO[7] PCM Mode: PCM_SYNC	VIO	I/O I/O
21	System_PDn	Full Power-down (active low) Low: Full power-down mode High: Normal mode internal pull-up on this pin	VIO	I

22	WL_WAKE_HOST	WL device wake-up HOST	VIO	O
23	GPIO4_PCM_DIN	GPIO Mode: GPIO[4] PCM Mode: PCM_DIN	VIO	I/O I
24	BT_WAKE_HOST	Bluetooth device to wake-up HOST	VIO	O
25	GPIO6_PCM_CLK	GPIO Mode: GPIO[6] PCM Mode: PCM_CLK	VIO	I/O I/O
26	GPIO3	GPIO[3]	VIO	I/O
27	SD_CMD	SDIO Command	VIO_SD	I/O
28	SD_CLK	SDIO Clock input	VIO_SD	I
29	SD_D0	SDIO Data line 0	VIO_SD	I/O
30	SD_D1	SDIO Data line 1	VIO_SD	I/O
31	SD_D2	SDIO Data line 2	VIO_SD	I/O
32	SD_D3	SDIO Data line 3	VIO_SD	I/O
33	GND	Ground connections	---	---
34	VIO_SD	1.8V Digital I/O SDIO Power Supply	1.8V	P
35	NC	No connect to anything	---	Floating
36	NC	No connect to anything	---	Floating
37	GND	Ground connections	---	---
38	VIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	p
39	BT_UART_RXD	UART_RXD	VIO	I
40	BT_UART_TXD	UART_TXD	VIO	O
41	BT_UART_RTS	UART_RTS	VIO	O
42	BT_UART_CTS	UART_CTS	VIO	I
43	BT_WAKE	HOST wake-up Bluetooth device	VIO	I
44	WL_WAKE	HOST wake-up WLAN device	VIO	I

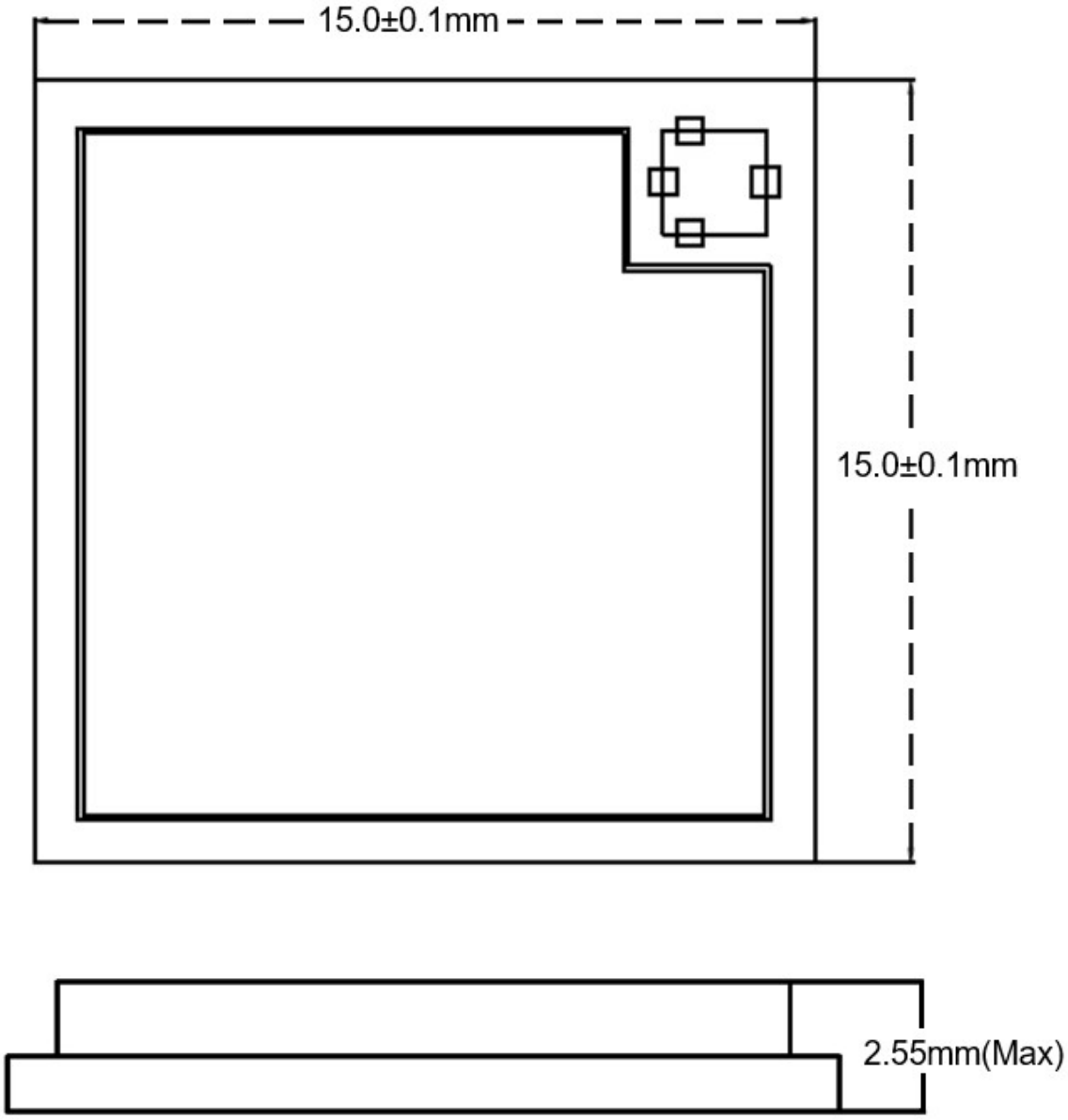
5.3 Layout Recommendation

Unit: mm



5.4 Physical Dimensions

Unit: mm



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VDD33	3.3V power supply	--	3.3	4.0	V
VIO	1.8V/3.3V digital I/O power supply	--	1.8	2.2	V
		--	3.3	4.0	V
VIO_SD	1.8V digital SDIO I/O power supply	--	1.8	2.2	V

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	3.3V power supply	3.07	3.3	3.53	V
VIO	1.8V/3.3V digital I/O power supply	1.67	1.8	1.92	V
		3.07	3.3	3.53	V
VIO_SD	1.8V digital SDIO I/O power supply	1.67	1.8	1.92	V

6.3 DC Characteristics

6.3.1 VIO DC characteristics-3.3V/1.8V operation

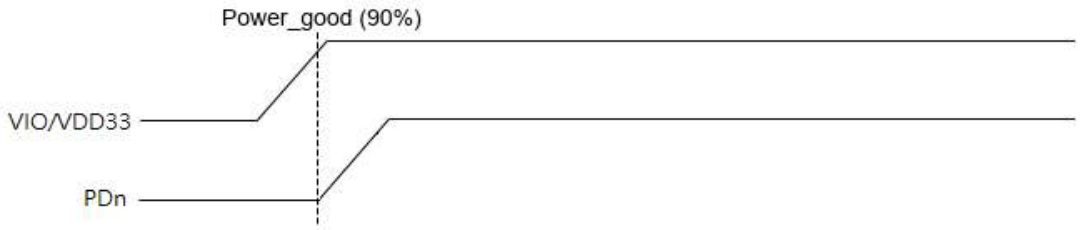
Symbol	Parameter	Condition	Min	Typ	Max	Units
VIH	Input high voltage	--	0.7*VIO	--	VIOI+0.4	V
VIL	Input low voltage	--	-0.4	--	0.3*VIO	V
VHYS	Input hysteresis	--	100	--	--	mV
VOH	Output high voltage	--	VIO-0.4	--	--	V
VOL	Output low voltage	--	--	--	0.4	V

6.3.2 VIO_SD DC characteristics-1.8V operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIH	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
VIL	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
VHYS	Input hysteresis	--	100	--	--	mV
VOH	Output high voltage	--	VIO_SD-0.4	--	--	V
VOL	Output low voltage	--	--	--	0.4	V

6.3.3 Power up Timing Sequence

VIO/VDD33 must be good (90%) before or at the same time PDn starts ramping up.



7. Host Interface

7.1 SDIO Interface

7.1.1 Introduction

The LS005ONWCS supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The LS005ONWCS acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

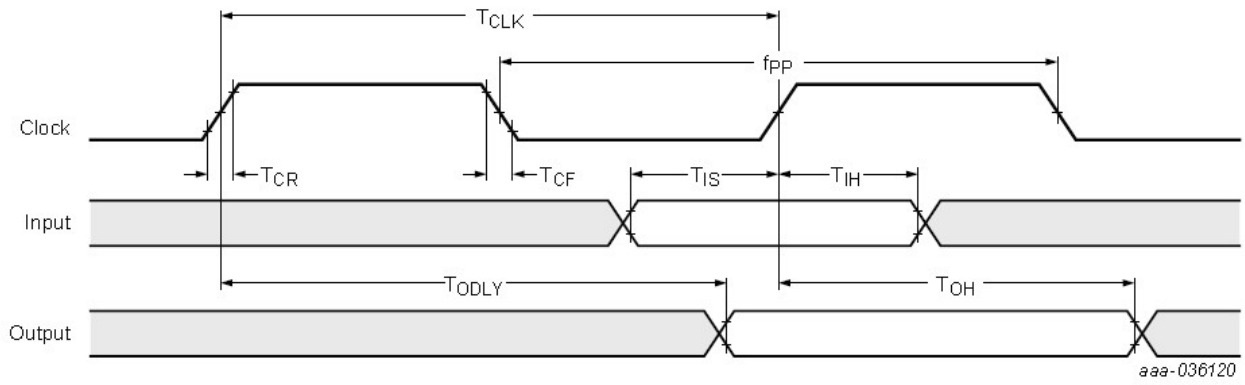
Main features of the SDIO device interface include:

- Supports SDIO 3.0 Standard
- On-chip memory used for CIS
- Supports 4-bit SDIO and 1-bit SDIO transfer modes
- Special interrupt register for information exchange

7.1.2 SDIO Interface Signals

Pin Name	Type	Description
SD_CMD	I/O	SDIO 4-bit Mode: Command line SDIO 1-bit Mode: Command line
SD_CLK	I	SDIO 4-bit Mode: Clock SDIO 1-bit Mode: Clock
SD_D0	I/O	SDIO 4-bit Mode: Data line Bit[0] SDIO 1-bit Mode: Data line
SD_D1	I/O	SDIO 4-bit Mode: Data line Bit[1] SDIO 1-bit Mode: Interrupt
SD_D2	I/O	SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) SDIO 1-bit Mode: Read wait (optional)
SD_D3	I/O	SDIO 4-bit Mode: Data line Bit[3] SDIO 1-bit Mode: Not used

7.1.3 SDIO Timing Diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz)

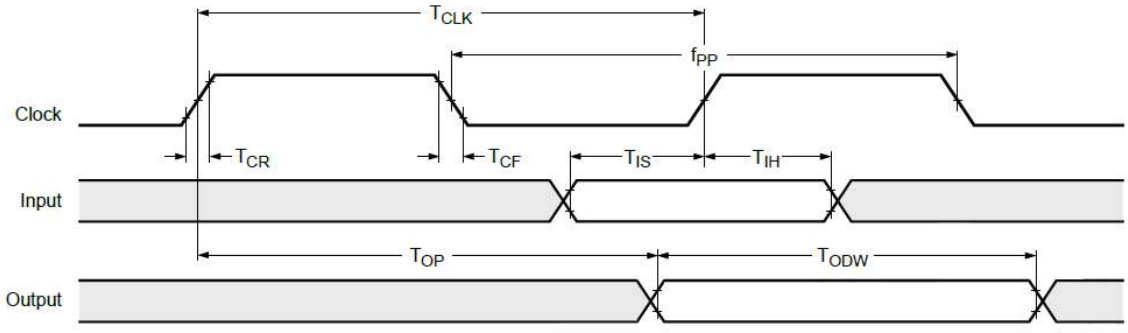


SDIO Timing Diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

✧ SDIO Timing Data——SDR12, SDR25, SDR50 Modes (up to 100 MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR},T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time CL ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time CL = 15 pF	SDR12/25/50	1.5	--	--	ns

7.1.4 SDIO Timing Diagram—SDR104 mode (208MHz)



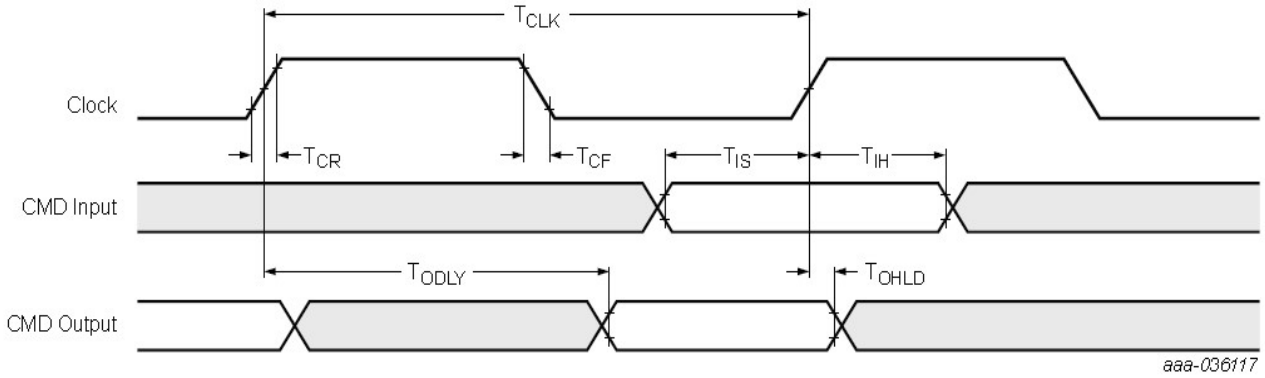
SDIO Timing Diagram—SDR104 Modes (208 MHz)

✧ SDIO Timing Data——SDR104 Mode(208MHz)

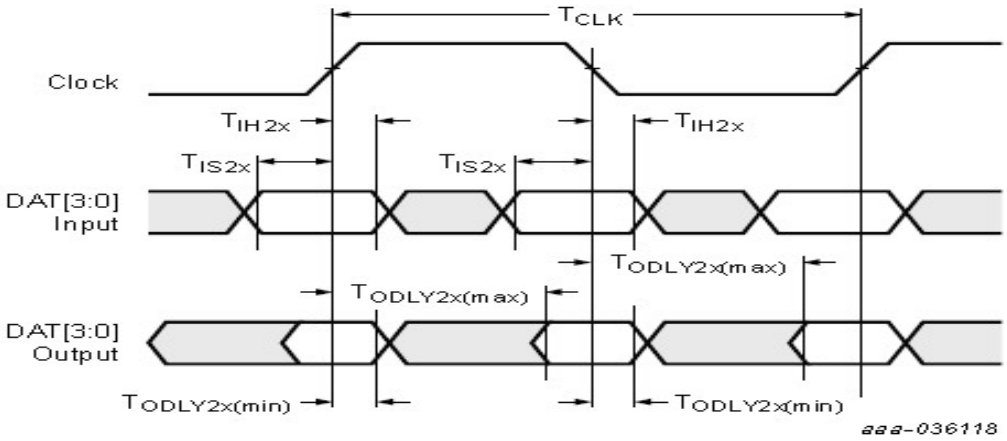
Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns

T_{CR},T_{CF}	Rise time, fall time T_{CR},T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

7.1.5 SDIO Timing Diagram—DDR50 Mode (50 MHz)



SDIO CMD Timing Diagram—DDR50 Mode (50 MHz)



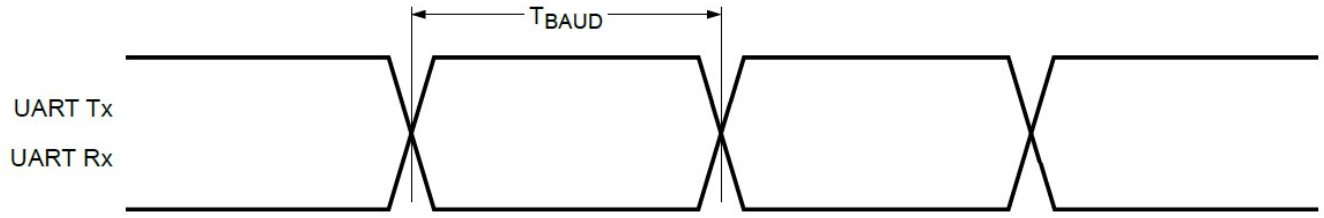
SDIO DAT[3:0] Timing Diagram—DDR50 Mode

✧ SDIO Timing Data——DDR50 Mode(50MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR},T_{CF}	Rise time, fall time T_{CR},T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD}=10 pF	DDR50	--	--	0.2*T_{CLK}	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD}≤10 pF(1 card)	DDR50	6	--	--	ns
T_{IH}	Input hold time C_{CARD}≤10 pF(1 card)	DDR50	0.8	--	--	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L≤30pF(1 card)	DDR50	--	--	13.7	ns
T_{OHLD}	Output hold time C_L≥15pF(1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edge)						
T_{IS2X}	Input setup time C_{CARD}≤10 pF(1 card)	DDR50	3	--	--	ns
T_{IH2X}	Input hold time C_{CARD}≤10 pF(1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edge)						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode C_L≤25pF(1 card)	DDR50	--	--	7.0	ns
$T_{ODLY2X(min)}$	Output hold time C_L ≥15pF(1 card)	DDR50	1.5	--	--	ns

7.2 UART Host Interface

7.2.1 High-Speed UART Specifications



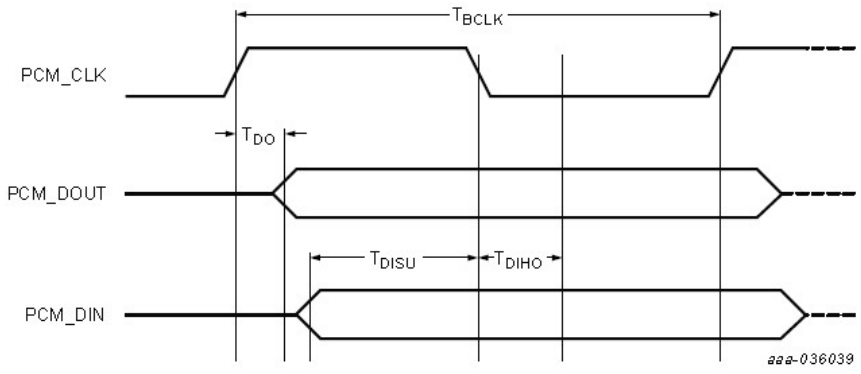
UART Timing Diagram

7.2.2 UART Timing Data

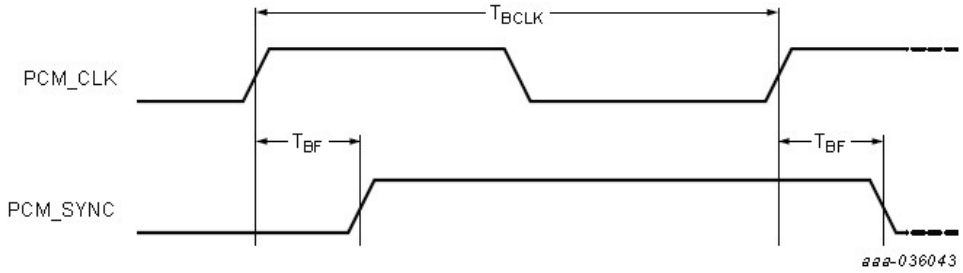
Symbol	Parameter	Condition	Min	Typ	Max	Units
TBAUD	Baud rate	38.4MHz input clk	250	--	--	ns

7.3 PCM Interface

7.3.1 PCM Timing Diagram—Master Mode



PCM Timing Specification Diagram for Data Signals—Master Mode

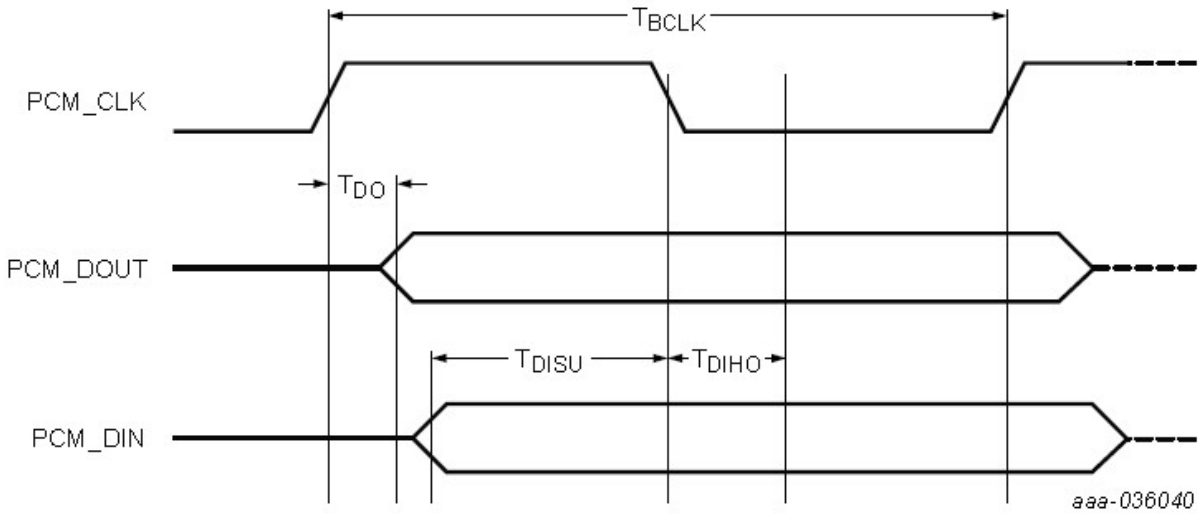


PCM Timing Specification Diagram for PCM_SYNC Signal—Master Mode

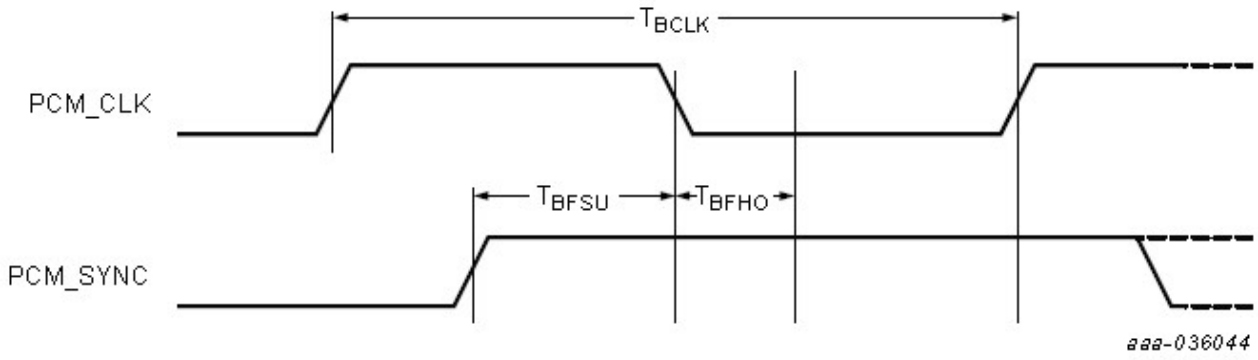
✧ PCM Timing Specification Data—Master Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

7.3.2 PCM Timing Diagram—Slave Mode



PCM Timing Specification Diagram for Data Signals—Slave Mode



PCM Timing Specification Diagram for PCM_SYNC Signal—Slave Mode

✧ PCM Timing Specification Data—Slave Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
T_{BCLK} rise/fall	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns

T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

8. FCC Statement:

Please take attention that changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

8.1 Operational use conditions

Module has professional users use condition limitations, Host product manufacturer please ensure giving such warning like "Product is limited to professional users use"in your product's instruction.

8.2 Antenna used

	Antenna Type	Max. Antenna Gain
BT	PCB Antenna	3.21dBi
BLE	PCB Antenna	3.21dBi
2.4G Wi-Fi	PCB Antenna	3.21dBi
5G Wi-Fi	PCB Antenna	U-NII-1: 3.35dBi
		U-NII-2A: 3.71dBi
		U-NII-2C: 3.83dBi
		U-NII-3: 3.08dBi

8.3 Labelling Instruction for Host Product Integrator

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. For FCC, this exterior label should follow “Contains FCC ID: 2A2EX-LS005”. In accordance with FCC KDB guidance 784748 Labeling Guidelines.

§ 15.19 Labelling requirements shall be complied on end user device. Labelling rules for special device, please refer to § 2.925, § 15.19 (a)(5) and relevant KDB publications. For E-label, please refer to § 2.935.

8.4 Installation Notice to Host Product Manufacturer

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.
The module is limited to installation in mobile application, a separate approval is required for all other operating configurations, including portable configurations with respect to § 2.1093 and difference antenna configurations.

8.5 Antenna Change Notice to Host manufacturer

If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

8.6 FCC other Parts, Part 15B Compliance Requirements for Host product manufacturer

This modular transmitter is only FCC authorized for the specific rule parts listed on our grant, host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.
Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.
Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in § 15.105 Information to the user or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:

8.7 For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help.

8.8 For Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.